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NÁVRH ANALOGOVÝCH OBVODŮ S NÍZKÝM NAPÁJECÍM NAPĚTÍM A NÍZKÝM PŘÍKONEM.

LOW VOLTAGE LOW POWER ANALOGUE CIRCUITS DESIGN.

TEZE DIZERTAČNÍ PRÁCE
SHORT VERSION OF DOCTORAL THESIS

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Nízké napětí, nízký příkon, návrh analogových obvodů, tranzistor řízený substrátem, tranzistor s plovoucím hradlem, tranzistor s kvazi plovoucím hradlem, aktivní filtry, aktivní prvky.

KEYWORDS

Low voltage, low power, analog circuit design, bulk–driven transistor, floating–gate transistor, quasi–floating–gate transistor, active filter, active element.

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INTRODUCTION

In the last decade, with the continuous scaling in the feature size of the transistors, nominal supply voltage of CMOS integrated circuits has been dramatically decreased due to the strongly emerging consumer market for portable devices that needed to be light weighted and hence operate for a long period of time with a small battery. When a MOS transistor size is scaled down, the thickness of the gate oxide is reduced. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from a breakdown due to higher electrical field across the gate oxide, and to ensure its reliability, the supply voltage needs to be reduced. Therefore, low–voltage (LV) low–power (LP) analog circuits have received significant attention and have become increasingly important in the electronic industry. The primary application targets of these circuits are low power Systems–on–Chips (SOCs). That covers markets such as: Mobile Internet Services (Smartphones, Tablets, Netbooks), Cellular Telecom, Home and Mobile Multimedia, etc. The idea of SOC came up originally from universal fact that the outside world is mostly analog in nature and that the bandwidth of a signal can become a magnitude higher if the signal is processed in analog circuits. Thus, it became inevitable to introduce analog signal processing.

However, system portability usually requires battery supply and therefore weight/energy storage considerations. For the time being, battery technologies do not proportionally evolve with the speed of the applications demand. Therefore the challenge is to reduce the power consumption of the circuits.

On the other hand, the new trend of the design of modern implantable or portable biomedical devices is toward miniaturization and portability for long–term monitoring. Crucial parameters for these healthcare electronics are low power consumption and low supply voltage, and that makes biomedical applications another major target of low–power analog circuits. Biomedical signals have very low amplitude in the range of microvolts to millivolts. For example, EEG signals (Electroencephalography signals), are varying between 5 and 100 microvolts. Due to their low–level amplitude, integrated circuits are essential to be designed for the amplification of the weak signals before any further signal processing can be performed to make them compatible with devices such as displays, recorders, or A/D converters for computerized equipment.

1. STATE OF THE ART

Low–voltage low–power capability could be achieved either by developed technologies or by design techniques.

Developed technologies are CMOS technology, BiCMOS technology, SOI (Silicon On Insulator) technology and Multi–gate transistors.

On the other hand, since a MOST's sub–threshold leakage current, $I_{leakage}$, is exponentially dependent upon the threshold voltage, V_T has not been able to decline as quickly as the power supply voltage V_{DD} does in each new process generation because of concerns over increasing P_{avg} through P_{static}. In order to overcome this restriction many techniques have been introduced in the literature based on CMOS technology. By utilizing these techniques, the threshold voltage is decreased or –in some cases– even removed. LV design techniques are divided into two categories: conventional and non–conventional.

The most widely used conventional techniques for LV LP analog circuits design are: circuits with rail–to–rail operating range, MOS transistors operating in weak inversion region, level shifter technique and MOS transistors in self–cascode structure. While the most widely used non–conventional approaches for LV LP analog circuits design are: bulk–driven (BD) MOST, floating–gate (FG) approach, quasi–floating–gate (QFG) approach and bulk–driven floating–gate (BD FG) and bulk–driven quasi–floating–gate (BD QFG) approach.

Both conventional and non–conventional design techniques have advantages and drawbacks. Examples of these advantages and disadvantages include, but not limited to, the following: rail–to–rail operating range circuits with acceptable signal–to–noise ratio but suffer from complexity to obtain a constant transconductance value. Sub–threshold circuits have low biasing currents but have very low transition frequency. Level shifter technique offers low input resistance but suffers from the offset current. Self–cascode structure offers output impedance similar to a regular cascode but suffers from limited input common mode range. BD MOSTs offer better linearity but suffer from limited gain. FG MOSTs offer rail–to–rail operation but consume much larger silicon area. QFG MOSTs do not consume much larger silicon area as floating–gate MOSTs do, but they high–pass filter the applied signal. BD FG and BD QFG combine the most advantages of BD, FG and QFG technique, but concurrently combine some disadvantages of them.

2. THESIS OBJECTIVES AND RESULTS

In references there are plenty of examples of analog basic building blocks (such as differential operational amplifiers, current mirrors, current conveyors, operational transconductance amplifiers, voltage followers, filters and more) implemented utilizing some of the LV LP techniques. Besides the conventional building blocks, over the course of past twenty years, designers have searched for new active elements for several reasons such as increasing the universality of the element, eliminating parasitic effects and minimizing the number of these elements in their applications. As a consequence, new circuit elements have appeared such as OTRA (Operational Trans–Resistance Amplifier), CDBA (Current Differencing Buffered Amplifier), CDTA (Current Differencing Transconductance Amplifier), CTTA (Current–Through Transconductance Amplifier) VDTA (Voltage Differencing Transconductance Amplifier), and others.

The main goal of this thesis is to design and simulate novel CMOS structures of basic building blocks and active elements so they can operate at very low power supply voltage levels (average of 0.6 V) and consume very low power (average of 20 μW) for 0.18 μm CMOS technology, extending common–mode dynamic range while preserving other characteristics acceptable for many applications.

2.1 BULK–DRIVEN QUASI–FLOATING–GATE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (BD–QFG OTA)

A new LV LP BD–QFG OTA is presented. The proposed circuit is designed using 0.18 μm CMOS technology. Fig. 1 shows the proposed configuration. The circuit is consisted of two stages. The first stage is consisted of a bulk–driven quasi–floating–gate differential input M_1 and M_2. The gates of these transistors are tied to the negative supply voltage V_{SS} through extremely high value resistors constructed by transistors M_{b1} and M_{b2} which are operating in cutoff region. The input terminals are connected to M_1 and M_2 from two sides: capacitively coupled to the quasi–floating gates via C_1 and C_2 from one side, and connected to bulk terminals from other side. Transistors M_4, M_5, M_6 and M_7 act as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit. Transistors M_5 and M_6 form the active load and transistor M_3 acts as tail current source for the differential input stage. The input voltage terminals are connected to the bulk terminals of M_1 and M_2, therefore high input impedances are achieved.

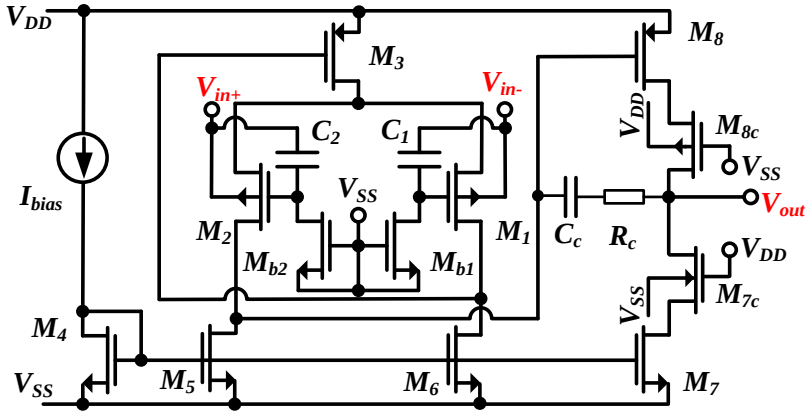


Fig. 1. The internal structure of BD–QFG OTA.

The use of bulk–driven quasi–floating–gate flipped voltage follower for the differential input stage makes the minimum power supply voltage $V_{DD\,(\min)}$. The supply voltage is given by:

$$V_{DD\,(\min)} = V_{GS\,(M3)} + V_{DS\,(M5)}. \tag{1}$$

Equation (1) shows the capability of the proposed BD–QFG OTA structure for operation under lower supply voltage. The second stage is consisted of M_7, M_{7c} and M_8, M_{8c}. Cascode structure is used to implement the gain stage in order to provide significantly high–value output impedance, consequently to achieve high voltage gain. Output impedance can be calculated from the following equation:

$$r_o = \frac{1}{\dfrac{g_{o,M7}g_{o,M7c}}{g_{m,M7c}+g_{mb,M7c}} + \dfrac{g_{o,M8}g_{o,M8c}}{g_{m,M8c}+g_{mb,M8c}}}. \tag{2}$$

2.1.1 BD–QFG OTA–based diode–less precision rectifier

Traditional methods of realizing precision rectifier circuits include the use of operational amplifiers, resistors, and either diodes [1–5] or alternating source–followers [6]. A number of current conveyors–based current–mode rectifier circuits are existed in the literature [7–13].

Diode–less half wave rectifier based on bulk–driven quasi–floating gate OTA is shown in Fig. 2. This circuit is a WTA–like (winner take all) circuit. The principle of work is as follow: if we applied a voltage signal to V_{in} terminal and a zero to V_{off} terminal, the output voltage would equal to the maximum voltage of both inputs. In other words, the positive half of the signal wave is

passed, while the other half is blocked. For an input voltage V_{in} the ideal half–wave rectified output V_{out} is given by:

$$V_{out} = \begin{cases} V_{in} & if\ V_{in} > 0 \\ 0 & otherwise \end{cases}. \tag{3}$$

It is worth mentioning that the same configuration shown in Fig. 2 could be used as full–wave rectifier just by applying $-V_{in}$ (an identical signal of V_{in} shifted 180°) to V_{off} terminal.

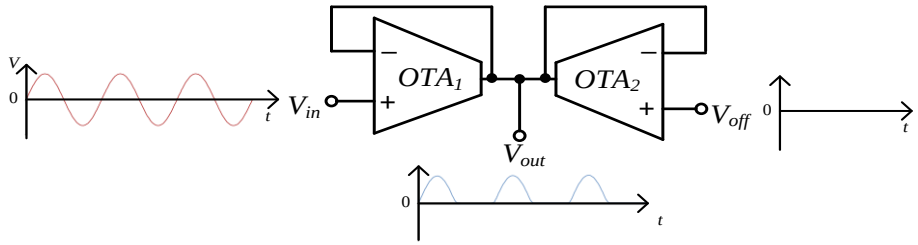


Fig. 2. BD–QFG half–wave rectifier.

2.1.2 Simulation results

The proposed BD–QFG OTA was designed and simulated using TSMC 0.18 μm N–well CMOS. The used PSpice model is available on [14]. The supply voltage was ±0.3 V, the biasing current was I_{bias} = 5 μA and the power consumption was 13.4 μW. The optimal transistor aspect ratios and the values of components are given in Tab. 1. Tab. 2 shows a list of measured operational amplifier benchmarks used to evaluate proposed OTA. Features of the circuit (shown in Fig. 1) are listed in the first column, along with values of other works listed in other columns. The AC gain and phase responses of the BD–QFG OTA with 3 pF load capacitance are shown in Fig. 3. The open–loop gain is 80 dB and the gain–bandwidth product is 6.4 MHz. The phase margin is 65º which guarantees the circuit stability. The voltage follower frequency response of the proposed circuit, which obtains 15 MHz, is shown in Fig. 4.

The diode–less half–wave precision rectifier shown in Fig. 2 was simulated using BD–QFG OTA shown in Fig. 1. The supply voltage of ±0.3 V and the bias current of I_{bias} = 5 μA for OTAs were used. The circuit consumes 26.8 μW. Fig. 5 shows the DC transfer characteristic of BD–QFG half–wave rectifier in comparison with the ideal one and it confirms the precise rectification for input amplitude ranging ±250 mV.

Tab. 1. Transistors aspect ratios for Fig. 1.

BD–QFG OTA	W/L [µm/µm]
M_1, M_2	20/0.3
M_{b1}, M_{b2}	30/2
M_3, M_8	100/0.3
M_4 , M_5, M_6	4/0.3
M_7	8/0.3
M_{7c}	45/2
M_{8c}	100/2
C_1= C_2=0.4 pF	
R_c= 10 kΩ, C_c = 3 pF	

Tab. 2. BD–QFG OTA performance benchmark indicators.

Parameters		**Proposed OTA**	**Koziel [18]**	**Majumdar [18]**	**Li [20]**	**Zhang [21]**
CMOS Technology	[µm]	0.18	0.5	0.35	0.35	0.18
Power supply	[V]	± 0.3	± 2.5	3.3	3.3	1.8
Power consumption	[µW]	13.4	6800	3370	2330	590
Transistors number	[/]	12	37	14	22	68
AC Gain	[dB]	51	65	80.4	65	55
Linearity range	[mV]	± 0.3	± 0.75	± 0.1	/	± 0.27
Output resistance	[MΩ]	0.317	3.4	/	1.2	8.3
–3dB bandwidth	[MHz]	59	100	123.2	100	200

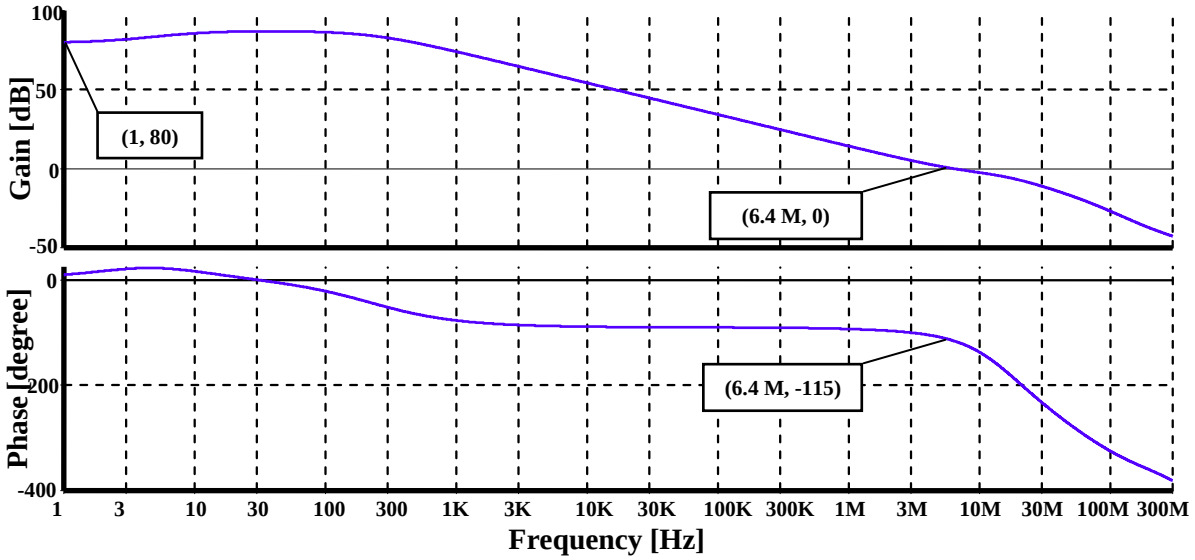


Fig. 3. Frequency response of BD–QFG OTA.

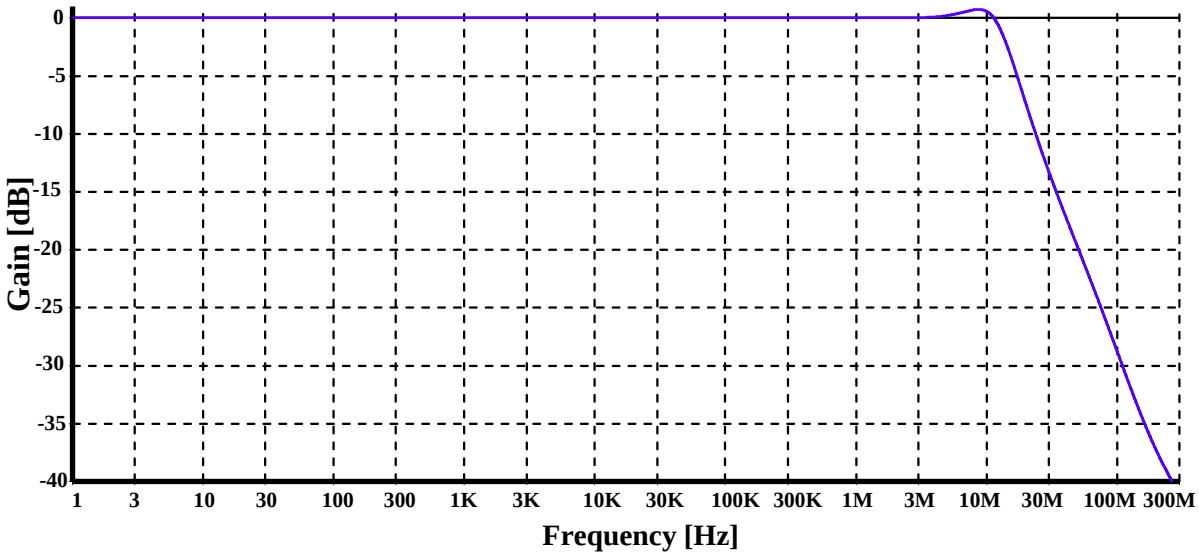


Fig. 4. Frequency response of OTA as a voltage follower.

Fig. 6 shows the transient response of the output waveforms for input signal of 15 kHz and amplitudes from 50 mV to 125 mV with step of 25 mV. It is obvious from that the rectifier is capable to rectify a wide range of amplitudes.

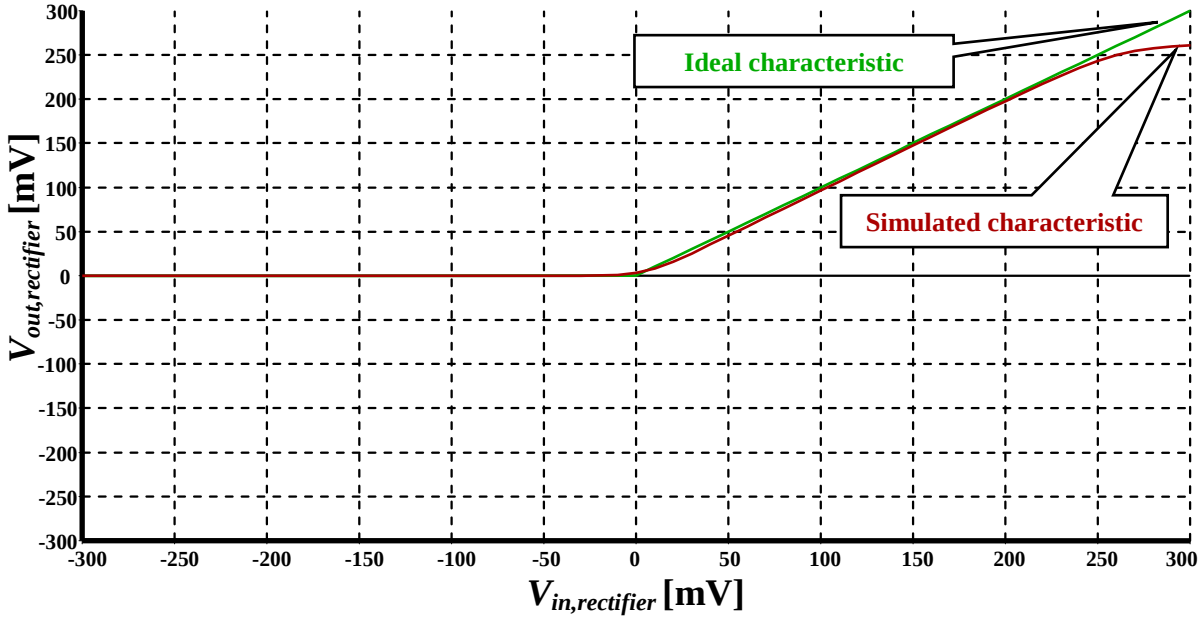


Fig. 5. DC transfer characteristic of BD-QFG Half-wave rectifier.

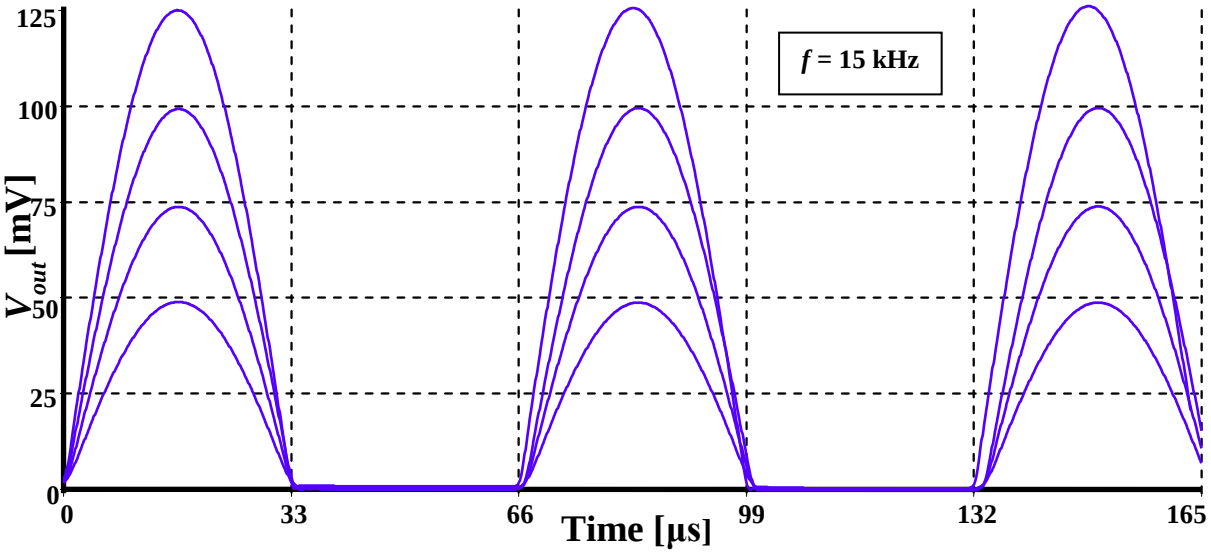


Fig. 6. Transient analyses of output waveforms with 15 kHz and various amplitudes of the input signal.

2.2 FLOATING–GATE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (FG OTA)

A configuration of operational transconductance amplifier (OTA) based on floating–gate MOSTs suitable for LV LP applications is presented. The circuit presented is a two–stage transconductance amplifier. The scheme uses *P*–channel floating–gate transistors at the input, M_1 and M_2, each with two gates. As specified by the name, the circuit is the cascade of two stages: The first is a differential amplifier which consists of input devices M_1, M_2 and the current mirror M_3, M_4 which is acting as an active load, the second stage is a conventional inverter with M_5 as a driver and M_6 as an active load. See Fig. 7.

The current of M_1 is mirrored by M_3, M_4 and subtracted from the current comes from the drain of M_2, then the signal contributions of the two currents multiplied by the output resistance of the first stage give the single–ended first stage output voltage. This resulting signal constitutes the input of the second gain stage. It is important to notice that all transistors are working in the saturation area. Compensation capacitor C_C takes care of compensation requirements since it connects gain stage's output of the OTA with its input. By the means of C_C, the dominant (first) pole's frequency is shifted down from 100 kHz to 3 kHz.

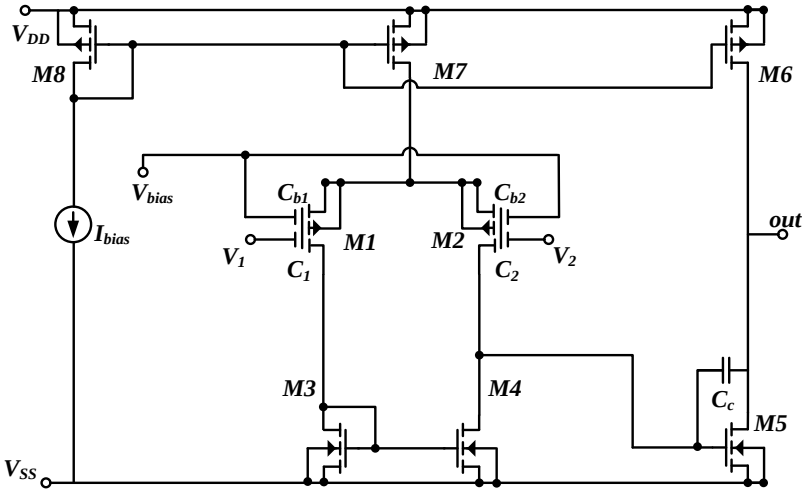


Fig. 7. The circuit of two–stage OTA using FG–MOSTs.

2.2.1 FG OTA based tunable voltage differencing transconductance amplifier (FG VDTA)

Tunable active circuit element VDTA (Voltage Differencing Transconductance Amplifier) based on floating–gate MOSTs is proposed in this section. The mentioned VDTA is brought as the convenient element for current mode signal processing, which might be very suitable for variety of applications such as biquad filters. This active circuit element is a type of analog block consists of two multiple–output operational transconductance amplifiers (MO–OTAs) using floating–gate MOSTs as input stage. The internal structure of the VDTA is shown in Fig. 8. Output current of input stage flows out of the VDTA terminal "z" into an outside load if desired. The voltage across the z–terminal is converted through a transconductance g_{mx} into two or more output currents with opposite polarity. To increase the universality of the element, it is completed of the I_z copy, this attribute can be implemented by several methods, and the one addressed in [15] is adopted. To further increase the versatility of the configuration, it is designed to allow orthogonal tuning capability through transconductance control by the amplifier bias current (I_{bias}) of each OTA, the main component of the proposed circuit. The VDTA can be remarkably used in filters; it can implement low–pass, band–pass, high–pass, band–notch, and all–pass filters.

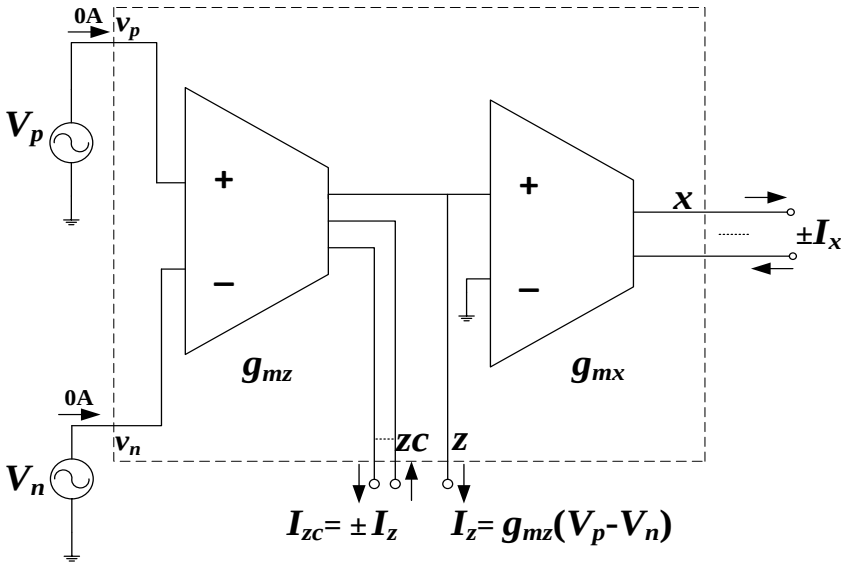


Fig. 8. VDTA element as a connection of two MO–OTAs.

As an application example of the proposed FG VDTA, a biquad filter is implemented as shown in Fig. 9. [16]. Fig. 9 presents a SIMO OTA–C filter based on VDTA configuration.

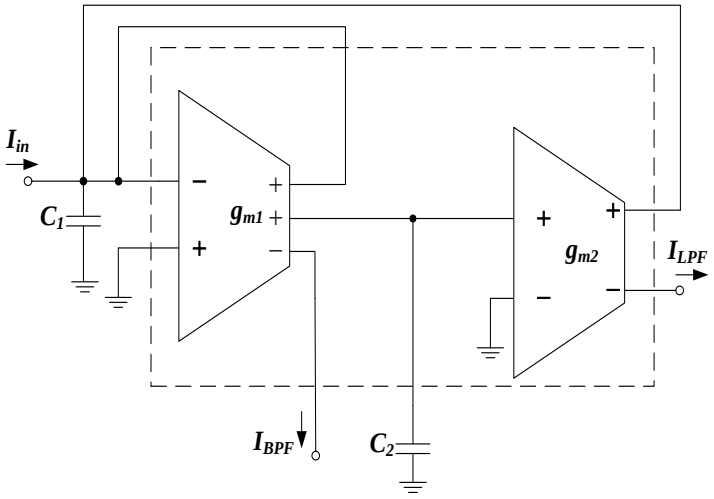


Fig. 9. Single–input multiple–output biquad filter based on FG VDTA.

2.2.2 Simulation results

Tab. 3 summarizes the performance of OTA in proposed VDTA. Component values are given in Tab. 4, transistor aspect ratios as well as their biasing currents are given in Tab. 5. Tab. 6 shows a list of measured operational amplifier benchmarks used to evaluate proposed OTA. Features of the circuit (shown in Fig. 7) are listed in the first column, along with values of other works listed in other columns. The AC gain and phase responses of the FG OTA with

1 pF load capacitance are shown in Fig. 10. Fig. 11 shows simulated transient responses of the FG OTA. The input range has been determined with the OTA connected as a buffer, and a 10 kHz sinusoidal input signal, allowing a maximum total harmonic distortion (THD) at the output of 0.93%.

Tab. 3. Summary of the performance for OTA.

Characteristics	Simulated results
Voltage gain	51 dB
CMRR	61 dB
Offset voltage	176 μV
GBW	3.15 MHz
Phase margin	80◦
Power consumption	36 μW
Slew rate	4.35 V/μs
Settling time	670 ns
Input range	0.8 V_{pp} = 0.78 V_{DD}
Output impedance	160 kΩ

Tab. 4. Measurement conditions of the circuit.

Parameter	Value
C_{b1}, C_{b2}	0.3 pF
C_1, C_2	0.1 pF
C_c	1 pF
V_b	–0.3 V

Tab. 5. Transistors dimensions.

Device	Type	L/W [μm]	I_d [μA]
M_1, M_2	PMOS	0.2/10	2.3
M_3, M_4	NOMS	0.8/10	2.3
M_5	NOMS	0.6/40	9.7
M_6	PMOS	0.8/40	9.5
M_7	PMOS	0.8/20	4.6
M_8	PMOS	0.8/20	5

Tab. 6. FG OTA performance benchmark indicators.

Parameters		Proposed OTA	Koziel [18]	Majumdar [19]	Li [20]	Zhang [21]
CMOS Technology	[μm]	0.18	0.5	0.35	0.35	0.18
Power supply	[V]	± 0.5	± 2.5	3.3	3.3	1.8
Power consumption	[μW]	36	6800	3370	2330	590
Transistors number	[/]	8	37	14	22	68
AC Gain	[dB]	51	65	80.4	65	55
Linearity range	[mV]	± 0.5	± 0.75	± 0.1	/	± 0.27
Output resistance	[MΩ]	0.16	3.4	/	1.2	8.3
–3dB bandwidth	[MHz]	2	100	123.2	100	200

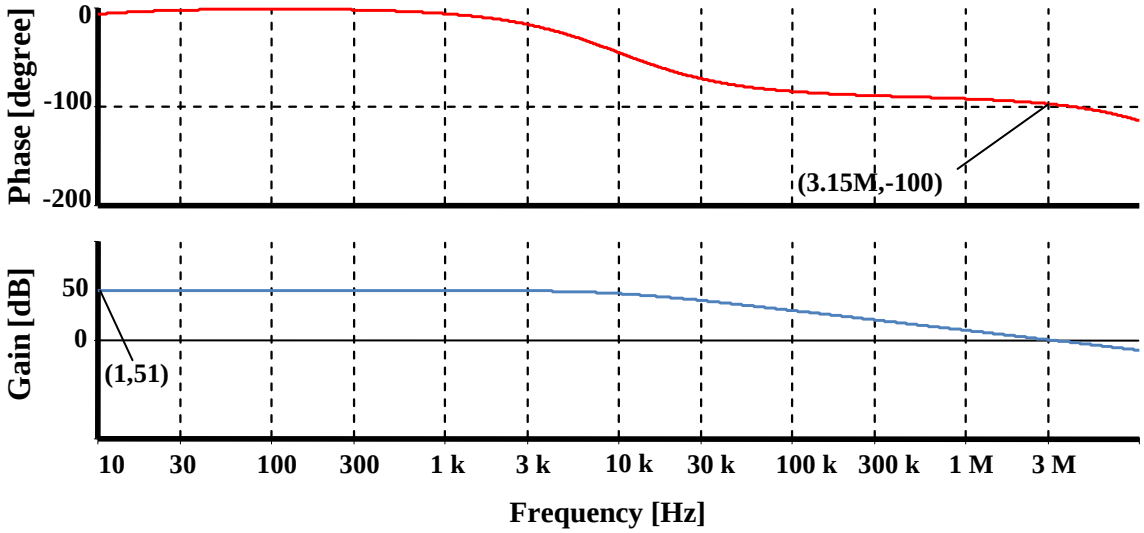


Fig. 10. Frequency response of FG–OTA.

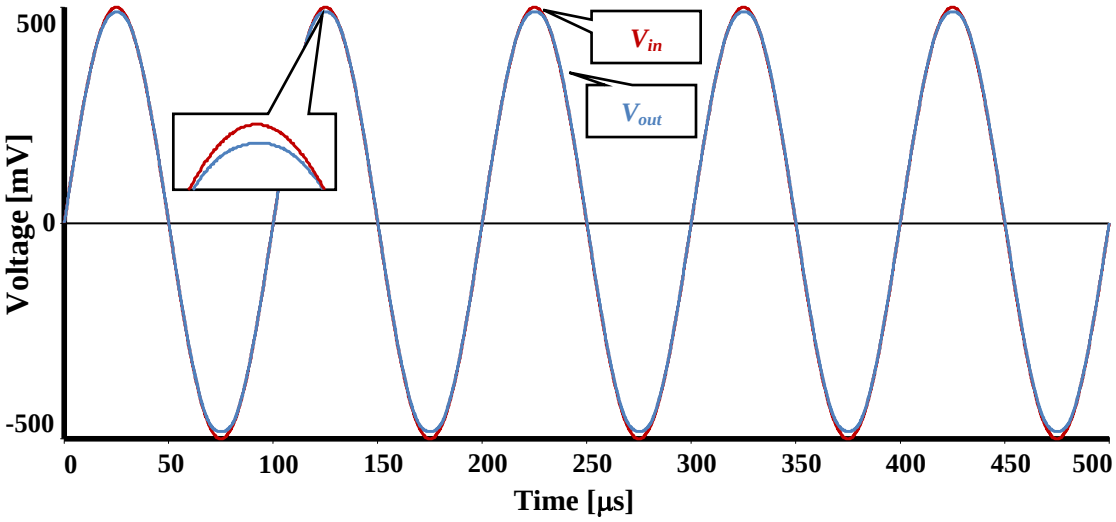


Fig. 11. Input and output signals vs. time.

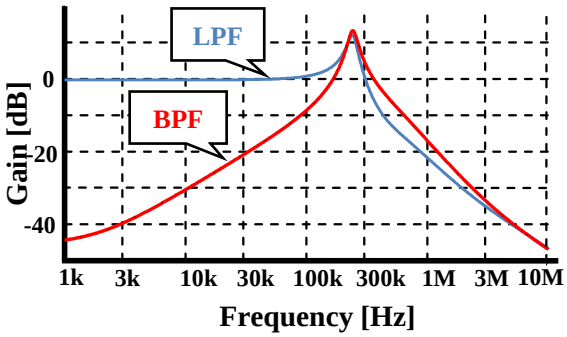


Fig. 12. Simulated frequency responses of low-pass and band–pass signals shown in Fig. 9.

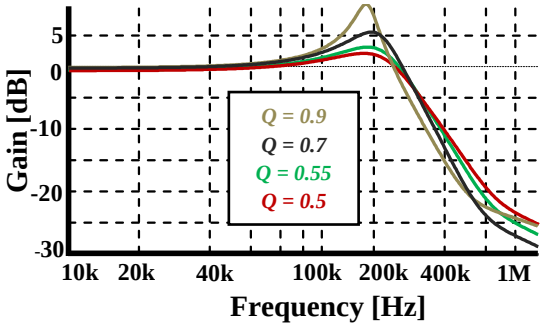


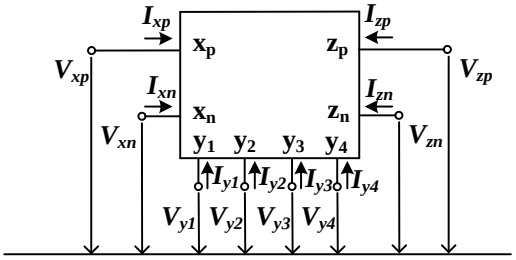
Fig. 13. Low-pass filter peaking vs. Q (G_{m1} is variable).

Fig. 12 shows the simulated low–pass and band–pass results. We observe from the figure some peaking in the low–pass filter response; the reason is the value of Q (Q is 1.225 > 0.707). We can avoid this by reducing Q's value to remain under 0.707 by altering the value of g_{m1}, which is possible thanks to tunability of the circuit. The amount of peaking for the low–pass filter vs. Q is indicated in Fig. 13.

2.3. FULLY DIFFERENTIAL CCII (FD–CCII)

Second generation current conveyors are powerful and simple at the same time, but on the other hand, they show some drawbacks. For example, only one of the input terminals presents a high impedance level. This can be a problem if differential signals have to be handled. To overcome this problem, fully differential CCII (FD–CCII) was in 2000 [17]. It may be considered as the most versatile building block that can be designed starting from the basic CCII. It is an eight–terminal analog active device which matrix characteristic and block scheme are shown in Fig. 14 (a) and (b), respectively.

$$\begin{pmatrix} V_{xp} \\ V_{xn} \\ I_{zp} \\ I_{zn} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{xp} \\ I_{xn} \\ V_{y1} \\ V_{y2} \\ V_{y3} \\ V_{y4} \end{pmatrix}$$



(a) **(b)**

Fig. 14. FD–CCII (a) matrix characteristic (b) block scheme.

2.3.1 Bulk–driven fully differential current conveyor (BD FD–CCII)

A new LV LP FDCCII using bulk–driven technique is shown in Fig. 15. The differential input stages are consisted of three bulk–driven differential amplifiers M_1–M_2, M_3–M_4 and M_5–M_6. Since the differential input stages are based on the bulk–driven flipped voltage follower, the minimum needed power supply voltage can be expressed by:

$$V_{DD\,(min)} = V_{GS\,(M7,M8,M9)} + V_{DS\,(M10,M11,M12)}. \quad (4)$$

If the voltages V_{GS} of M_1 to M_6 are lower than their threshold voltages, then these transistors will operate in sub–threshold region. Transistors M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28} and M_{29} act as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit. The

power consumption of the circuit can be controlled appropriately by setting I_{bias} and V_{DD}. Transistors M_{10}, M_{11} and M_{12} are common for the differential input stages and they form the active load for them. Transistors M_7, M_8 and M_9 act as tail current sources for the first, second and third differential input stages, respectively. The second stage of three differential input stages is created by cascoding transistors M_{14}–M_{16}, M_{18}–M_{21}, M_{22}–M_{24} and M_{26}–M_{28}. The negative feedback connection between the drain terminals of M_{16}, M_{18} and M_{24}, M_{26} and the input terminals of M_1 and M_6, respectively, is used to achieve the voltage transfers between x and y.

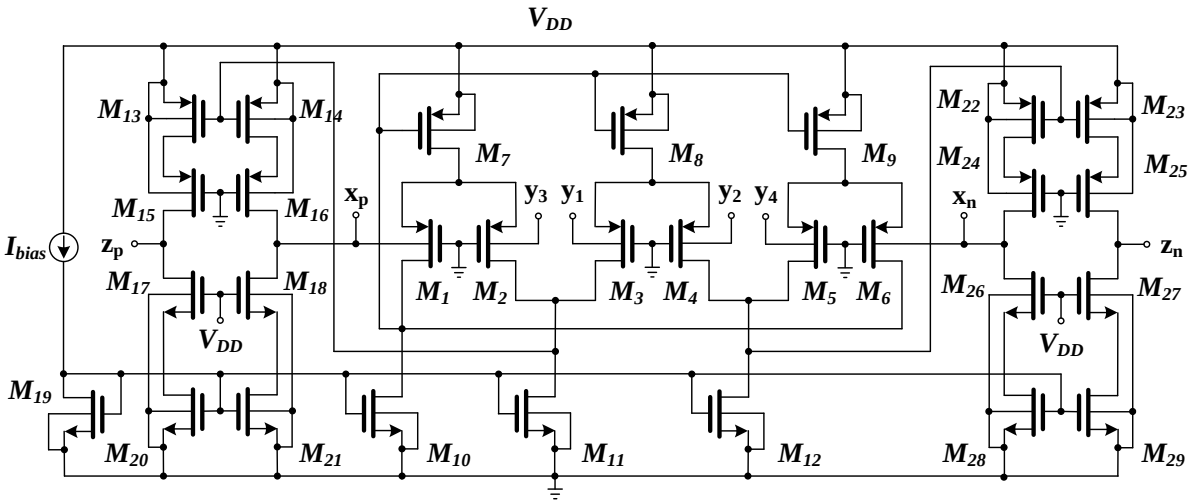


Fig. 15. Proposed BD–FDCCII.

2.3.1.1 BD–FDCCII–based universal filter

In order to confirm that the proposed BD–FDCCII can be used in analog signal processing, the BD–FDCCII–based universal filter as shown in Fig. 16 is an example application. This filter employs one BD–FDCCII, two capacitors and two resistors. Because BD–FDCCII uses single power supply (0.5V), the common–mode voltage (V_{CM}) is needed. The filtering functions can be obtained appropriately connecting the input and the output terminals. As an example, high–pass (HP), low–pass (LP), band–pass (BP) and band–stop (BS) filters can be obtained, respectively, as:

- HPF: $V_{in1}=V_{in}$, $V_{in2}=V_{in3}=V_{CM}$ and $V_{o1}=V_{out}$,
- LPF: $V_{in2}=V_{in}$, $V_{in1}=V_{in3}=V_{CM}$ and $V_{o2}=V_{out}$,
- BPF: $V_{in1}=V_{in}$, $V_{in2}=V_{in3}=V_{CM}$ and $V_{o4}=V_{out}$,
- BSF: $V_{in1}=V_{in3}=V_{in}$, $V_{in2}=V_{CM}$ and $V_{o1}=V_{out}$.

It should be noted that these filtering functions are obtained using only one BD–FDCCII. This is the advantage of this active building block that

provides the arithmetic operation capability of voltage signals and addition/subtraction of current signal.

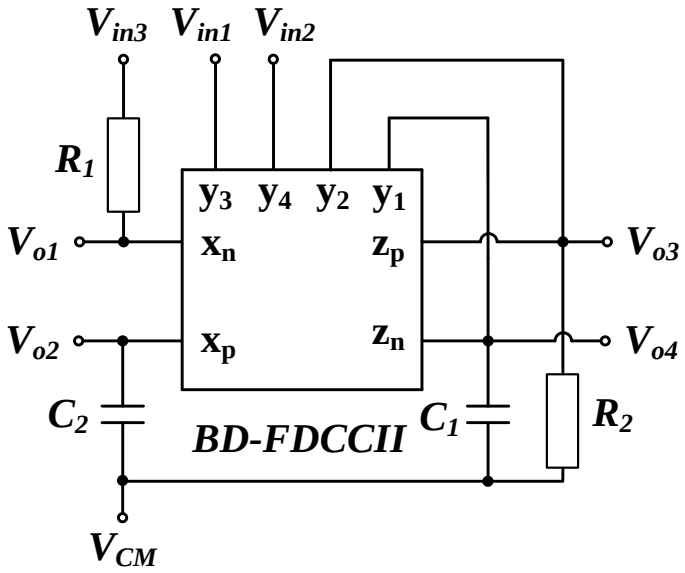


Fig. 16. BD–FDCCII–based universal filter.

2.3.1.2 Simulation results

The proposed BD–FDCCII was simulated by PSpice simulator using the 0.18 μm TSMC CMOS parameters. The transistor aspect ratios of Fig. 15 are listed in Tab. 7. The supply voltage is 0.5 V, while the biasing current I_{bias} was chosen as 2 μA and the common–mode voltage (V_{CM}) is 0.25 V. Fig. 17 shows the DC voltage characteristics of the two terminals X_p and X_n versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. Fig. 18 shows the output currents I_{zp} and I_{zn} versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. In this case, the terminals X_p and X_n were connected to 10 kΩ resistances and the terminals Z_p and Z_n were connected to 50 kΩ resistances.

The simulated results of the proposed BD–FDCCII are also summarized in Tab 8. The filter in Fig. 16 was also simulated using PSpice simulators. The BD–FDCCII as shown in Fig. 15 was used. As an example design, the capacitors $C_1 = C_2 = 50$ pF and the resistors $R_1 = R_2 = 345$ kΩ are given. This setting were chosen to obtain the HPF, LPF, BPF and BSF responses with $f_o = 10$ kHz and $Q = 1$. Fig. 19 shows the simulated input and output noise amplitude responses for BPF with INOISE and ONOISE. The simulated equivalent input noise and total output noise are respectively 22.7 μV/√Hz and 1.42 μV/√Hz for the frequency between 100 Hz to 1 MHz. The simulated results for the HPF, LPF, BPF, and BSF characteristics are shown in Fig. 20.

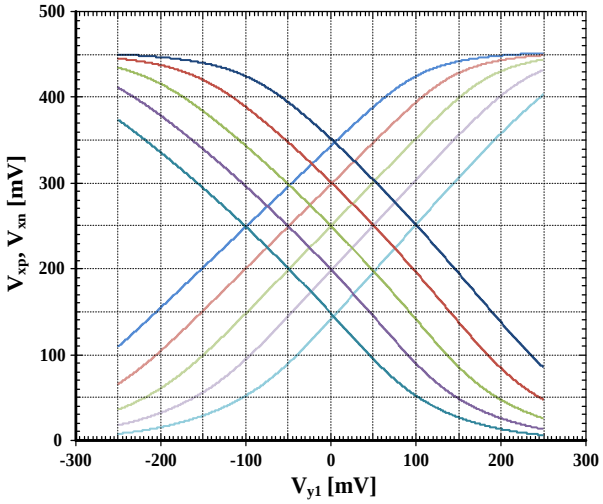


Fig. 17. Simulated V_{xp} and V_{xn} versus V_{y1} for different of V_{y2}.

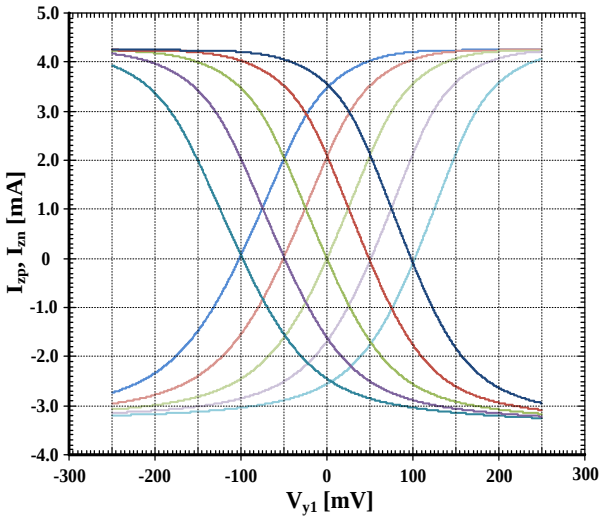


Fig. 18. Simulated I_{zp} and I_{zn} versus V_{y1} when R_{xp}=R_{xn}=10 kΩ.

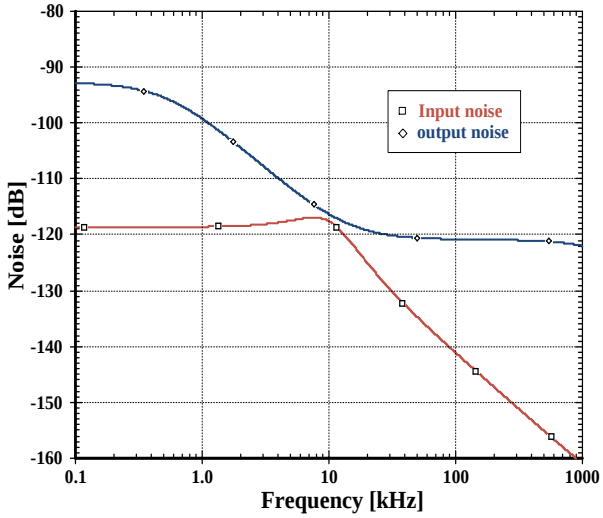


Fig. 19. The equivalence input and output noise against frequency.

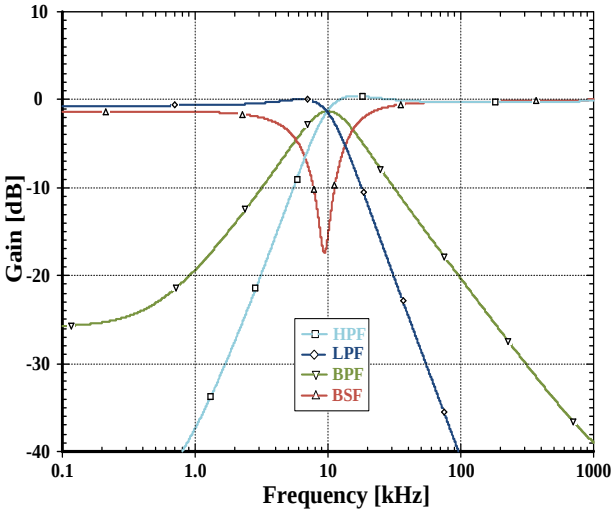


Fig. 20. Simulated HPF, LPF, BPF and BSF responses.

Tab. 7. Transistors aspect ratios for Fig. 15.

MOS transistors	W/L(μm/μm)
M_1–M_6	20/0.3
M_7–M_9	20/0.3
M_{10}–M_{12}, M_{19}	4/0.3
M_{13}, M_{14}, M_{22}, M_{23}	100/0.3
M_{15}, M_{16}, M_{24}, M_{25}	200/4
M_{17}, M_{18}, M_{26}, M_{27}	100/4
M_{20}, M_{21}, M_{28}, M_{29}	16/0.3

Tab. 8. Summarized performances of proposed BD–FDCCII.

Parameters	Value
Technology	0.18 μm
Supply voltage	0.5 V
DC voltage range	–150 mV to 150 mV
DC current range	–4 μA to 4 μA
–3dB bandwidth voltage follower	≤ 8.6 MHz
–3dB bandwidth current follower	≤ 9.6 MHz
R_{yi}, C_{yi} (i = 1, 2, 3, 4)	47 GΩ, 27 fF
R_{xp}, R_{xp} L_{xp}, L_{xn}	10.2 kΩ, 2 mH
R_{zp}, R_{zp} L_{xp}, L_{xn}	4.2 MΩ, 0.25 pH
Power dissipation	13.6 μW

For these results, the power consumption of only 16.1 μW was obtained.

2.3.2 Bulk–driven quasi–floating–gate fully differential current conveyor (BD–QFG FD–CCII)

The proposed BD–QFG FDCCII is shown in Fig. 21. The input stages are consisted of three BD–QFG differential amplifiers M_1–M_2 and M_{b1}–M_{b2}, M_3–M_4 and M_{b3}–M_{b4}, M_5–M_6 and M_{b5}–M_{b6}. Transistors M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5} and M_{b6} are operating in cutoff region to create large resistance value for providing the negative supply voltage to each gate of transistors M_1, M_2, M_3, M_4, M_5 and M_6. For this structure the minimum needed power supply voltage $V_{DD\ (\min)}$ can be expressed by:

$$V_{DD\ (min)} = V_{GS\ (M7,M8,M9)} + V_{DS\ (M10,M11,M12)}. \quad (5)$$

If the voltages V_{GS} of M_1 to M_6 are lower than their threshold voltages, these transistors will be operated as sub–threshold region. Transistors M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28} and M_{29} act as a multiple output current mirror applying the constant current source I_B to each branch of the circuit. The power consumption of the circuit can be controlled appropriately by setting I_{bias} and V_{DD}. Transistors M_{10}, M_{11} and M_{12} are common for the differential input stages and they form the active load for them. Transistors M_7, M_8 and M_9 act as tail current sources for the first, second and third differential input stages, respectively. The second stage of the three differential input stages is created by cascoding transistors M_{14}–M_{16}, M_{18}–M_{21}, M_{22}–M_{24} and M_{26}–M_{28}. Due to the negative feedback connection between the drain terminals of M_{16}, M_{18} and M_{24}, M_{26} and the input terminals of M_1 and M_6, respectively, the voltage transfers between x and y terminals is achieved. The compensation network R_{c1}, C_{c1} and R_{c2}, C_{c2} are used to ensure the stability of the BD–QFG FDCCII.

On the other hands, the cascode transistors M_{13}–M_{15}, M_{17}–M_{20}, M_{23}–M_{25} and M_{27}–M_{29} create the output stage for BD–QFG FDCCII at the outputs and they provide the current copies of x_p and x_n to z_p and z_n terminals, respectively. Also the use of cascode technique makes the proposed BD–QFG FDCCII provide a high resistance value for z terminals and improve the accuracy between z and x currents.

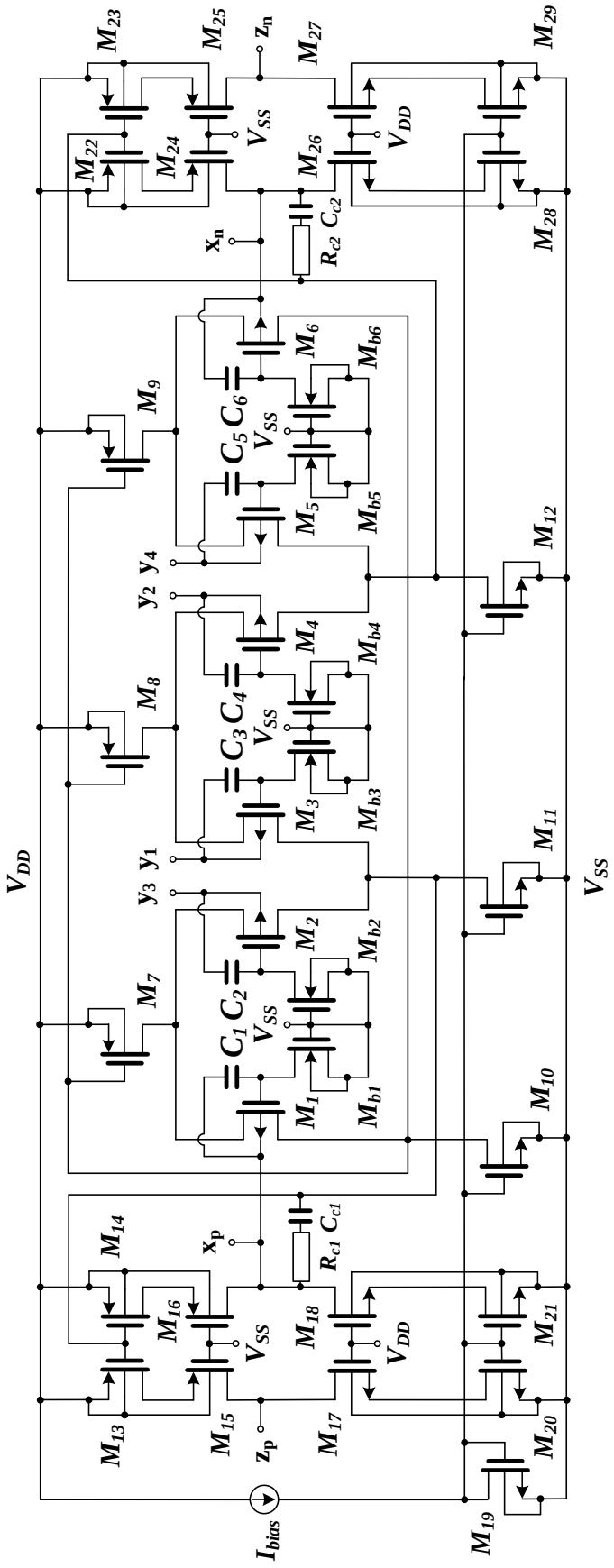


Fig. 21. Proposed BD–QFG–FDCCII.

2.3.2.1 BD–QFG–FDCCII–based universal filter

To confirm that the proposed BD–QFG FDCCII can be used in analog signal processing, the BD–QFG FDCCII–based universal filter as shown in Fig. 22 is an example application. This filter employs three BD–QFG FDCCIIs, two grounded capacitors and four grounded resistors. It should be noted that the input voltage V_{in} of the filter is applied to the y_2 of the first BD–QFG FDCCII. Thus, the filter has the feature of high–input impedance, which is suitable for cascading in voltage–mode operation. The use of all grounded passive components makes the filter particularly attractive for integrated circuit point of view.

High–pass (HPF), band–stop (BSF), band–pass (BPF), low–pass (LPF) and all–pass (APF) voltage responses are obtainable at the node voltage V_{o1}, V_{o2}, V_{o3}, V_{o4} and V_{o5}, respectively. It is to be noted that the output terminals V_{o3} and V_{o4} of Fig. 22 are not in low–output impedances. If low–output impedance terminal is needed, it can be obtained by connecting these terminals to the input $V_{in}^{'}$ and node voltage V_{o6} will become the new low–output impedance terminal. Therefore, the filter is possible for providing the high–input impedance and low–output terminal.

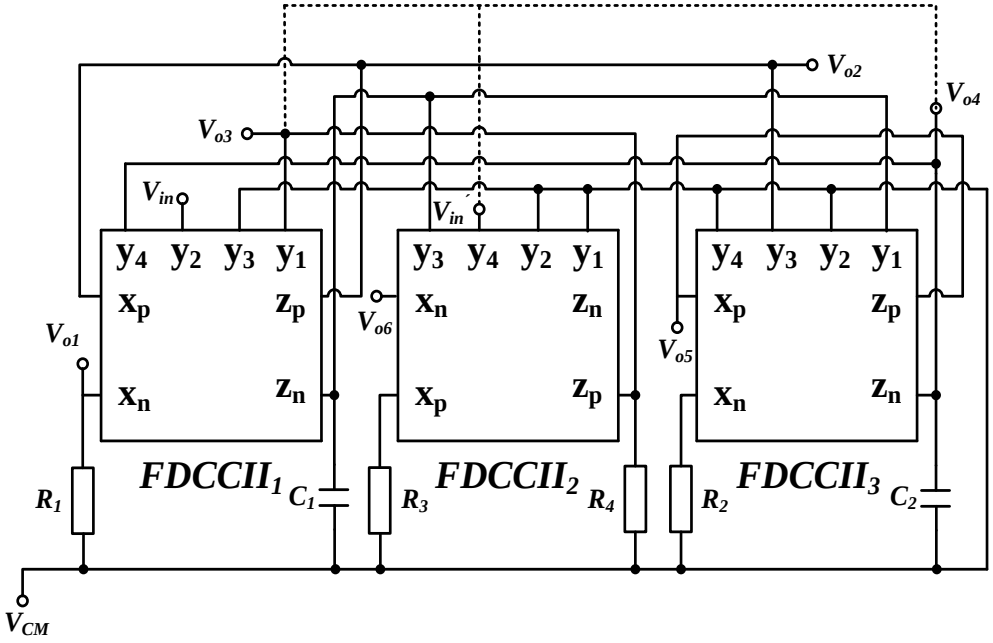


Fig. 22. Universal filter using BD–QFG–FDCCII.

2.3.2.2 Simulation results

The proposed BD–QFG FDCCII was simulated by PSpice simulators using the 0.18 μm TSMC CMOS parameters. The transistor aspect ratios of

Fig. 21 were listed in Tab. 9. The supply voltage and the biasing current I_{bias} were taken respectively as 0.5 V and 2 μA.

Tab. 9. Component values and transistors aspect ratios for Fig. 21.

MOS transistors	W/L(μm/μm)
M_1–M_6	20/0.3
M_{b1}–M_{b6}	8/0.3
M_7–M_9	20/0.3
M_{10}–M_{12}, M_{19}	4/0.3
M_{13}, M_{14}, M_{22}, M_{23}	100/0.3
M_{15}, M_{16}, M_{24}, M_{25}	200/4
M_{17}, M_{18}, M_{26}, M_{27}	100/4
M_{20}, M_{21}, M_{28}, M_{29}	16/0.3
C_1, C_2, C_3, C_4, C_5, C_6, C_{C1}, C_{C2} = 0.1 pF	
R_{C1}, R_{C2} = 3 kΩ	

Tab. 10. Summarized performances of proposed BD–QFG–FDCCII.

Parameters	Value
Technology	0.18 μm
Supply voltage	0.5 V
Common–mode voltage	0.25 V
Power dissipation	16.1 μW
DC voltage range	–100 to 100 mV
DC current range	–4 μA to 4 μA
–3dB bandwidth voltage follower	≤ 8.6 MHz
–3dB bandwidth current follower	≤ 9.6 MHz
R_{yi}, C_{yi} (i = 1, 2, 3, 4)	47 GΩ, 27 fF
R_{xp}, R_{xp} L_{xp}, L_{xn}	10.2 kΩ, 2 mH
R_{zp}, R_{zp} L_{xp}, L_{xn}	4.2 MΩ, 0.25 pH
Input noise (1 kHz)	6.33 μV/√Hz
Dynamic range (THD=1%@1 kHz)	59 dB

Tab. 11. Performance comparison of BD–QFG FDCCII with other FDCCIIs.

Parameters		Proposed FDCCII	Ref. [22]	Ref. [23]	Ref. [24]	Ref. [25]
Technology	[μm]	0.18	1.2	0.18	0.18	0.35
Power supply	[V]	0.5	± 1.5	± 0.8	1	± 1.5
Power consumption	[μW]	16.1	–	3000	403.77	–
Input voltage linear range	[mV]	± 100	± 200	± 300	± 1000	2400
Input current linear range	[μA]	± 4	–	2000	± 1000	± 500
–3dB bandwidth V_X/V_Y	[MHz]	6.8	10	–	25.7	–
–3dB bandwidth I_Z/I_X	[MHz]	9.6	–	> 1000	30	–

The simulated results of the proposed BD–QFG FDCCII were also summarized in Tab. 10. From this table, the values of R_{xp} and R_{xn} of 10.2 kΩ seem to be high; hence the values of R_{xp} and R_{xp} must be taken in account during application design. Tab. 11 shows the comparison of BD–QFG FDCCII–based filter with previously FDCCII–based filters and confirm the attractive features of the proposed structure. The common–mode voltage (V_{CM}) was 0.25 V.

Fig. 23 shows the DC voltage characteristics of the two terminals X_p and X_n versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. Fig. 24 shows the output currents I_{zp} and I_{zn} versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. In this case, the terminals X_p and X_n were connected to 10 kΩ resistance value and the terminals Z_p and Z_n were connected to 50 kΩ resistance values.

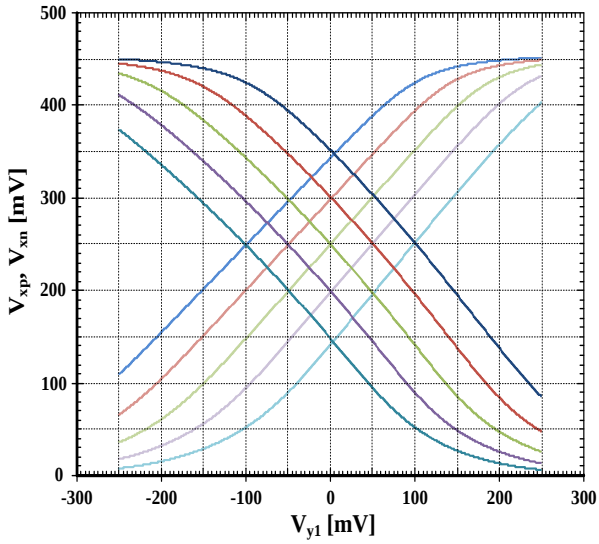


Fig. 23. Simulated V_{xp} and V_{xn} versus V_{y1} for different of V_{y2}.

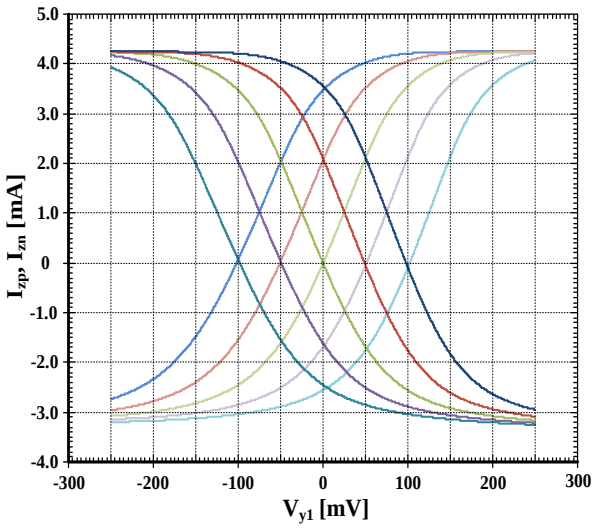


Fig. 24. Simulated I_{zp} and I_{zn} versus V_{y1} when $R_{xp} = R_{xn} = 10$ kΩ.

The filter in Fig. 22 was also simulated using PSpice simulators. The BD–QFG FDCCII as shown in Fig. 21 was used. As an example design, the capacitors $C_1 = C_2 = 50$ pF and the resistors $R_1 = R_2 = R_3 = R_4 = 100$ kΩ are given. This setting has been designed to obtain the HP, BS, BP, LP and AP filter responses with $f_o = 31.8$ kHz and $Q = 1$. The simulated results for the HPF, BSF, BPF, and LPF characteristics were shown in Fig. 25. The characteristic of AP filter was shown in Fig. 26. It is observed from Figs. 25 and 26 that the filter in Fig. 22 performs all the standard biquadratic filtering functions well, which can verify the theoretical analysis. In this case, the natural frequency and the power consumption of 31.6 kHz and 48.3 μW were respectively expressed.

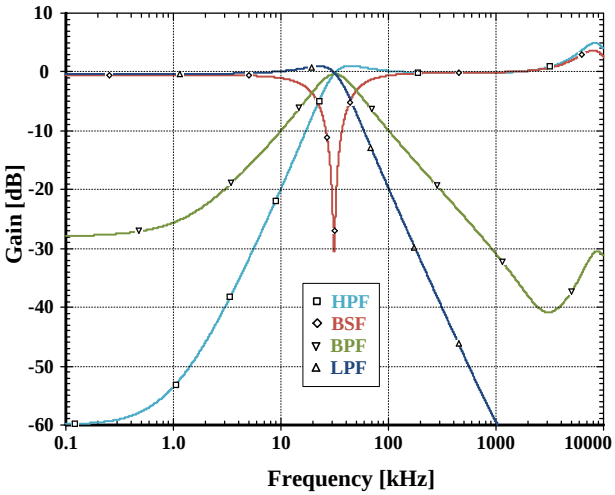


Fig. 25. Simulated HPF, BSF, BPF, and LPF responses.

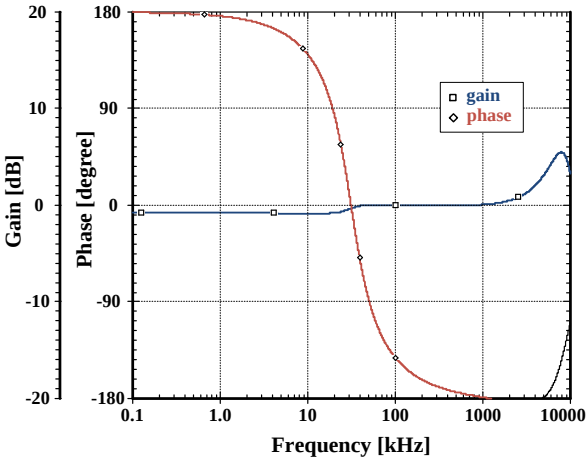
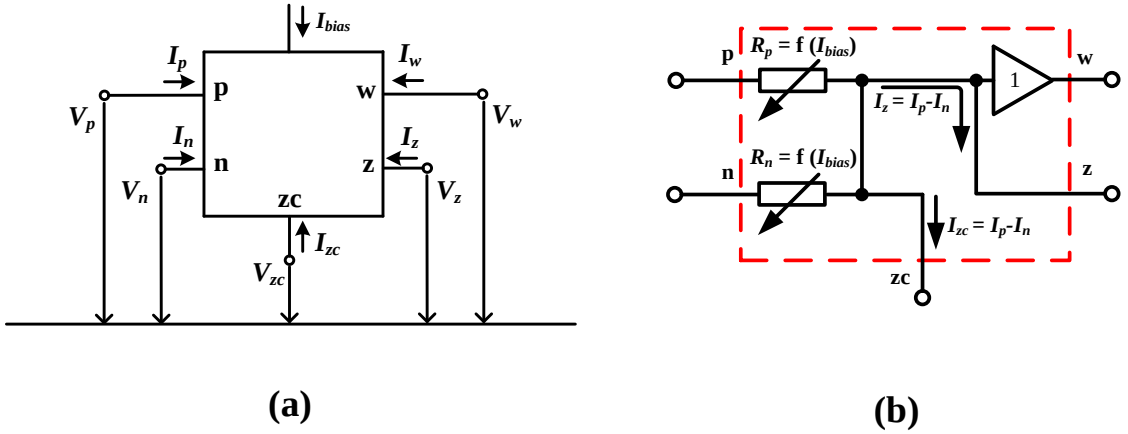


Fig. 26. Simulated gain and phase of APF responses.

2.4. BULK–DRIVEN Z–COPY CURRENT–CONTROLLED CURRENT DIFFERENCING BUFFERED AMPLIFIER (BD ZC CC CDBA)

The ZC–CC–CDBA is a five terminal active element; two low impedance input terminals (p, n), two high impedance output terminals (z, zc), and one low impedance output terminal (w). The schematic symbol of the ZC–CC–CDBA and its equivalent circuit are depicted in Fig .27 (a) and (b), respectively.



(a) **(b)**

Fig. 27. ZC–CC–CDBA: (a) schematic symbol, (b) equivalent circuit.

Unlike the conventional CDBA, here the input voltages V_p and V_n are not equal to zero. Instead they have finite parasitic input resistances R_p and R_n, respectively. The input/ output behavior of the ZC–CC–CDBA circuit can be described by the following matrix:

$$\begin{pmatrix} V_p \\ V_n \\ I_z, I_{zc} \\ V_w \end{pmatrix} = \begin{pmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_p \\ I_n \\ V_z \\ I_w \end{pmatrix}. \tag{6}$$

The MOS internal structure of the proposed ZC–CC–CDBA is depicted in Fig. 28. Transistors M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, and M_{b6} represent multiple output current mirror providing the constant bias current I_{bias} to the circuit branches. The current differencing unit (CDU) is the cascade of two BD current followers M_1–M_4 and M_5–M_8. Each current follower is constructed from the flipped voltage follower current sensor structure (BD–FVFCS) with enhanced BD current mirror. The transistors M_4 and M_8 represent simple voltage source. The current I_B through these transistors is extremely small in comparison with the bias current I_{bias} to avoid extra undesired offset. The transistors M_9, M_{10} mirror the output current of the first current follower ($I_n + I_{bias}$) to be subtracted from the output current of the second current follower ($I_p + I_{bias}$). The resulting current ($I_p - I_n$) is lead away from z terminal. Transistors M_{11} and M_{12} provide a current copy of z terminal to zc terminal. The voltage follower (VF) consists of BD differential input stage M_{13}, M_{14}. Transistor M_{15} acts as a tail transistor of the differential input stage. Transistors M_{b6} and M_{16} represent the second stage of the VF. Transistors M_{b4} and M_{b5} act as active loads. Transistors M_{13}–M_{15} construct BD flipped voltage follower differential structure (BD–DFVF).

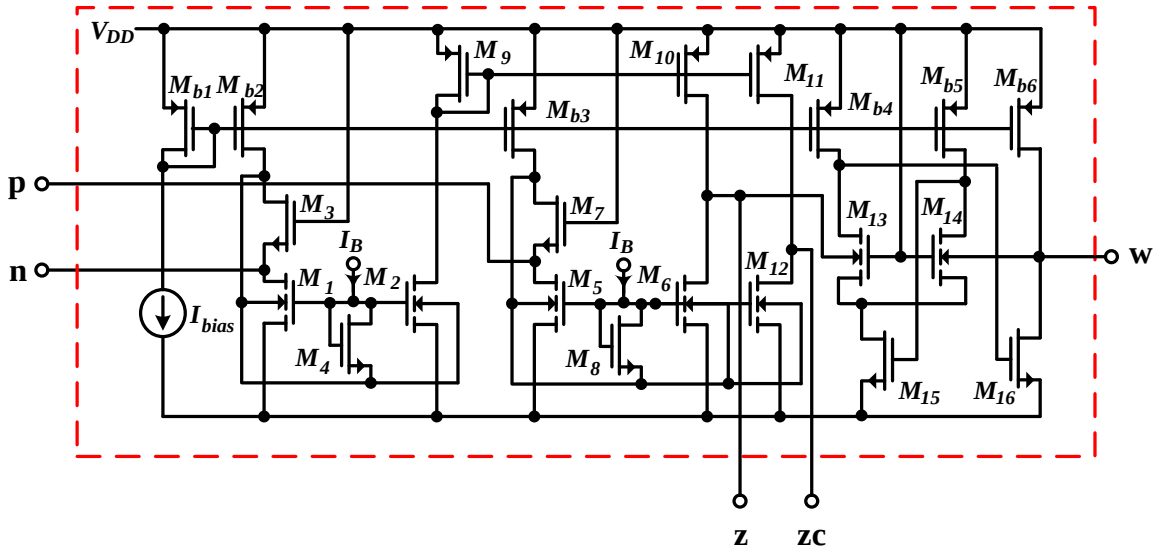


Fig. 28. The proposed MOS structure of the ZC–CC–CDBA.

Owing to use the BD flipped voltage follower structure in the proposed circuit, the minimum power supply voltage $V_{DD\,(min)}$ is given by:

$$V_{DD\,(min)} = V_{GS} + V_{DSat} \tag{7}$$

As it is obvious from (7), the proposed circuit is capable to operate under ULV conditions.

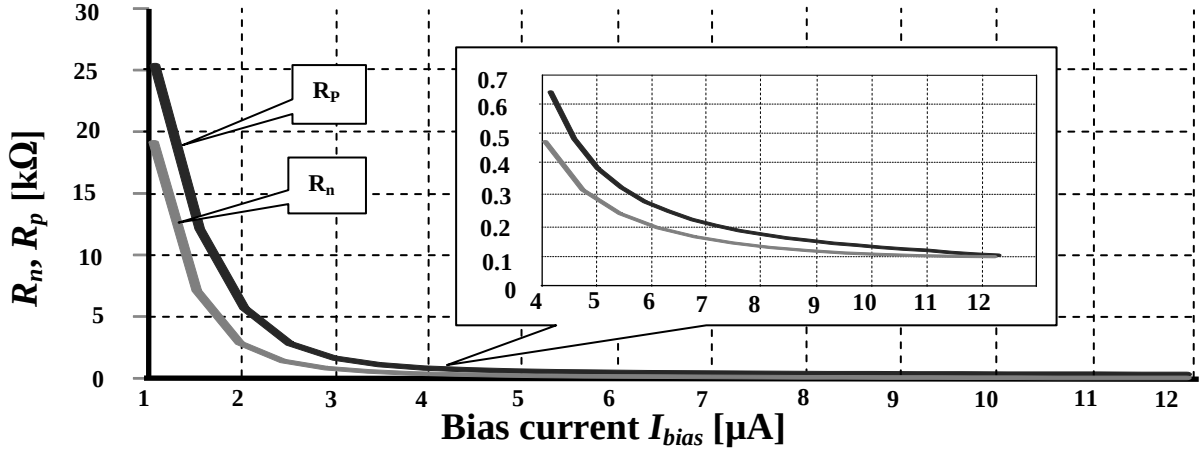


Fig. 29. Parasitic resistances R_p and R_n versus the bias current I_{bias}.

Moreover, the parasitic input resistances R_p, R_n can be adjusted via the bias current I_{bias} as it is shown in Fig. 29. Hence designers started to utilize these resistances instead of the passive resistors in several applications.

2.4.1 BD–ZC–CC–CDBA–based universal filter

A current mode universal filter based on ZC–CC–CDBA is introduced in this section to confirm the functionality of the proposed circuit. The multi–function current mode filter is depicted in Fig. 30.

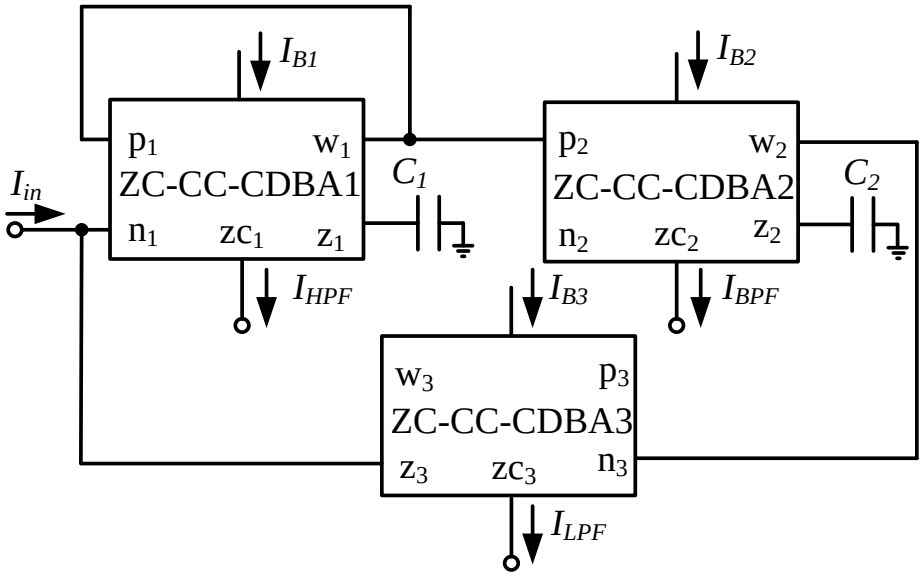


Fig. 30. Current mode biquad filter based on ZC–CC–CDBA.

This filter performs three functions simultaneously: low pass, high pass, and band pass with high output impedance property. The parasitic resistances (R_{p1}, R_{n1}) of the ZC–CC–CDBA$_1$, (R_{p2}, R_{n2}) of the ZC–CC–CDBA$_2$, and (R_{p3}, R_{n3}) of the ZC–CC–CDBA$_3$ can be tuned via bias currents: I_{B1}, I_{B2}, and I_{B3}, respectively. The output currents I_{HPF}, I_{BPF} and I_{LPF} of this filter are flowing out the zc$_1$, zc$_2$ and zc$_3$ terminals, respectively. These currents are flowing into the working impedances directly.

2.4.2 Simulation results

The performances of the proposed ZC–CC–CDBA shown in Fig. 28 were simulated using PSpice simulator. The circuit was simulated using the 0.18 µm TSMC CMOS parameters [14].

All the simulations were performed for I_{bias}= 3 µA, I_B = 4 nA with an extremely low voltage supply of 0.65 V. The DC curves $I_{z,zc}$ versus I_n and I_p are depicted in Fig. 31. Thanks to utilizing enhanced BD current mirror, the proposed circuit offers high linearity of I_z versus I_n and I_p with extremely low current offset whose value is less than 0.05 µA. The DC curves I_z versus I_p for various values of I_n are shown in Fig. 32, whereas the current I_n vary from –3 µA to 3 µA with a step of 1 µA

The DC curve V_w versus V_z is shown in Fig. 33. Besides, the voltage error is depicted. The high linearity and the wide range operation can be observed. Furthermore, in the range from 0.04 V to 0.58 V, the voltage error is less than 1 mV. The frequency response of the voltage gain V_w/V_z is clarified in Fig. 34. The AC simulation is performed using capacitive load of 1pF. The cutoff frequency is 11.18 MHz with unity gain at low frequencies. The frequency response of the parasitic impedance of w terminal is depicted in Fig. 35. The value of this impedance at low frequencies is 1 kΩ.

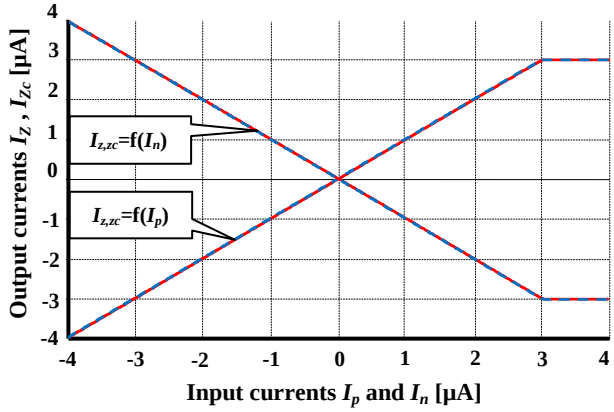


Fig. 31. DC curves I_z, I_{zc} versus I_p and I_n.

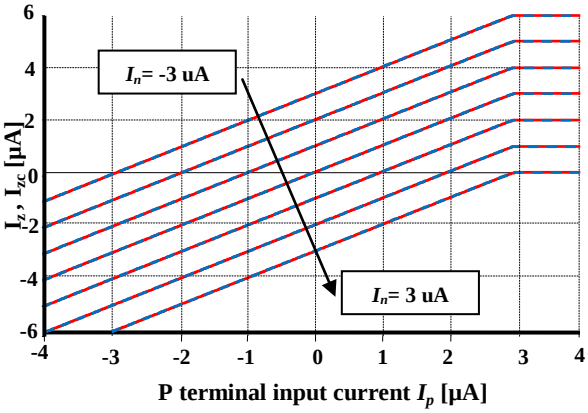


Fig. 32. DC curves I_z, I_{zc} versus I_p for various values of I_n.

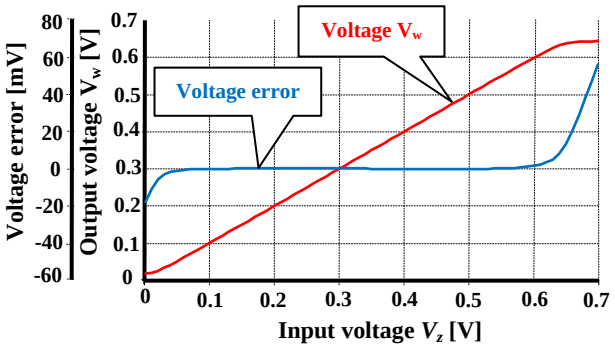


Fig. 33. DC curves V_w versus V_z and the voltage error.

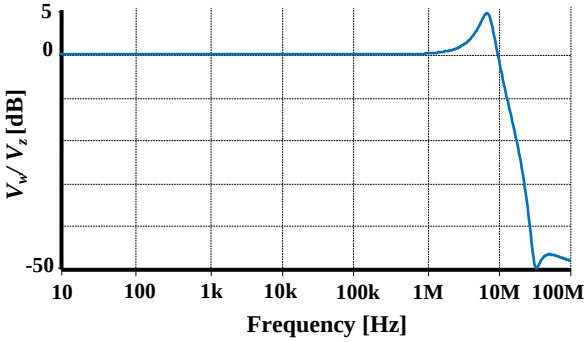


Fig. 34. AC curve of the voltage gain V_W/V_Z.

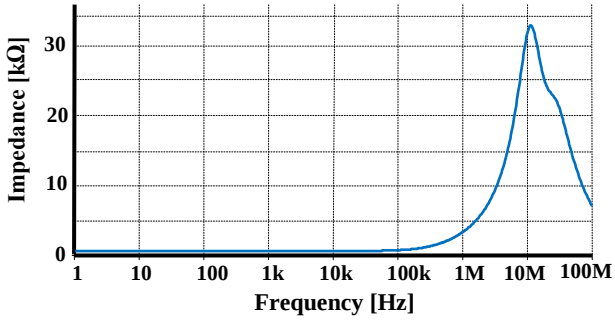


Fig. 35. Frequency dependence of the parasitic impedance of w terminal.

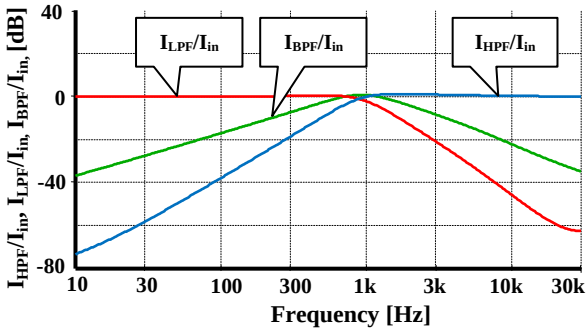


Fig. 36. Frequency response of the proposed filter.

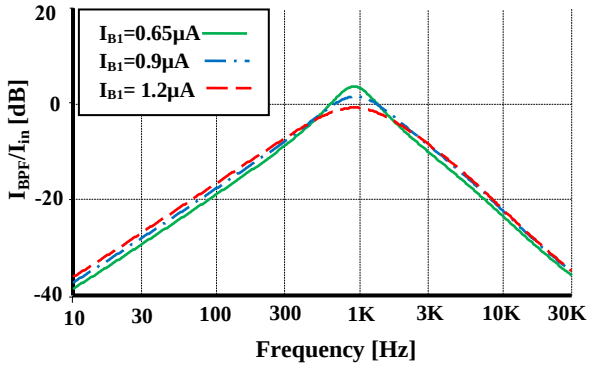


Fig. 37. The response of the band pass filter for different I_{B1} values.

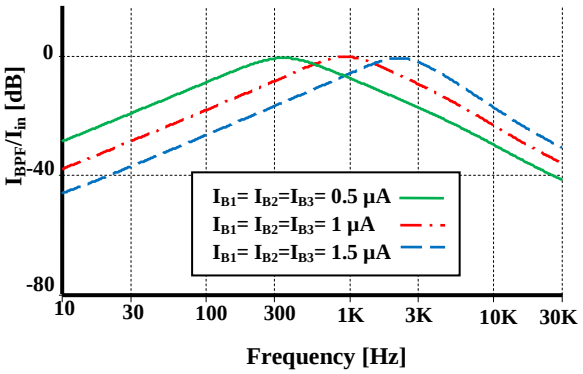


Fig. 38. The response of the band pass filter for different values of I_{B1}, I_{B2} and I_{B3}.

The optimal transistors aspect ratios of the proposed circuit are listed in Tab. 12. The most important features of the proposed ZC–CC–CDBA are listed in Tab. 13.

The simulation results of the multi–function current mode biquad filter shown in Fig. 30 are depicted in Fig. 36, Fig. 37 and Fig. 38. The three ZC–CC–CDBAs are biased by I_{B1} = I_{B2} = I_{B3} = 1 μA. The components of the filter are C_1 = 5 nF and C_2 = 10 nF. That yields the pole frequency of 950 Hz, while the calculated pole frequency is 1 kHz. Thus the deviation is 5.2%. This error comes from the non–ideal parasitic properties of the ZC–CC–CDBA. The frequency responses of the current gains of the filter shown in Fig. 30 are presented in Fig. 36 for R_{load}=1 Ω. It is obvious that this filter can provide low

pass, band pass and high pass functions simultaneously, without any change in the circuit topology. The band pass gain responses for various values of I_{B1} are depicted in Fig. 37. Moreover, Fig. 38 depicts the band pass filter gain responses for ($I_{B1} = I_{B2} = I_{B3} = 0.5$ µA, 1 µA and 1.5 µA).

Tab. 12. The transistors aspect ratios of the circuit shown in Fig. 28.

Transistor	**W/L [µm/µm]**
M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, M_{b6}	15/1.5
M_9, M_{10}, M_{11}	80/3
M_3	3/0.3
M_7	8/0.3
M_1, M_2	40/2
M_5, M_6, M_{12}	40/3
M_4, M_8	80/1
M_{15}	20/3
M_{13}, M_{14}	30/3
M_{16}	15/3

Tab. 13. The most important characteristics of the circuit in Fig 28.

Parameter	**Value**
Voltage supply, bias current	0.65 V, 3 µA
Power consumption for I_{bias}=3 µA	17 µW
3 dB bandwidth of $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	5.15 MHz, 2.4 MHz
Current offset	<50 nA
Current gains $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	1.1
3 dB bandwidth of V_w/V_z	11.18 MHz
Voltage gain V_w/V_z	1
Voltage offset	<1 mV
Resistance of terminal z	2.67 MΩ
Resistance of terminal w	1 kΩ

3. CONCLUSION

The recent trend towards miniaturized circuits and portability of electronic equipment has given a strong and decisive boost towards the design of low–voltage low–power (LV LP) analog circuits. The difficulty of low voltage design consists of maintaining the most important characteristics of circuit's performance without altering it. Generally, characteristics such as the linearity, the gain, the input common mode range, the dynamic range, rail–to–rail operation, and other features have to be implemented to maximum in order for circuit to be applicable and in such way desirable.

Circuits along with application examples are presented to demonstrate their functionality as designed using LV LP techniques. Circuits include Operational Transconductance Amplifier (OTA), Voltage Differencing Transconductance Amplifier (VDTA), Fully Differential Current Conveyor (FD CCII) and Current Controlled Current Differencing Buffered Amplifier (CC CDBA). Whereas application examples include diode–less precision rectifier, inductance simulation, as well as low–pass, band–pass and universal filters.

However, each low–voltage low–power technique has its advantages and disadvantages. The short version of doctoral thesis focused on designing LV LP circuits depending on both: LV LP techniques and LV LP building blocks. By following this strategy, the voltage supply was reduced down to approximately 0.5–0.6 V and the power consumption was reduced down to less than 20 μW almost in all circuits. Moreover, all circuits were stable, had rail–to–rail operation, and were very suitable for low–frequency applications such as biomedical applications. It is noteworthy that almost all parts of this short version of thesis were already published in many international journals. Please refer to my Curriculum Vitae for further information.

The main goal of this short version of doctoral thesis was to design and simulate novel CMOS structures of basic building blocks and active elements so they can operate at very low power supply voltage levels (average of 0.6 V) and consume very low power (average of 20 μW) for 0.18 μm CMOS technology, extending common–mode dynamic range while preserving other characteristics acceptable for many applications. With respect to above mentioned discussions it is declared that aims of this thesis were fulfilled.

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4. CURRICULUM VITAE

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Personal Details

Date of Birth	13 May 1984
Nationality	Syrian
Marital status	Single

Language skills

Arabic	Mother tongue
English	Excellent knowledge of speaking, reading and writing
Czech	Good knowledge of speaking and reading
German	Basic knowledge of speaking and reading

Objectives

To secure a challenging **position in the field of telecommunications or analog circuits design within** a **progressive reputable organization**, which facilitates professional growth and utilization of my qualification and experience, while embracing new methodologies & strategies to remain competitive in the market

Education

2011 - now	Brno University of Technology, Faculty of Electrical Engineering and Communication, Czech Republic, doctoral degree in Microelectronics
	Successfully passed the 2nd year doctoral state exam
2003–2010	Al-Baath University, Faculty of Electrical and Mechanical Engineering, Department of Electrical and

Communication Engineering, Syria, diploma degree in Electronic & Communication Engineering

Nostrificated as an engineering degree by Brno University of Technology

Professional Training Courses

- CBT Nuggets Cisco CCNA Training
- CBT Nuggets Cisco CCNP BSCI
- CBT Nuggets Microsoft MCSE
- MTN Syria special training course including Network Planning and Management, Maintenance and Configuring Devices
- Several courses in English language

Undergraduate and postgraduate projects

4th year project	Design and implementation of AM radio receiver
5th year project	High–range laser digital transmitter of audio signals with encryption and signalisation of interception
Ph.D. thesis	Low voltage low power analog circuits design

Technical skills

Mobile networks	Cellular communication systems (2G, 2.5G, 3G, 3.5G, 4G) and specially GSM & UMTS as well as MSS (Mobile Satellite Services)
Switches	Addressing, trunk, VLANs, VTP and subbnetting. Experience with Cisco Catalyst Series Switches 2950 and 1900
Security	IP access lists (standard and extended)
Routers	Experience with Cisco 1700 and 2600 Series Routers
Routing protocols	Static routing, RIP (v1, v2), IGRP, EIGRP, OSPF, ISIS, BGP and in WANs: frame relay, ISDN. Beside PPP & Chap, telnet, Nat and PAT

Circuit design	Excellent knowledge in analog circuits design, especially low-voltage low–power circuits

Software skills

Circuits design and simulation	PSpice, Eagle, Cadence Virtuoso, Cadence Spectre, Orcad, Workbench/Multisim, Micro-Cap, SNAP
Programming and scripting languages	Turbo Pascal, C/C++, Matlab/Simulink, Assembler

Research and teaching experience

Since 2011	Teaching assistant at Brno University of Technology, Department of Microelectronics. Taught courses: *Analogue electronic circuits* (practicals), *Modelling and Computer Simulation* (practicals)
Published papers in international journals	-ALSIBAI, Z. Floating- Gate Operational Transconductance Amplifier. *International Journal of Information and Electronics Engineering*, 2013, vol. 2013 (3), no. 4, p. 361-364. ISSN: 2010– 3719 -ALSIBAI, Z. Floating- Gate MOSFET Based Tunable Voltage Differencing Transconductance Amplifier and Its Application to Biquad Filters. *International Journal of Engineering Sciences and Research Technology*, 2013, vol. 2013 (2), no. 4, p. 772–777. ISSN: 2277–9655 -B. A. DABBOUS, S and ALSIBAI, Z. Ultra-Low Voltage Low Power Bulk Driven Z Copy-Current Controlled–Current Differencing Buffered Amplifier. *International Journal of Electronics and Electrical Engineering*, 2014, vol. 2014 (2), no. 3, p. 229-234. ISSN: 2301–380X

Hobbies

Playing piano, listening to music, watching and playing sports, writing poetry and reading

ABSTRACT

The dissertation thesis is aiming at examining the most common methods adopted by analog circuits' designers in order to achieve low voltage (LV) low power (LP) configurations. The capability of LV LP operation could be achieved either by developed technologies or by design techniques. The thesis is concentrating upon design techniques, especially the non–conventional ones which are bulk–driven (BD), floating–gate (FG), quasi–floating–gate (QFG), bulk–driven floating–gate (BD–FG) and bulk–driven quasi–floating–gate (BD–QFG) techniques. The thesis also looks at ways of implementing structures of well–known and modern active elements operating in voltage–, current–, and mixed–mode such as operational transconductance amplifier (OTA), second generation current conveyor (CCII), fully–differential second generation current conveyor (FB–CCII), fully–balanced differential difference amplifier (FB–DDA), voltage differencing transconductance amplifier (VDTA), current–controlled current differencing buffered amplifier (CC–CDBA) and current feedback operational amplifier (CFOA). In order to confirm the functionality and behavior of these configurations and elements, they have been utilized in application examples such as diode–less rectifier and inductance simulations, as well as low–pass, band–pass and universal filters. All active elements and application examples have been verified by PSpice simulator using the 0.18 µm TSMC CMOS parameters. Sufficient numbers of simulated plots are included in this thesis to illustrate the precise and strong behavior of structures.