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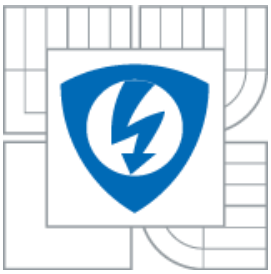

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NÁVRH ANALOGOVÝCH OBVODŮ S NÍZKÝM NAPÁJECÍM NAPĚTÍM A NÍZKÝM PŘÍKONEM.

LOW VOLTAGE LOW POWER ANALOGUE CIRCUITS DESIGN.

DIZERTAČNÍ PRÁCE
DOCTORAL THESIS

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ABSTRACT

The dissertation thesis is aiming at examining the most common methods adopted by analog circuits' designers in order to achieve low voltage (LV) low power (LP) configurations. The capability of LV LP operation could be achieved either by developed technologies or by design techniques. The thesis is concentrating upon design techniques, especially the non–conventional ones which are bulk–driven (BD), floating–gate (FG), quasi–floating–gate (QFG), bulk–driven floating–gate (BD–FG) and bulk–driven quasi–floating–gate (BD–QFG) techniques. The thesis also looks at ways of implementing structures of well–known and modern active elements operating in voltage–, current–, and mixed–mode such as operational transconductance amplifier (OTA), second generation current conveyor (CCII), fully–differential second generation current conveyor (FB–CCII), fully–balanced differential difference amplifier (FB–DDA), voltage differencing transconductance amplifier (VDTA), current–controlled current differencing buffered amplifier (CC–CDBA) and current feedback operational amplifier (CFOA). In order to confirm the functionality and behavior of these configurations and elements, they have been utilized in application examples such as diode–less rectifier and inductance simulations, as well as low–pass, band–pass and universal filters. All active elements and application examples have been verified by PSpice simulator using the 0.18 µm TSMC CMOS parameters. Sufficient numbers of simulated plots are included in this thesis to illustrate the precise and strong behavior of structures.

KEYWORDS

Low voltage, low power, analog circuit design, bulk–driven transistor, floating–gate transistor, quasi–floating–gate transistor, active filter, active element.

ABSTRAKT

Disertační práce je zaměřena na výzkum nejběžnějších metod, které se využívají při návrhu analogových obvodů s využití nízkonapěťových (LV) a nízkopříkonových (LP) struktur. Tyto LV LP obvody mohou být vytvořeny díky vyspělým technologiím nebo také využitím pokročilých technik návrhu. Disertační práce se zabývá právě pokročilými technikami návrhu, především pak nekonvenčními. Mezi tyto techniky patří využití prvků s řízeným substrátem (bulk-driven - BD), s plovoucím hradlem (floating-gate - FG), s kvazi plovoucím hradlem (quasi-floating-gate - QFG), s řízeným substrátem s plovoucím hradlem (bulk-driven floating-gate - BD-FG) a s řízeným substrátem s kvazi plovoucím hradlem (quasi-floating-gate - BD-QFG). Práce je také orientována na možné způsoby implementace známých a moderních aktivních prvků pracujících v napěťovém, proudovém nebo mix-módu. Mezi tyto prvky lze začlenit zesilovače typu OTA (operational transconductance amplifier), CCII (second generation current conveyor), FB-CCII (fully-differential second generation current conveyor), FB-DDA (fully-balanced differential difference amplifier), VDTA (voltage differencing transconductance amplifier), CC-CDBA (current-controlled current differencing buffered amplifier) a CFOA (current feedback operational amplifier). Za účelem potvrzení funkčnosti a chování výše zmíněných struktur a prvků byly vytvořeny příklady aplikací, které simulují usměrňovací a induktanční vlastnosti diody, dále pak filtry dolní propusti, pásmové propusti a také univerzální filtry. Všechny aktivní prvky a příklady aplikací byly ověřeny pomocí PSpice simulací s využitím parametrů technologie 0,18 μm TSMC CMOS. Pro ilustraci přesného a účinného chování struktur je v disertační práci zahrnuto velké množství simulačních výsledků.

KLÍČOVÁ SLOVA

Nízké napětí, nízký příkon, návrh analogových obvodů, tranzistor řízený substrátem, tranzistor s plovoucím hradlem, tranzistor s kvazi plovoucím hradlem, aktivní filtry, aktivní prvky.

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DECLARATION

I declare that I have elaborated my doctoral thesis on the theme of "*Low Voltage Low Power Analogue Circuits Design*" independently, under the supervision of the doctoral thesis supervisor and with the use of technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

Brno . . . . . ……..

(Author's signature)

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I would like to express my gratitude to my supervisor, Doc. Ing. et Ing. Fabian Khateb, Ph.D. et Ph.D. who has provided me with guidelines for my work and has supported me with valuable advices through my studies.

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LIST OF ABBREVIATIONS

AC	Alternating Current
APF	All Pass Filter
AVR	Average Value Ratio
A/D	Analog to Digital
BD	Bulk Driven
BD FG	Bulk Driven Floating Gate
BD QFG	Bulk Driven Quasi Floating Gate
BJT	Bipolar Junction Transistor
BOX	Buried OXide
BPF	Band Pass Filter
BSF	Band Stop Filter
CC	Current Conveyor
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
CCCII	Current Controlled Current Conveyor
CCCDBA	Current Controlled Current Differencing Buffered Amplifier
CCTA	Current Conveyor Transconductance Amplifier
CDU	Current Differencing Unit
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CDVB	Current Differencing Voltage Buffer
CE	Characteristic Equation
CF	Current Follower
CFA	Current Feedback Amplifier
CFOA	Current Feedback Operational Amplifier
CGCCII	Current Gain Current Conveyor
CMRR	Common Mode Rejection Ratio
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
D/A	Digital to Analog
DC	Direct Current
DCCII	Differential CCII

DCVC	Differential Current Voltage Conveyor
DDA	Differential Difference Amplifier
DDCC	Differential Difference Current Conveyor
DOTA	Dual Output OTA
DOCCII	Dual Output CCII
DVCCII	Differential Voltage CCII
DVCCS	Differential Voltage Controlled Current Source
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FDCCII	Fully Differential Second Generation Current Conveyor
FG	Floating Gate
FN	Fowler–Nordheim
GB	Gain Bandwidth
GD	Gate Driven
HPF	High Pass Filter
IC	Integrated Circuit
KHN	Kerwin–Huelsman–Newcomb
LP	Low Power
LPF	Low Pass Filter
LV	Low Voltage
MIFG	Multi Input Floating Gate
MOOTA	Multiple Output Operational Transconductance Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOST	MOSFET Transistor
OC	Oscillation Condition
OF	Oscillation Frequency
OPA	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTA–C	Operational Transconductance Amplifier–Capacitor
QFG	Quasi Floating Gate
QO	Quadrature Oscillator
RMS	Root Mean Square
RMSE	Root Mean Square Error
SIMO	Single Input Multiple Output
SNR	Signal to Noise Ratio

SOC	System on Chip
SOI	Silicon On Insulator
PSpice	Simulation Program with Integrated Circuit Emphasis
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company
UCC	Universal Current Conveyor
UV	Ultra Violet
VB	Voltage Buffer
VC	Voltage Conveyor
VCCS	Voltage Controlled Current Source
VDTA	Voltage Differencing Transconductance Amplifier
VF	Voltage Follower
VLSI	Very large scale integration
VM	Voltage Mode
ZC	Z-Copy

LIST OF SYMBOLS

C	capacitor
C_{BC}	total bulk channel capacitance
C_{bd}	bulk to drain parasitic capacitance
C_{bs}	bulk to source parasitic capacitance
C_{bsub}	bulk to substrate parasitic capacitance
C_{GC}	total gate channel capacitance
C_{gd}	gate to drain parasitic capacitance
C_{gs}	gate to source parasitic capacitance
C_j	zero bias junction capacitance
C_{load}	load capacitor
C_{OX}	gate oxide capacitance per unit area
D	denominator of transfer function
ΔV_T	mismatch between the threshold voltages of PMOST and NMOST
$\mathcal{E}_{OX}$	dielectric permittivity
$\mathcal{E}_{si}$	permittivity of silicon
ϕ_F	surface potential
f	frequency
f_c	cut off frequency
f_T	transition frequency
$f_{T,b}$	transition frequency of BD MOST
$f_{T,FG}$	transition frequency of FG MOST
$f_{T,QFG}$	transition frequency of QFG MOST
η	slope factor
φ	phase
γ	bulk–threshold parameter
$g_{ds,eff}$	effective output conductance of FG MOST/QFG MOST
G	conductance
GBW	gain bandwidth product
g_m	transconductance
$g_{m,b}$	bulk transconductance
$g_{m,\,eff}$	effective transconductance
$g_{m,FG}$	floating gate transconductance

$g_{m,QFG}$	quasi floating gate transconductance
I_{bias}	bias current of the transconductance
I_{DSsat}	drain source current in saturation
I_{D0}	process dependent parameter
$I_{Leakage}$	sub–threshold leakage current
K	transconductance parameter
μ_0	free electron mobility in the channel
L	inductor
λ	channel length modulation coefficient
ω_0	pole frequency
P_{avg}	average power
$P_{dynamic}$	dynamic power
P_{static}	static power
Q	quality factor
q	charge of an electron
Q_{FG}	residual charge trapped at the FG during the fabrication process
R	resistor
R_{large}	large value resistor
R_{leak}	leakage resistance
r_o	output resistance
$s=j\omega$	complex parameter – Laplace operator
t_{OX}	oxide thickness
t_{si}	thickness of the depletion layer between the channel and the bulk
V	terminal voltage of an active element
V_{BS}	bulk to source voltage
V_{DD}, V_{SS}	supply voltages of CMOS structure
V_{DS}	drain to source voltage
V_{FG}	voltage at FG in FG MOST
V_{GS}	gate to source voltage
v^2_{noise}	input referred noise power spectral density
V_{QFG}	voltage at FG in QFG MOST
V_T	threshold voltage
V_{ther}	thermal voltage
W/L	CMOS transistor dimensions

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1. INTRODUCTION

In the last decade, with the continuous scaling in the feature size of the transistors, nominal supply voltage of CMOS integrated circuits has been dramatically decreased due to the strongly emerging consumer market for portable devices that needed to be light weighted and hence operate for a long period of time with a small battery. When a MOS transistor size is scaled down, the thickness of the gate oxide is reduced. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from a breakdown due to higher electrical field across the gate oxide, and to ensure its reliability, the supply voltage needs to be reduced [1–5]. Therefore, low–voltage (LV) low–power (LP) analog circuits have received significant attention and have become increasingly important in the electronic industry. Recent advances in LV LP circuit design made it possible to conceive electronic systems that could be worn by people, monitor physiological parameters, and even provide some kind of treatment [6]. The primary application targets of these circuits are low power Systems–on–Chips (SOCs). That covers markets such as: Mobile Internet Services (Smartphones, Tablets, Netbooks), Cellular Telecom, Home and Mobile Multimedia, etc. SOCs are circuits composed of analog and digital components co–existing on a single chip. The idea of SOC came up originally from universal fact that the outside world is mostly analog in nature and that the bandwidth of a signal can become a magnitude higher if the signal is processed in analog circuits. Thus, it became inevitable to introduce analog signal processing. However, when switched to low supply voltage, digital circuits do not suffer lower performance, but the circuit performances of analog circuits, such as gain, dynamic range, speed, bandwidth, linearity, etc. are strongly affected by reduced supply voltage [7]. In addition, chip area reduces the cost of advanced multi–function SOC design. Moreover, LP SOCs need to combine demanding dynamic performance with low power consumption. Therefore, there is urgent need to develop new design techniques for analog circuits at 1–V supply which consume levels of power in the nanowatt range. However, the advances in VLSI technology, circuit design, and product market are actually interrelated. In the past decade, CMOS technology has played a major role in the rapid advancement and the increased integration of VLSI systems. CMOS devices feature high input impedance, extremely low offset switches, high packing density, low switching power consumption, and thus can be easily scaled. The minimum feature size of a MOS transistor has been scaled down to around 90 nm. Consequently, more circuit components in a single chip can then be integrated, so the circuit area and thus its cost will be reduced. In addition, smaller geometry usually lowers the parasitic capacitance, which leads to higher operating speed.

However, system portability usually requires battery supply and therefore weight/energy storage considerations. For the time being, battery technologies do not proportionally evolve with the speed of the applications demand. Therefore the challenge is to

reduce the power consumption of the circuits. In any case, average power, P_{avg}, consumed by these circuit, consists of the sum of two components, static and dynamic power:

$$P_{avg} = P_{static} + P_{dynamic} = V_{DD}\, I_{leakage} + C V_{DD}^2\, f\ , \tag{1.1}$$

where V_{DD} is power supply voltage, $I_{leakage}$ is sub–threshold leakage current of MOS transistor, C represents the total capacitance of a system, and f denotes the frequency at which a circuit operates. Among the most important factors of CMOS VLSI processes is the threshold voltage of the MOS devices V_T. However, since a MOST's sub–threshold leakage current, $I_{leakage}$, is exponentially dependent upon the threshold voltage, V_T has not been able to decline as quickly as V_{DD} does in each new process generation because of concerns over increasing P_{avg} through P_{static}. Therefore, for instance, for five standard IBM bulk CMOS processes, the ratio of V_T/V_{DD} has increased noticeably – from V_T/V_{DD} = 0.5 V/2.5 V = 0.2 to V_T/V_{DD} = 0.29 V/1 V = 0.29 – between IBM's 0.25 μm and 65 nm nodes [8–12]. As one would expect, this trend shall continue on until the end of bulk CMOS scaling, at which point, V_{DD} and V_T/V_{DD} are predicted to reach 0.70 V and 0.355, respectively [13]. Another example in order to show how disproportionately V_T and V_{DD} have fallen in recent years is shown in Fig. 1.1 where the two parameters are plotted for six standard TSMC bulk CMOS processes [14].

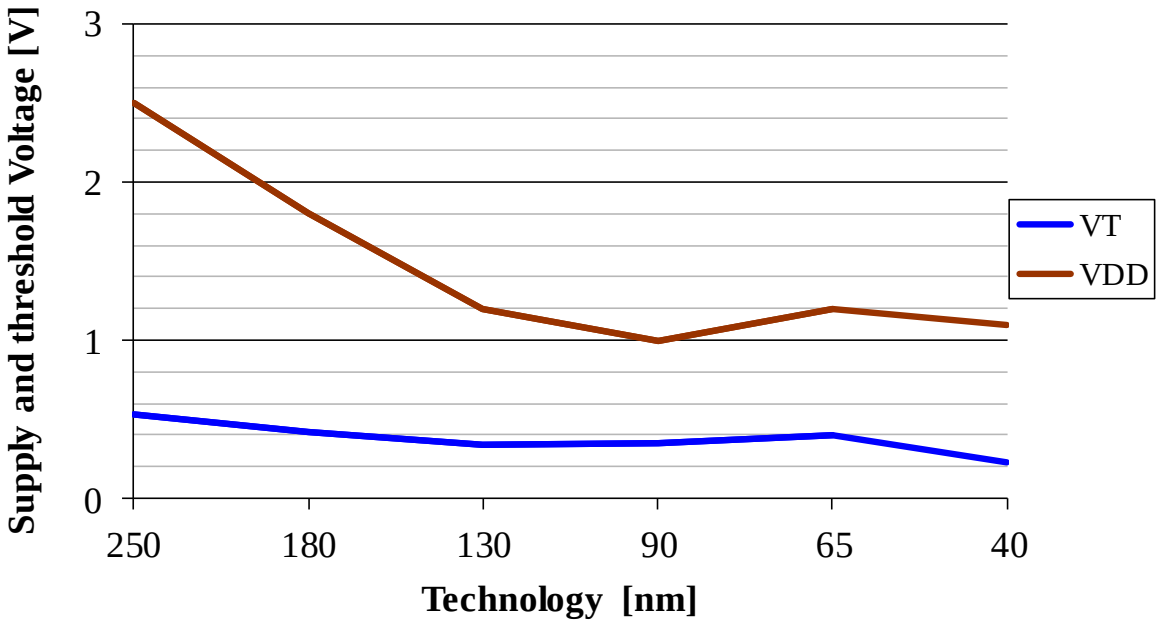

Fig. 1.1. A plot of the recent trends seen in V_T and V_{DD} for standard TSMC bulk CMOS processes.

On the other hand, the new trend of the design of modern implantable or portable biomedical devices is toward miniaturization and portability for long–term monitoring. Crucial parameters for these healthcare electronics are low power consumption and low supply voltage, and that makes biomedical applications another major target of low–power analog circuits. Biomedical signals can be classified into bioelectric, bioacoustic,

bioimpedance, biomechanical, biochemical and biomagnetic signals [15]. All these signals have very low amplitude in the range of microvolts to millivolts. For example, EEG signals (Electroencephalography signals), which are bioelectric signals, are varying between 5 and 100 microvolts [16]. Other bioelectric signals such as ECG (Electrocardiography), EMG (Electromyography), ERG (Electroretinography) and ENG (Electronystagmography) have about the same value of amplitude. Bioelectric signals (AKA Biosignals) are recorded as potentials, voltages, and electrical field strengths generated by nerves and muscles. Due to their low–level amplitude, integrated circuits are essential to be designed for the amplification of the weak signals before any further signal processing can be performed to make them compatible with devices such as displays, recorders, or A/D converters for computerized equipment. Amplifiers, adequately, have to measure these signals, satisfying very specific requirements. They have to provide amplification responsive to physiological signal, rejecting superimposed noise and interference signals, and guaranteeing protection from damages through voltage and current surges for both patient and electronic equipment. Amplifiers featuring these specifications are what we call *biopotential amplifiers*. In fact, amplifying such low voltages is very challenging. Fig. 1.2 shows an overview of the most commonly measured biopotentials, and specifies the normal ranges for amplitude and bandwidth [17]. To maintain a reasonable signal to noise ratio while minimizing energy consumption to maximize the useful life of the implant, the designer needs to use special circuit techniques and make difficult design compromises. I will address this issue in more detail later.

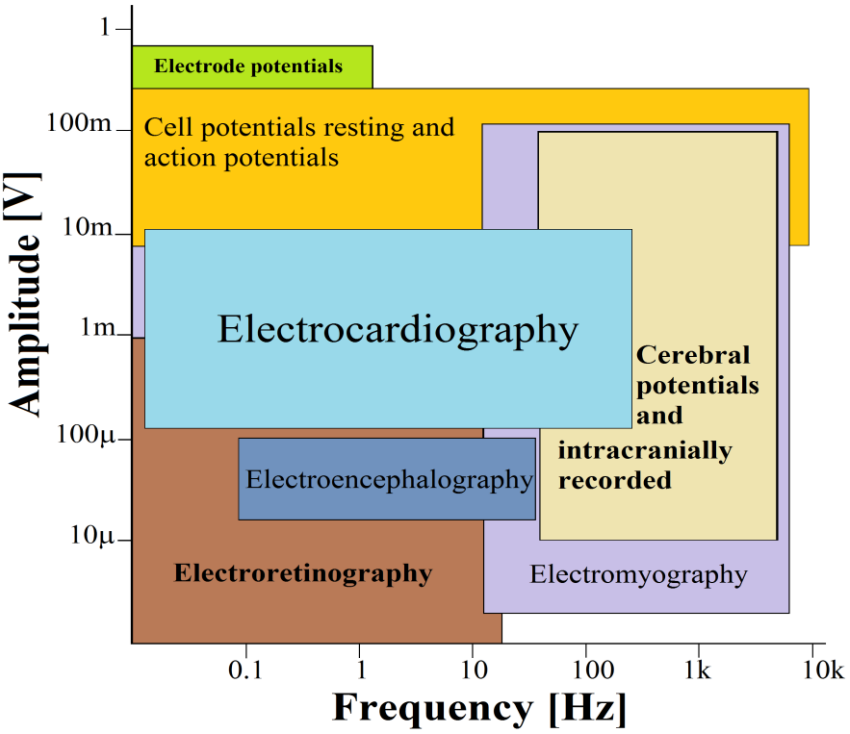

Fig. 1.2. Amplitudes and spectral ranges of some important biosignals.

The thesis is organized as follows: in section 2, a state–of–the–art of conventional and non–conventional techniques and structures, as well as developed technologies, which could

be implemented to obtain LV LP circuits is done. In section 3, circuits, in addition to application examples for them to prove their functionality, are designed using LV LP techniques. Finally, the main conclusions of this thesis are presented in section 4.

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2. STATE OF THE ART

Low–voltage low–power capability could be achieved either by developed technologies or by design techniques [1]. Since developed technologies are out of the scope of this thesis they will be mentioned briefly. The main technologies used for LV LP IC design are:

- CMOS technology [2]: is a MOS technology integrates both *N*–channel and *P*–channel transistors on the same chip. If the substrate of the circuit is *P*–doped, the *N*–channel transistors sit directly on the substrate, whereas the *P*–channel devices need a well (tube). The technology is termed *N*–well technology. For an *N*–type substrate the arrangement is complementary: the *P*–channel transistors are made in the substrate and the *N*–channel transistors sit inside the *P*–well (Fig. 2.1 [3]). CMOS technology is used in the fabrication of conventional microchips, since it is less expensive than BiCMOS and SOI technologies and offers high performance, high density and low–power dissipation.

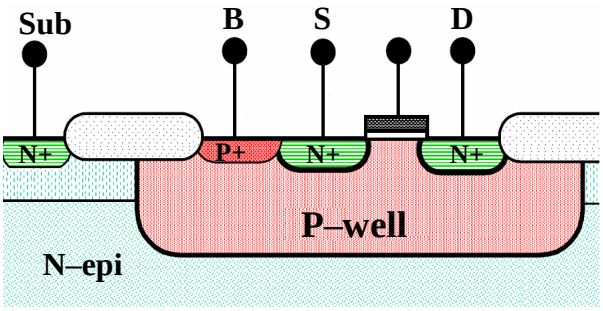


Fig. 2.1. Simplified cross section of an NMOST (*P*–well CMOS technology).

- BiCMOS technology [4, 5]: this technology integrates BJT and CMOS transistor in a single integrated circuit, thus combines the advantages of both. A number of advantages can be achieved using this advanced semiconductor technology such as: improving speed over purely bipolar technology, lowering power dissipation over purely CMOS technology, improving current drive over CMOS and packing density over bipolar, and obtaining high input impedance, low output impedance, high gain, low noise, high analog performance, flexible I/Os for high performance, latch–up immunity, smaller IC size and of more reliable IC. However, BiCMOS technology requires extra fabrication steps, the matter which makes the technology not cost–effective.

- SOI (Silicon On Insulator) technology [6–10]: in this technology a layer of silicon dioxide is implanted below the surface by oxidation of Si or by oxygen implantation into Si. This implanted silicon dioxide is called buried oxide (BOX) and helps reducing parasitic capacitances, and as a result improves the performance of the device. SOI can be divided into two categories, fully depleted FD and partially

depleted PD, the main differences are summarized in Tab. 2.1. Fig. 2.2 shows a starting wafer of FD–SOI.

Tab. 2.1. PD–SOI vs. FD–SOI.

PD–SOI	FD–SOI
The channel is doped.	The channel is often undoped or slightly doped.
The top silicon is 50 to 90 nm thick.	The top silicon is 5 to 20 nm thick.
The insulating BOX layer is typically 100 to 200 nm thick.	The insulating BOX layer may be ultra–thin: 5 to 50 nm.

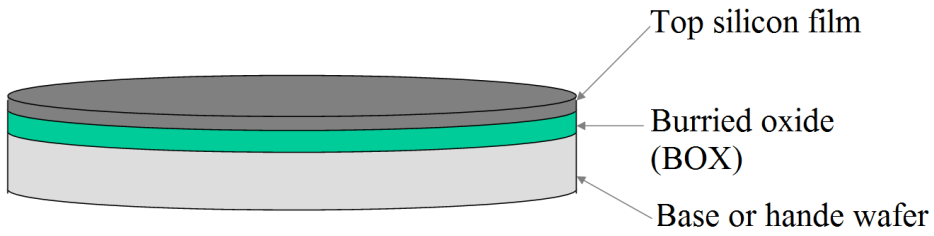


Fig. 2.2. FD–SOI starting wafer.

SOI technology has many advantages such as capacitance reduction, reduced short channel effects, lower device threshold, lower supply voltage, soft error rate effects, ideal device isolation, smaller layout area, high switching speed and lower–power consumption. However, fabrication of this technology is more expensive featuring also higher self–heating because of poor thermal conductivity of the insulator.

- Multi–gate transistors [11–14]: amongst the different types of SOI devices proposed, one clearly stands out: the multi–gate field–effect transistor (multi–gate FET). A multi–gate transistor is a MOST which incorporates more than one gate into a single device. This device has a general “wire–like” shape with a gate electrode that controls the flow of current between source and drain. Multi–gate FETs are commonly referred to as “multi(ple)–gate transistors”, “wrapped–gate transistors”, “double–gate transistors”, “FinFETs”, “tri(ple)–gate transistors”, “Gate–all–Around transistors”, etc. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. Fig. 2.3 shows a double–gate FinFET device. A multi–gate device employing independent gate electrodes is sometimes called a Multiple Independent Gate Field Effect Transistor (MIGFET). The International Technology Roadmap for Semiconductors (ITRS) recognizes the importance of these devices and calls them “Advanced non–classical CMOS devices”.

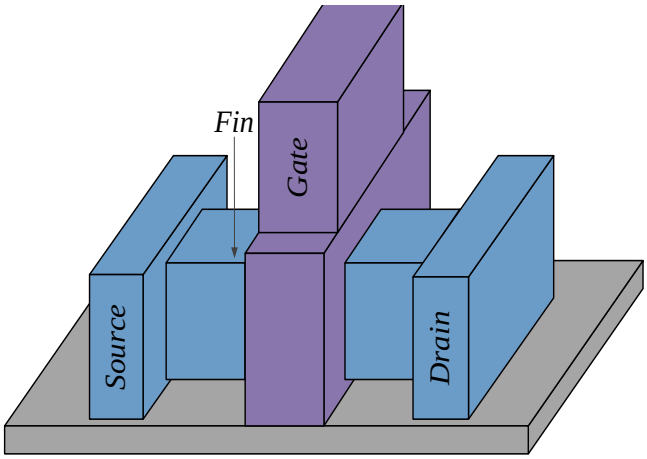


Fig. 2.3. Double–gate FinFET.

On the other hand, low–voltage design techniques are divided into two categories: conventional and non–conventional. All LV design techniques will be discussed in the next sub–section including principle of operation, small signal models of non–conventional techniques and main advantages and disadvantages of each technique.

2.1. SURVEY OF LOW–VOLTAGE DESIGN TECHNIQUES

Among the most important factors of CMOS VLSI processes is the threshold voltage of the MOS devices V_T. However, since a MOST's sub–threshold leakage current, $I_{leakage}$, is exponentially dependent upon the threshold voltage, V_T has not been able to decline as quickly as the power supply voltage V_{DD} does in each new process generation because of concerns over increasing P_{avg} through P_{static}. Another factor prevents the threshold voltage from being scaled down by the same ratio is that devices with higher threshold voltage value have higher noise margin and smaller leakages. In order to overcome this restriction many techniques have been introduced in the literature based on CMOS technology. By utilizing these techniques, the threshold voltage is decreased or –in some cases– even removed.

2.1.1 Conventional low–voltage techniques

The most widely used conventional techniques for low–voltage low–power analog circuits design are:

1) Circuits with rail–to–rail operating range.
2) MOS transistors operating in weak inversion region.
3) Level shifter technique.
4) MOS transistors in self–cascode structure.

2.1.1.1 Circuits with rail–to–rail operating range

Usually, gate–source voltage prevents the input stage from reaching the positive and/or negative supply voltages within the range of a threshold voltage; the value of this threshold voltage varies depending on semiconductor manufacturing process. This becomes a serious issue when the supply voltage is as low as 1 V or less in battery–powered systems or in low–power applications. A solution to this problem includes designing an input stage with a rail–to–rail common–mode input–voltage range allowing input common–mode signals to vary from negative to positive supply rails by the use of complementary differential pairs operated in parallel as shown in Fig. 2.4. [15, 16].

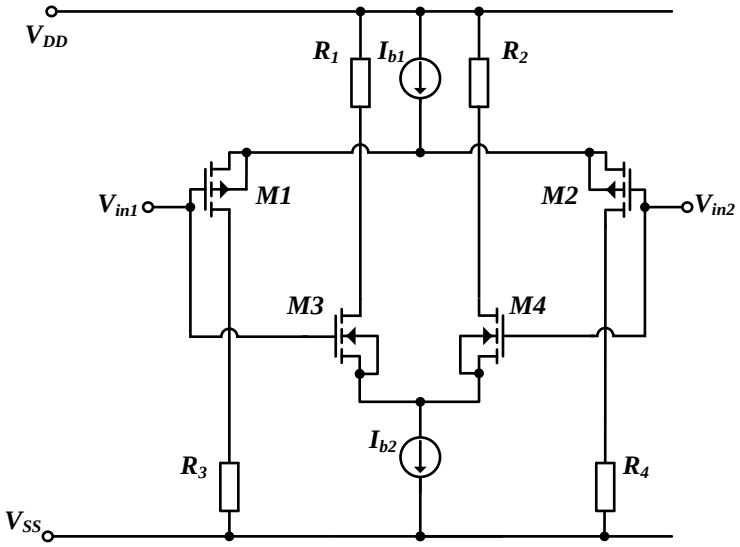


Fig. 2.4. Rail–to–rail input common–mode stage.

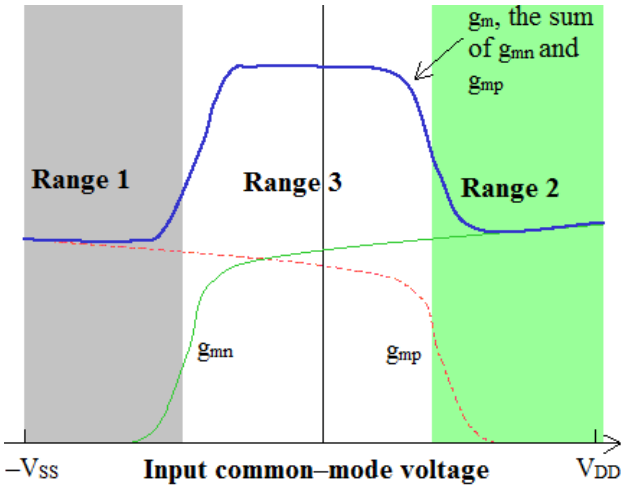


Fig. 2.5. Transconductance variations versus input common–mode voltage.

Three common–mode input voltage ranges can be distinguished as shown in Fig. 2.5:

1) In the range from the negative supply voltage V_{SS} to $V_{SS} + V_T$ only the PMOS pair Ml, M2 is operating.
2) In the range from the positive supply voltage V_{DD} to $V_{DD} - V_T$ only the NMOS pair M3, M4 is operating.
3) In the intermediate range both pairs are operating.

When the common–mode voltage moves from one range into another, the transconductance of the input stage changes by a factor of two. Because of this, the total transconductance is not constant across the input common–mode range. This is an undesired phenomenon because it not only results in non–constant gain and variable unity–gain frequency but also degrades the common–mode rejection ratio (CMRR) and causes the slew rate to vary. This prevents frequency compensation from being optimal since the bandwidth is proportional to that transconductance. Moreover, transient distortion occurs when fast changes in the common–mode voltage abruptly saturate and restore the tail–current sources.

A number of techniques have been proposed to achieve constant g_m [17–32]. A simple technique could be adopted to reduce the variations in the small–signal response of rail–to–rail input stage consists in shifting the common–mode response of one input pair so the curves of g_{mp} and g_{mn} shown in Fig. 2.5 overlap [33, 34]. With this approach, provided that the two differential pairs are perfectly matched, variations in the total amplifier transconductance can only arise in the common transition region of the two pairs, and are much lower with respect to the traditional composite rail–to–rail input stages [33]. Authors in [33], inspiring from [30] and [31], achieved adequate common–mode response shifting by connecting two floating and constant voltage sources V_S between the input signals and the gate terminals of one of the input pairs as shown in Fig. 2.6.

In Fig. 2.6, an appropriate positive value of V_S shifts the takeover region of the PMOS input pair, as seen by the signal inputs V_{in1} and V_{in2}, to a $V_{i,\mathrm{cm}}$ voltage range closer to the negative supply voltage. In [33, 34], authors also presented a technique in order to further decrease the total amplifier transconductance deviations, which mainly arise in the overlapping takeover regions, and named this technique as common–mode response shaping. According to their approach, the floating voltage sources have a variable value, which is a function of the input common–mode voltage [i.e., $V_S = \mathrm{f}\ (V_{i,cm})$]. Resulting variations in the small–signal transconductances versus input common–mode voltage is illustrated in Fig. 2.7.

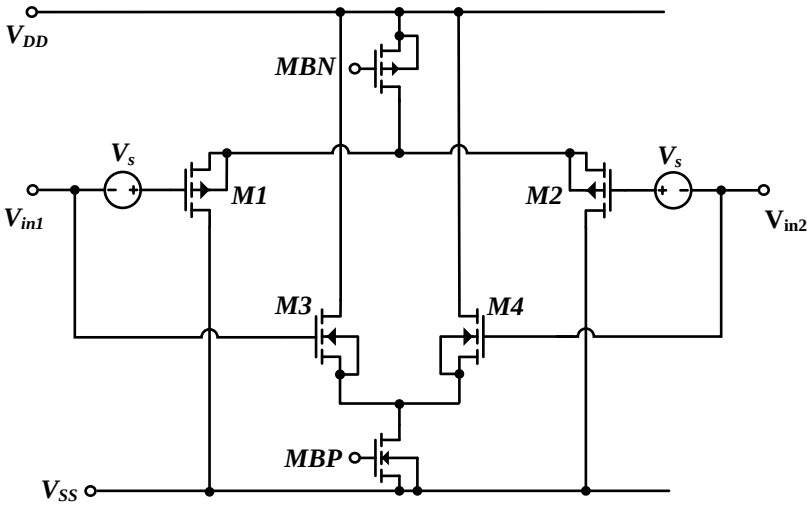


Fig. 2.6. Adding a floating voltage source at the inputs of the differential pair to implement common–mode response shaping.

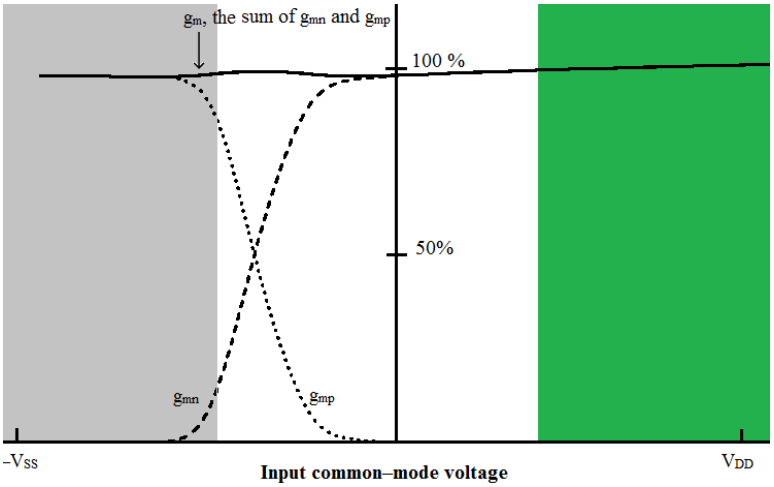


Fig. 2.7. Transconductance variations vs. input common–mode stage in Fig. 2.6.

Advantages

1) Obtaining an acceptable SNR (signal–to–noise ratio) in low–voltage environments [17–20, 24, 28, 30, 32, 35–42].
2) Circuits with rail–to–rail operating range can be used in low voltage analog design.
3) Rail–to–rail operation which allows input common–mode signals to vary from the negative to positive supply rails.

Disadvantages

1) Circuit complexity to obtain a constant transconductance value over the input voltage range.
2) THD and offset.

2.1.1.2 MOS transistors operating in weak inversion region

Another way to reduce the current levels and hence the power consumption of a circuit is by using MOS transistors biased in the weak inversion (or sub–threshold) region driving very low current levels. It is well known that in a NMOS transistor under the condition of drain–source voltage is greater than saturation voltage, when gate–source voltage exceeds an extrapolated value called threshold voltage V_T the MOST works in strong inversion (or saturation) region, and when it does not the MOST operates in weak inversion region. Actually, there is a region between these two regions called moderate inversion region, but for simplicity we will ignore this region and suppose that the transition between the weak and the strong inversion regions occurs abruptly.

In weak–inversion region, the applied gate–source voltage is barely larger (or even slightly less) than the threshold voltage of the NMOS transistor so a channel between the drain and the source is not established, but the aforementioned voltage is high enough so it creates a depletion layer at the surface of the silicon. Thus, in this region, the channel charge is much less than the charge in the depletion region so the drain current arising from the drift of majority carriers is negligible. When $V_{DS} > V_{ther}$ (around 3 V_{ther} which is about 78 mV) and $V_{GS} < V_T$, the current in this case is attributed to diffusion in the region and is given by:

$$I_{DS} = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS} - V_T}{\eta V_{ther}}\right). \tag{2.1}$$

I_{D0} is process–dependent parameter which is dependent also on bulk–source and threshold voltages. I_{D0} is given by:

$$I_{DO} = 2\eta \mu C_{ox} V_{ther}^2 \frac{W}{L}, \tag{2.2}$$

where η is the weak inversion slope factor and lies between 1.2 and 2, V_{ther} is the thermal voltage and equals 26 mV at room temperature and the other parameters have usual meanings.

Note from the equation that the current is independent of V_{DS} and exponentially proportional to the overdrive voltage. Again this result is valid only for big values of V_{DS}.

The transconductance of an MOST operating in weak inversion is identical to that of a corresponding bipolar transistor except for the factor of $1/\eta$:

$$g_m = \frac{I_{DS}}{\eta V_{ther}}. \tag{2.3}$$

Since the current in sub–threshold region is so small, the transconductance is expected to be very small.

Transconductance to current ratio is, however, a better criterion since it shows how efficiently the current is used to generate transconductance. This ratio of an MOST in weak inversion is given by:

$$\frac{g_m}{I_{DS}} = \frac{1}{\eta V_{ther}}, \quad (2.4)$$

which is independent of the current and the overdrive. Again, since the current is the lowest in weak inversion region, the transconductance to current ratio is the highest among any region of operation. Thus for high gain this region is preferred.

Last but not least, in weak inversion $C_{gs} \approx C_{gd} \approx 0$ where C_{gs} and C_{gd} are gate–source and gate–drain parasitic capacitances, respectively. Thus input capacitance C_{in}, which is approximately C_{gb}, can be thought of as the series combination of the oxide and depletion capacitors, as well as the transconductance is small as mentioned. Therefore the transition frequency f_T becomes very small because of the relationship: $f_T = \frac{g_m}{2\pi C_{in}}$.

Advantages

1) The ability to work in very low voltage environment, and here we are talking about just dozens of millivolts even for cascode structures.
2) Very suitable to be used in very low–power low–frequency applications such in the biomedical applications where operating frequencies range between 1 Hz to 1 kHz.

Disadvantages

1) Increased chip area.
2) Slow speed because of the low value of f_T as mentioned earlier.

2.1.1.3 Level shifter technique

In conventional two–transistor current mirror shown in Fig. 2.8 (a), the input transistor M1 is used in diode connected configuration and an input voltage V_{in} is required to pump I_{in} into the input port. Here, V_{in} depends solely on the biasing conditions of M1, which operates in saturation mode. Thus, this topology requires V_{in} of at least one threshold voltage V_T.

In level shifter technique, a MOST (or more) is inserted at the input port so that input voltage required is reduced to minimum. Fig. 2.8 (b) [43] shows a current mirror based on level shifter technique, from the circuit we note that $V_{in} = V_{DS1} = V_{GS1} - V_{GS3}$. So if we made $V_{GS3} \approx V_{GS1}$, V_{in} would approximately equal zero.

Assuming low bias current I_{bias} is presented; M3 operates in the sub–threshold region for the entire input current I_{in} range. The operation of M1 and M2 depends on their aspect ratios and on I_{in}. Hence, when $I_{in} < 1$ μA, M1 and M2 operate in the sub–threshold region and when I_{in} exceeds l μA they operate in the saturation region.

Practically, even with zero I_{in}, M1 and M2 work in weak inversion region, and this is the main problem of the technique. The reason of this drawback is the offset current I_{offset} caused by I_{bias}. I_{bias} drives V_{GS2} to be near V_{T1} even for zero I_{in}. V_{in} will also be zero, but V_{DS2} increases independently with V_{bias} causing I_{offset} to appear. When the input current is of the order of the offset current, I_{offset} decides the range of operation for such circuits.

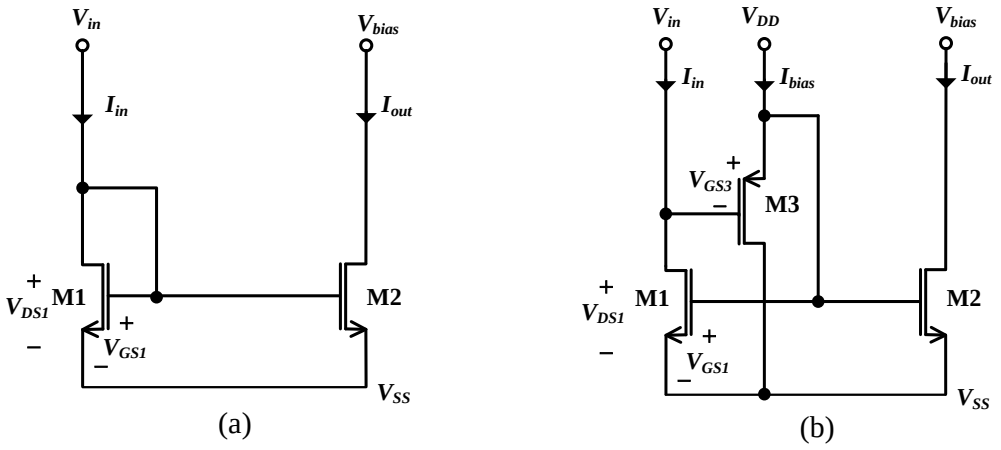


Fig. 2.8. Current mirror: (a) simple, (b) based on level shifter technique.

The offset current will be given by:

$$I_{offset} = \frac{W_2}{L_2}\frac{L_3}{W_3}\frac{I_{DO2}}{I_{DO3}} I_{bias} \exp\left(\frac{\Delta V_T}{\eta V_{ther}}\right), \tag{2.5}$$

where I_{DO2}, I_{DO3}, η and V_{ther} have been introduced before and ΔV_T is the mismatch between the threshold voltages of PMOST and NMOST.

Equation (2.5) indicates that I_{offset} can be tailored according to the designers' need through the appropriate selection of W and L.

Threshold voltage mismatch ΔV_T depends on particular CMOS technology. Even if the threshold voltages of PMOST and NMOST are matched and $I_{DO2} = I_{DO3}$, I_{offset} cannot be reduced to zero. The lower limit of I_{offset} equals $\frac{W_2}{L_2}\frac{L_3}{W_3} I_{bias}$. So to ensure low I_{offset}, appropriate values for W/L of M2 and M3 must be taken and I_{bias} must be as low as possible.

So far, we assumed that I_{bias} is low, but if we considered the case when I_{bias} is high the situation would be completely different. In this case, I_{bias} drives M3 into the saturation region; but M1 will be in linear mode due to low input current. However, M2 will operate in the saturation region because the external bias voltages will decide its drain voltage. In this situation the offset current is given by:

$$I_{offset} = \frac{\beta_2}{2}\left(\sqrt{\frac{2I_{bias}}{\beta_3}} - V_{TN2} + V_{TP3}\right)^2. \tag{2.6}$$

If threshold voltages of NMOST and PMOST were matched, the offset current would be:

$$I_{offset} = \frac{K_2}{K_3}\frac{W_2}{L_2}\frac{L_3}{W_3} I_{bias}, \tag{2.7}$$

where K_2 and K_3 are the transconductance parameters for M2 and M3, respectively. The ratio's value of $\frac{K_2}{K_3}$ is usually around 3 which makes the offset current sufficiently high, so I_{bias} must always be kept as low as possible to reduce I_{offset} and to keep the ratio of $\frac{K_2}{K_3}$ away from the calculation of I_{offset}.

Advantages

1) The input resistance is low, which is desirable for current mode circuits.
2) The bandwidth at low voltage is higher.
3) Rail–to–rail and low voltage operation.

Disadvantages

— This technique utilizes more transistors which increases the power dissipation.

2.1.1.4 MOS transistors in self–cascode structure

Along with the scaling of MOST size, the output impedance is reducing since it is proportional to channel length (or more accurately to effective channel length). Thus the gain is also degrading.

A solution to this problem could be in using the cascode structure, but although this technique increases the output impedance, it decreases the output signal swing, thus cascode structure cannot be used in low voltage systems [43].

Because it does not require high compliance voltages at output nodes, self–cascode (SC) configuration shown in Fig. 2.9 (a) [44] provides high output impedance with larger voltage headroom than the conventional cascode structure offers. This approach has potential applications in low voltage design.

A self–cascode structure can be treated as a single composite transistor (as shown in Fig. 2.9 (b)) operating in saturation region but without severe channel–length modulation effects. The composite structure has much larger effective channel length and the effective output conductance is much lower.

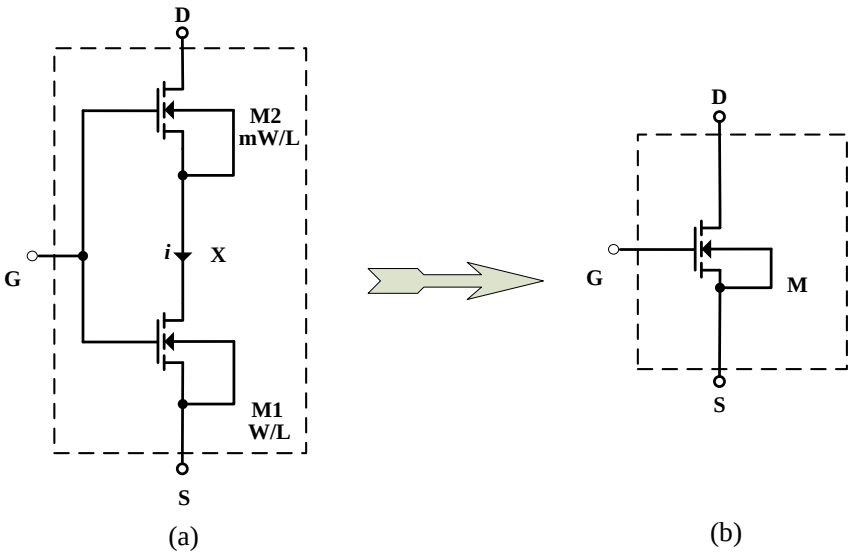


Fig. 2.9. (a) Self–cascode structure, (b) equivalent composite transistor.

The lower transistor M1 operates in non–saturation (linear) region. Depending on the drain voltage, transistor M2 can work in saturation or linear region.

For the composite transistor to work in saturation region; M2 should work in saturation region and M1 should work in linear region. Thus, we can write equations for these two transistors as:

$$i = \frac{\beta_2}{2}(V_{GS} - V_X - V_T)^2 = \beta_1\left(V_{GS} - V_T - \frac{1}{2}V_X\right)V_X . \tag{2.8}$$

Solving *i* we obtain:

$$i = \frac{1}{2}\beta_{eq}(V_{GS} - V_T)^2 , \tag{2.9}$$

where $\beta_{eq} = \dfrac{\beta_1\beta_2}{\beta_1 + \beta_2}$ is the effective transconductance.

For optimal operation the *W/L* ratio of M2 should be larger than that of M1 by the factor of *m* so that *m>1*.

If $\beta_2 = m\beta_1$ then:

$$\beta_{eq} = \frac{m}{m+1}\beta_1 = \frac{1}{1+m}\beta_2 \Rightarrow \beta_{eq}\big|_{m\to\infty} = \beta_1 . \tag{2.10}$$

So if we kept the channel length the same for both transistors and made W_2 wide enough, W_1 would be in charge of controlling the current.

The equivalent output impedance of the composite transistor is:

$$r_o \approx (m-1) r_{o-M2} . \tag{2.11}$$

The effective transconductance of the composite transistor is approximately equal to the transconductance of M1:

$$g_{m-eff} \approx \frac{g_{m-M2}}{m} = g_{m-M1} . \tag{2.12}$$

As mentioned before, M1 usually works in linear region, so the voltage between its drain and source is so small that there is no considerable difference between V_{DSAT} of composite and simple transistors.

Advantages

1) The SC structure offers high output impedance similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor.
2) Unlike cascode circuits, SC circuit does not require additional real–estate and power for its operation [45].

Disadvantages

— Its drawbacks are limited input common mode range and small output swing.

2.1.2 Non–conventional low–voltage techniques

The most widely used non–conventional approaches for low–voltage low–power analog circuits design are:

1) Bulk–driven MOST.
2) Floating–gate approach.
3) Quasi–floating–gate approach.
4) Bulk–driven floating–gate and bulk–driven quasi–floating–gate approach.

2.1.2.1 Bulk–driven MOST

Bulk–driven MOST (BD MOST) concept was first proposed by A. Guzinski et al in 1987 [46]. After that and as evidenced in the literature during the last years, BD technique has been adopted to implement a number of analog building blocks such as operational amplifiers [47–51], current mirrors [52–54], current conveyors, [55], [56], operational transconductance amplifiers [47], [49], [57–61], voltage followers [62], [63], voltage to current converters [64], buffers [65], voltage–controlled oscillators [66], and phase–locked loops [67]. An NMOST and its cross–section are shown in Fig. 2.10.

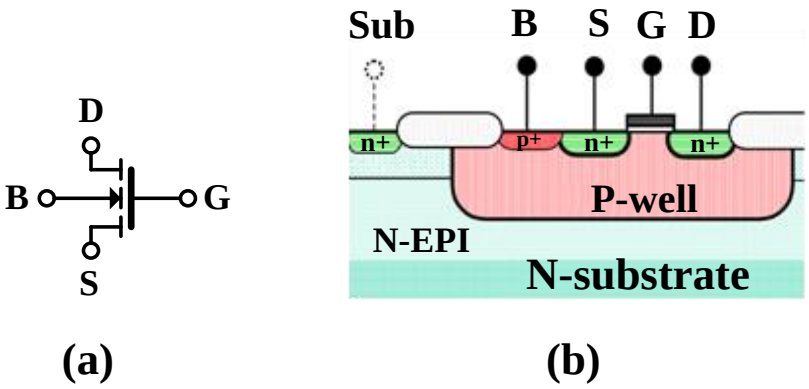


Fig. 2.10 Bulk–driven NMOST: (a) symbol and (b) cross–section.

In BD technique, a bias voltage is applied to the gate of the MOST so a channel is established between the source and the drain. This channel remains constant as long as the gate bias voltage is still the same, as the case for BD technique. On the other hand, the signal is applied to the bulk contact. By this way, the limitation of threshold voltage on the signal pathway is eliminated; consequently, the applicability of any analog cell to a very low supply voltage is possible to be extended.

Since the bulk contact serves the function of the gate of JFET and modulates the channel width according to the voltage applied to the bulk (see Fig. 2.11), BD MOST is considered as a depletion type device. For *N*–channel (*P*–channel), BD MOST can work in negative (positive), zero or slightly positive (negative) biasing condition.

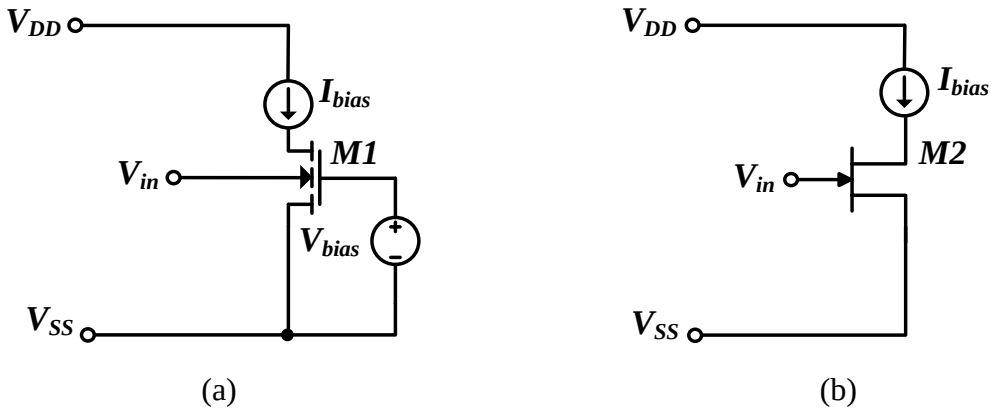
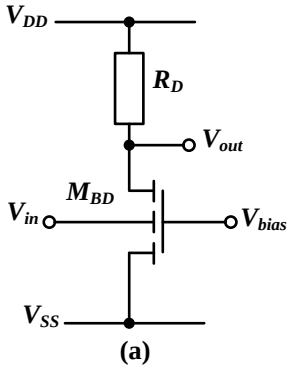
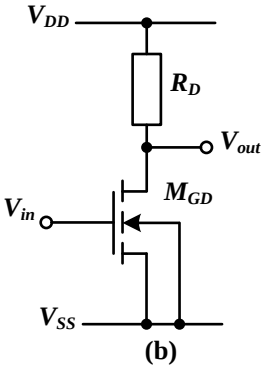


Fig. 2.11. Bulk–driven MOS transistor (a), and its equivalent JFET (b).

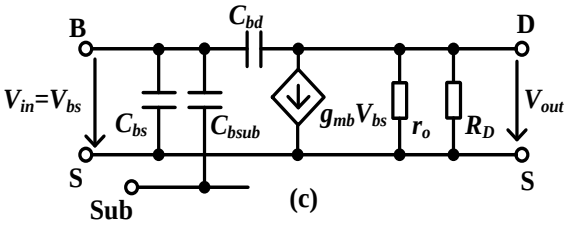
An important aspect in analog design is small signal analysis. To study the small signal equivalent circuit of BD MOST in comparison with the small signal equivalent circuit of gate–driven MOST (GD MOST), BD and GD common–source (CS) amplifiers are shown in Fig. 2.12 (a,b), and the small signal equivalent circuits at high frequencies of the SC amplifiers are shown in Fig. 2.12 (c,d).



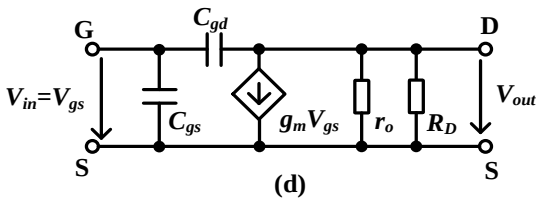
BD MOST based CS amplifier



GD MOST based CS amplifier



Small signal equivalent circuit of (a)



Small signal equivalent circuit of (b)

Fig. 2.12. (a) CS amplifier based on BD MOST. (b) CS amplifier based on GD MOST. (c) Small signal equivalent circuit of the BD based CS amplifier. (d) Small signal equivalent circuit of the GD based CS amplifier.

The capacitances C_{bd}, C_{bs}, C_{bsub} are bulk–drain, bulk–source and bulk–substrate parasitic capacitances, respectively. These parasitic capacitances are a result of well and substrate structure of the transistor.

The relationship between threshold voltage and bulk–source voltage in BD MOST is:

$$V_T = V_{T0} \pm \gamma(\sqrt{|2\phi_F| - V_{BS}} - \sqrt{|2\phi_F|}) \,. \tag{2.13}$$

With + for an NMOST and – for PMOST where V_T is the threshold voltage, V_{BS} is the bulk–source voltage, V_{T0} is the threshold voltage at zero bulk–source voltage, γ and ϕ_F are the bulk–threshold parameter and the surface potential, respectively.

The transconductance of GD MOST which operates in strong inversion is given by:

$$g_m = k\frac{W}{L}(v_{gs} - V_T) \,, \tag{2.14}$$

where k is the current gain factor of the used process. However, the transconductance of BD MOST is given by:

$$g_{m,b} = \frac{\gamma}{2\sqrt{|2\phi_F - V_{BS}|}} g_m = \frac{C_{BC}}{C_{GC}} g_m \cong (0.2 \to 0.4) g_m \,, \tag{2.15}$$

where C_{BC} and C_{GC} are the total bulk–channel and the total gate–channel parasitic capacitances, respectively.

To determine the frequency performance of a transistor, transition frequency f_T must be calculated. To calculate f_T, consider the AC circuit in Fig. 2.13 (a) and the small signal equivalent in Fig. 2.13 (b).

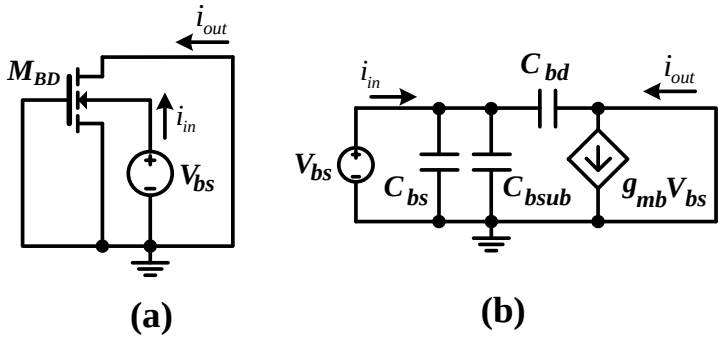


Fig. 2.13. Circuits for calculating transition frequency of BD MOST: (a) AC schematic, (b) small signal equivalent circuit.

The small signal input current i_{in}:

$$i_{in} = s(C_{bs} + C_{bsub} + C_{bd}) v_{bs} \,. \tag{2.16}$$

If the current through C_{bd} is neglected then i_{out}:

$$i_{out} \approx g_{mb} v_{bs} \,. \tag{2.17}$$

From (2.16) and (2.17) we can calculate the current gain:

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb}}{s(C_{bs} + C_{bsub} + C_{bd})} \,. \tag{2.18}$$

We substitute s with jw then we get:

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{mb}}{j\omega\,(C_{bs} + C_{bsub} + C_{bd})} \,. \tag{2.19}$$

The magnitude of the small signal current gain is unity when:

$$\omega = \omega_T = \frac{g_{mb}}{C_{bs} + C_{bsub} + C_{bd}} \,. \tag{2.20}$$

Then the transition frequency of the BD MOST is given by:

$$f_{T,b} = \frac{1}{2\pi}\omega_T = \frac{1}{2\pi}\frac{g_{mb}}{C_{bs}+C_{bsub}+C_{bd}} \ . \tag{2.21}$$

Assuming that (C_{bs} + C_{bsub}) is much greater than C_{bd}, then:

$$f_{T,b} = \frac{g_{mb}}{2\pi(C_{bs}+C_{bsub})} \approx (0.3 \to 0.5) f_T \ , \tag{2.22}$$

whereas f_T is transition frequency of GD MOST which can be calculated by following the same steps:

$$f_T = \frac{g_m}{2\pi C_{gs}} \ . \tag{2.23}$$

From (2.22) it is obvious that the transition frequency of BD MOST is smaller than the transition frequency of GD MOST, since the transition frequency is proportional to the transconductance, as well as the effect of the parasitic capacitances.

The input referred noise power spectral density of GD MOST is expressed by:

$$v^2_{noise,GD} = \frac{i^2_{ni}}{g^2_m} \ , \tag{2.24}$$

where i^2_{ni} is the total drain current generated by noise sources and its unit is A^2. The input referred noise power spectral density of BD MOST can be expressed by:

$$v^2_{noise,BD} = \left(\frac{g_m}{g_{mb}}\right)^2 v^2_{noise,GD} \ . \tag{2.25}$$

BD MOST suffers from higher referred noise as it is clear from (2.25), since $g_{m,b}$ is inherently smaller than g_m.

BD MOST and GD MOST have identical output resistance r_o as we can notice from Fig. 2.12 and its value is given by:

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda I_{DSsat}} \ . \tag{2.26}$$

Advantages

1) As mentioned, *N*–channel bulk–driven MOST works in negative, zero or slightly positive bias voltage also. This can lead to larger input common mode voltage range and voltage swing that could not otherwise be achieved at low power supply voltages.
2) Depletion characteristics avoid V_T requirement in the signal path. Voltage swing for low voltage supply is increased, and minimum operational supply voltage is pushed to its limit.

3) This technique offers a possibility of using the conventional gate to modulate the BD MOST since the transfer characteristic changes greatly with different V_{GS}, because I_d is more sensitive to V_{GS} than to V_{BS}.

4) Better linearity and smaller power supply requirements because of the small value of the transconductance of the bulk–driven MOST, $g_{m,b}$.

5) Suitable for rail–to–rail applications.

6) Can be modeled using the conventional MOS transistor.

Disadvantages

1) The transconductance of the device, $g_{m,b}$, is typically 20–40% of the transconductance of a conventional gate–driven MOST, g_m, based on long–channel theory. This –as shown in equations– limits both the intrinsic gain and the cut–off frequency of the device, and increases the equivalent input noise voltage.

2) The polarity of the BD MOSTs is process related; only *N*–channel BD MOSTs are available for *P*–well process, and on the other hand, only *P*–channel BD MOSTs are available for *N*–well process. This limits the applicability of this technique since we cannot use BD MOS transistors in some circuit structures which require both N and P MOSTs.

3) Bulk terminals of all BD MOSTs usually have to be isolated, so it is necessary for each BD MOST to reside within its own separate well for many applications. Accordingly, the BD MOST consumes more area than its GD counterpart does and further suffers from a degraded frequency response due to the added input capacitance from its well structure. More than that, the matching between BD MOSTs in differential wells suffers. Thus analog circuits with tight matching between MOSTs are difficult to fabricate.

4) When V_{BS} is critically large (more than the turn–on voltage of the bulk–channel PN junction diode), latch–up incurs.

2.1.2.2 Floating−gate approach

The first appearance of floating–gate technique was in 1967 [68]. In the late 1980s, the Intel ETANN chip employed it as an analog nonvolatile memory element [69]. From that date, floating–gate devices are finding wider applications by analog researchers. A number of papers have been reported in the literature for applications of floating–gate technique in analog circuits, such as floating–gate CMOS analog trimming circuits [70], neural network components, multipliers [71], D/A converters [72], amplifiers [73–75], operational transconductance amplifiers [76], and differential voltage current conveyors [77].

These devices can be fabricated in all CMOS technologies, but a double poly CMOS technology is preferred [78].

In FG MOST, the gate is fabricated using the gate electrode (poly1) layer and is surrounded by two SiO_2 insulator layers thus electrically isolated from the rest of the device.

The device inputs are placed on top of the upper SiO_2 insulating layer and are fabricated using another conducting layer, preferably a second layer of polysilicon (poly2). Thus, from the dc operating point of view, the gate is floating node, and that is why the MOST is called floating–gate MOST. Inputs are capacitively coupled to the FG, and the sizes of the input electrodes determine the values of the capacitors, they can be varied according to the designer's needs. The circuit symbol, equivalent circuit, layout, and cross–section of a two–input floating–gate NMOST are shown in Fig. 2.14 [61].

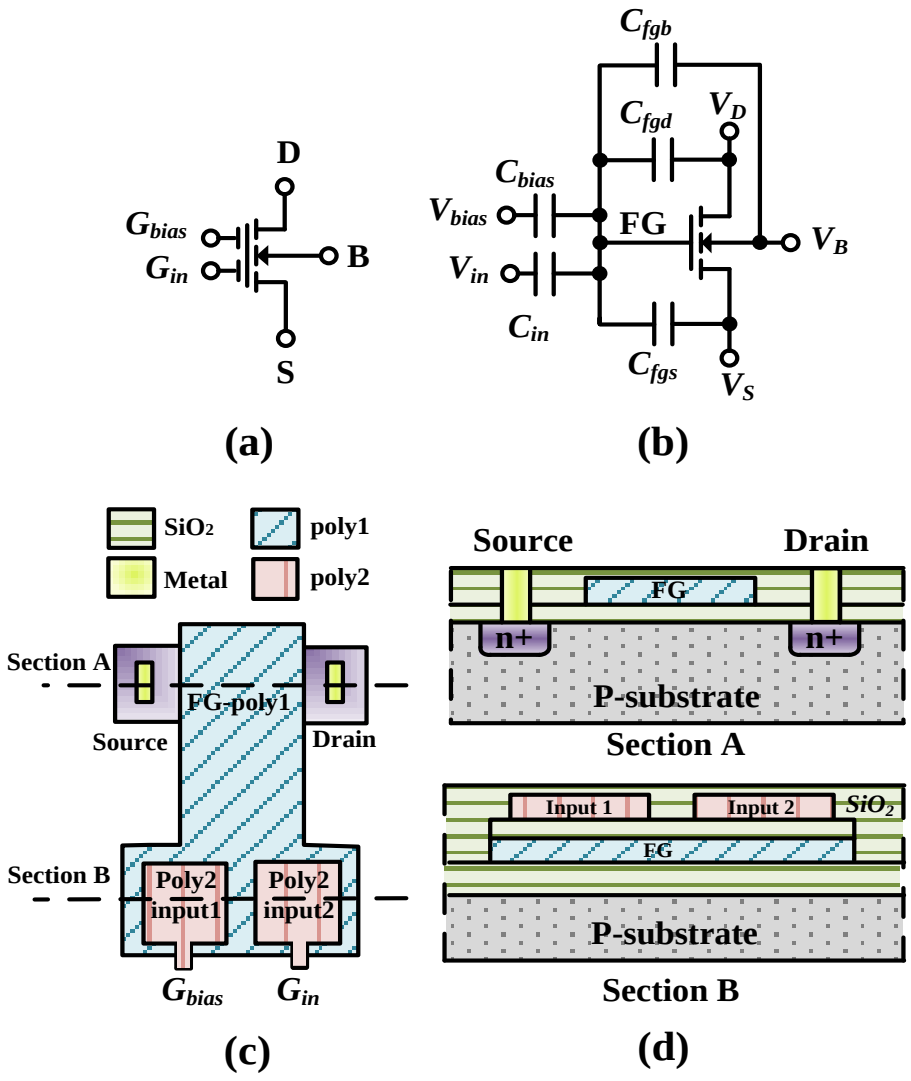


Fig. 2.14. Two–input floating–gate NMOST: (a) symbol, (b) equivalent circuit, (c) layout and (d) cross–section.

During fabrication, an amount of charge Q_{FG} traps in the FG and should be removed in order MOST to be valid to use in analog applications. As this term is constant, it can be interpreted as a voltage offset at the FG, or alternatively, as an offset in the threshold voltage of the device. Reported solutions to remove Q_{FG} include cleaning with ultraviolet (UV) light

shining [43], [78–80], hot–electron injection [43], [78], [79], Fowler–Nordheim (FN) tunneling [78–80], and forcing an initial condition with a switch [78].

By applying the charge conservation law to the floating node, the voltage at the FG is given by:

$$V_{FG} = \frac{Q_{FG} + C_{fgd} V_D + C_{fgs} V_S + C_{fgb} V_B + \sum_{i=1}^{n} C_{Gi} V_{Gi}}{C_{Total}}, \tag{2.27}$$

where n is the number of effective inputs, the term Q_{FG} has been introduced before, C_{fgd}, C_{fgs}, and C_{fgb} denote the parasitic capacitances from gate to drain, source, and bulk, respectively, V_D, V_S, and V_B are drain, source, and bulk voltages, C_{Gi} is the coupling capacitance of the ith input branch, V_{Gi} is voltage of the ith control gate, and the term C_{Total} refers to the total capacitance seen by the FG and is given by:

$$C_{Total} = C_{fgd} + C_{fgs} + C_{fgb} + \sum_{i=1}^{n} C_{Gi} \ . \tag{2.28}$$

Let us consider the common source amplifier shown in Fig. 2.15 (a), where V_{bias} is applied at one gate through C_{bias} and V_{in} is applied at the second gate through C_{in}. The small signal equivalent circuit is depicted in Fig. 2.15 (b).

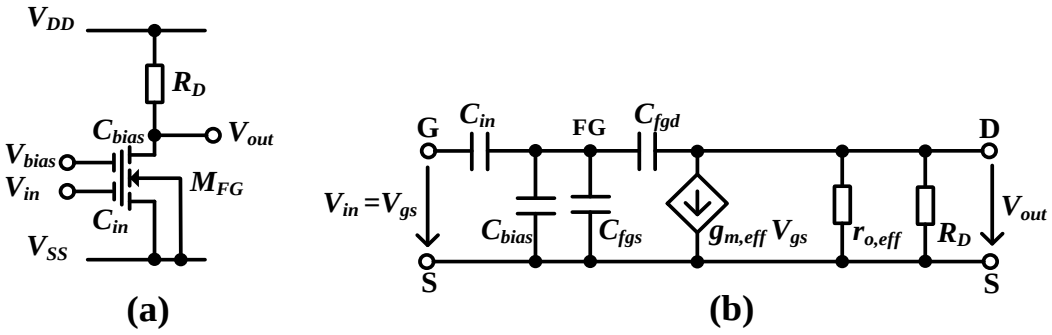


Fig. 2.15. Floating–gate MOST: (a) common source amplifier and (b) small signal model equivalent circuit.

Assuming zero initial charge and neglecting parasitic capacitances as compared to C_{bias} and C_{in}, the gate voltage of MOST shown in Fig. 2.15 is:

$$V_{FG} \approx k_1 V_{in} + k_2 V_{bias}, \tag{2.29}$$

where $k_1 = \frac{C_{bias}}{C_{Total}}$ and $k_2 = \frac{C_{in}}{C_{Total}}$.

The equivalent threshold voltage for the MOST adjusts itself to a new value $V_{T,eq}$:

$$V_{T,eq} = \frac{V_T - V_{bias} k_1}{k_2} . \tag{2.30}$$

The effective transconductance is given by:

$$g_{m,eff} = k_2 g_{m,FG} , \tag{2.31}$$

where $g_{m,FG}$ is the transconductance seen from the floating gate.

When g_{ds} is the output conductance of a MOST, the effective output conductance of the floating–gate MOST $g_{ds,\text{eff}}$ is:

$$g_{ds,eff} = g_{ds} + g_{m,FG} \frac{C_{fgd}}{C_{Total}} . \tag{2.32}$$

The effective output conductance of the FG MOST is larger than the output conductance of the GD MOST, because of DC and AC feedback from drain to floating gate through C_{fgd}.

To calculate transition frequency, let's consider the AC circuit and its small signal equivalent circuit in Fig. 2.16:

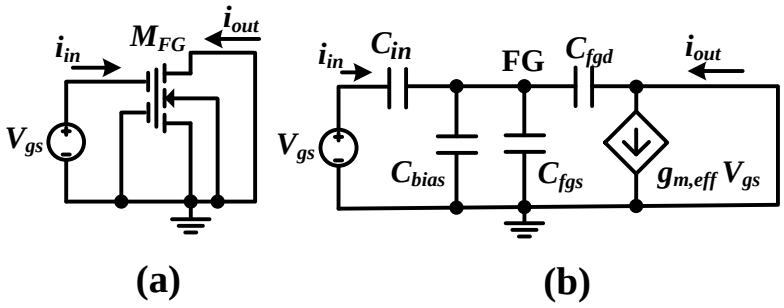


Fig. 2.16. Circuit for calculating transition frequency of FG– MOST: (a) AC schematic, (b) small signal equivalent circuit.

The small signal input current is:

$$i_{in} = s\left[\frac{C_{in}(C_{bias} + C_{fgs} + C_{fgd})}{C_{Total}}\right] v_{gs} . \tag{2.33}$$

If the current through C_{fgd} is neglected then:

$$i_{out} \approx g_{m,eff} v_{gs} . \tag{2.34}$$

From (2.33) and (2.34), the current gain can be written:

$$\frac{i_{out}}{i_{in}} = \frac{g_{m,eff}}{s\left[\frac{C_{in}(C_{bias} + C_{fgs} + C_{fgd})}{C_{Total}}\right]} . \tag{2.35}$$

By following the same steps done to find transition frequency of BD MOST at the previous subsection, the transition frequency equation of FG MOST will be given by:

$$f_{T,FG} = \frac{g_{m,eff}}{2\pi\left[\frac{C_{in}(C_{bias}+C_{fgs}+C_{fgd})}{C_{Total}}\right]}. \tag{2.36}$$

Assuming C_{fgs} is much greater than C_{fgd} and substituting the effective transconductance value from (2.31), then:

$$f_{T,FG} = \frac{g_m}{2\pi(C_{bias}+C_{fgs})}. \tag{2.37}$$

The transition frequency equation of FG MOST is given by:

$$f_{T,FG} = \frac{g_m}{2\pi(C_{bias}+C_{fgs})}. \tag{2.38}$$

It is clear that the transition frequency of FG MOST is smaller than the transition frequency of GD MOST; hence FG MOST has smaller bandwidth than GD MOST.

The relationship between the input referred noise power spectral density of FG MOST and GD MOST is given by:

$$v^2_{noise,FG} = \left(\frac{C_{Total}}{C_{in}}\right)^2 v^2_{noise,GD}. \tag{2.39}$$

It is evident from the equation that the input referred noise increases at the effective input of the FG MOST.

Advantages

1) $V_{T,eq}$ can be programmed to be less than V_T with the appropriate selection of V_{bias}, k_1 and k_2. Thus the floating gate technology can be used in low voltage analog design.
2) Can be used in ultra–low power ultra–low voltage applications.
3) Possibility of multi–input terminals.
4) Can be fabricated in any MOS technology, although for better performance double poly technology is recommended.
5) Rail to rail operation.

Disadvantages

1) FG MOST consumes much larger silicon area compared with the MOS transistor due to the added input capacitors. However, with a careful design and layout, the extra area can be minimized and the effect of the charge can be negligible [78].

2) There is a reduction in the transconductance by a factor of k_2. However, smaller transconductance results in higher input referred noise voltage as well as smaller cut–off frequency, accordingly, smaller bandwidth.
3) Because there is DC and AC feedback from drain to floating gate through C_{fgd}, the output impedance is less than that of a MOST working in the same biasing condition.
4) There is uncertain amount of charge might remain trapped at the FG during fabrication. Although there are many procedures could be done to change this charge, these programming techniques are relatively complex.
5) Further manufacturing process is required.

2.1.2.3 Quasi–floating−gate approach

To overcome the main problems of the floating–gate MOST, namely the initial charge trapped in the floating gate problem and the large silicon area problem, a quasi–floating–gate MOST (or pseudo–floating–gate MOST) is an appropriate solution [81]. Applications based on QFG MOSTs include: differential operational amplifiers [82], [83], transconductors [84–86], current mirrors [87], filters [88], current conveyors [89–91], and linear MOS resistors [92].

Floating–gate MOSTs use voltage dividers with relatively large attenuation factors at the transistor gates to reduce supply requirements. The dividers use large capacitance to set the floating gate DC voltage close to one of the supply rails. Unfortunately, this large capacitance leads to an increase in silicon area and a reduction of the effective transconductance and gain–bandwidth product (GBW). Besides, as mentioned before, some technique is required to avoid the initial charge trapped in the floating gate.

All these issues are solved by weakly connecting the floating gate to a proper DC voltage using a large–valued resistor which can be implemented by the leakage resistance of a reverse–biased junction of a diode–connected MOS transistor operating in cutoff region. Therefore, this pull–up or pull–down resistor R_{leak} sets the DC gate voltage to a power rail, thus preventing initial charge issues and simultaneously minimizing the supply voltage requirements. The large resistance value employed makes the gate effectively floating from signal frequencies of above 0.05 Hz so that AC operation is unaffected even for very low frequencies. At the same time, GBW degradation effects are avoided since a large biasing capacitor is no longer required.

The symbol of single input terminal QFG MOST (a), its equivalent circuit (b) and layout (c) are shown in Fig. 2.17. The input terminals are capacitively coupled to the quasi–floating gate, but the DC gate voltage is set to V_{bias} without requiring a large capacitor.

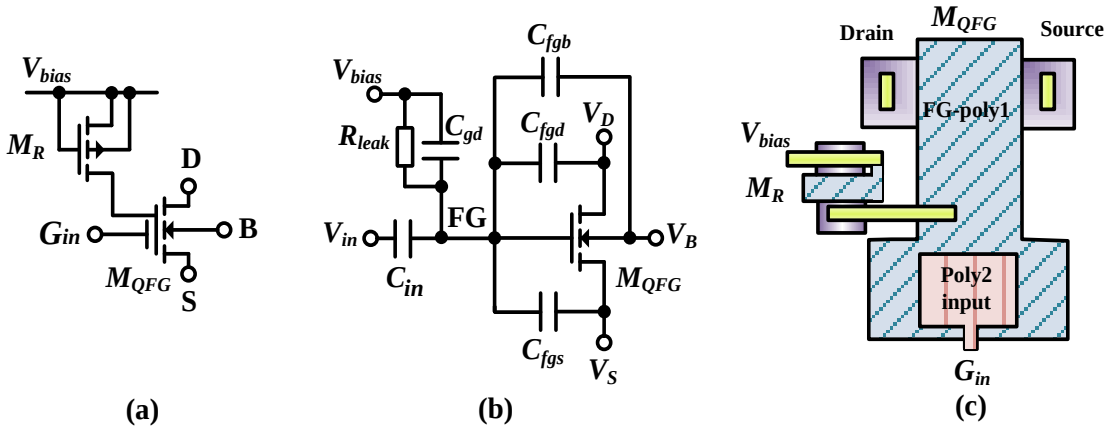


Fig. 2.17. One–input quasi–floating–gate NMOST: (a) symbol, (b) its equivalent circuit and (c) layout.

The pull–up or pull–down resistor can be implemented in practice by the large (and nonlinear) leakage resistance of reverse–biased p–n junction of MOS transistor operating in cutoff region, as shown in Fig. 2.18 (a). This fact leads to significant savings in terms of area compared to the MIFG device.

A simple analysis reveals that the AC voltage at the floating gate is given by:

$$V_{QFG} = \frac{s R_{leak}}{1 + s R_{leak} C_{Total}} \times (C_{fgd} V_D + C_{fgs} V_S + C_{fgb} V_B + \sum_{k=1}^{n} C_k V_k) , \tag{2.40}$$

where C_{fgd} C_{fgs}, and C_{fgb} denote the parasitic capacitances from gate to drain, source, and bulk respectively, V_D, V_S, and V_B are drain, source, and bulk voltages, C_k is the coupling capacitance of the kth input branch, V_k is voltage of the kth control gate, C_{Total} is the total capacitance and is given by:

$$C_{Total} = C_{gd} + C_{fgd} + C_{fgs} + C_{fgb} + \sum_{k=1}^{n} C_k \quad , \tag{2.41}$$

where C_{gd} represents the gate–drain parasitic capacitance of the reversed–biased MOS transistor implementing the high–value resistor M_R. Note from (2.40) that inputs are high–pass filtered with a cutoff frequency $1/2\pi R_{leak} C_{TOTAL}$, which can be made very low. Note also that the exact value of R_{leak} or its temperature and voltage dependence are unimportant, provided that R_{leak} remains large enough not to influence the circuit operation at the lowest frequency required. The exact value of C_{Total} is also unimportant.

For NMOST (PMOST), the pull–up (pull–down) resistor R_{leak} sets the gate to a DC voltage equal to the positive (negative) rail, to which an AC voltage given by (2.40) is superimposed. Hence, the gate voltage can become more (less) than V_{bias}. This does not pose a

problem as long as the amplitude of the signals is (approximately) limited to 0.5 V in order to avoid forward biasing of the junction implementing R_{leak}, so that it never becomes forward–biased. For larger signal amplitudes, utilization of two reverse–biased junctions in series can increase the maximum signal amplitude.

Due to a large value of R_{leak}, even at low frequencies, (2.40) can be simplified as follows:

$$V_{QFG} = \frac{1}{C_{Total}} \times (C_{fgd}\, V_D + C_{fgs}\, V_S + C_{fgb}\, V_B + \sum_{k=1}^{n} C_k\, V_k)\,. \tag{2.42}$$

Note from (2.42) that the voltage at the floating gate becomes a weighted averaging of the AC input voltages determined by capacitance ratios when the parasitical capacitance is negligible.

Fig. 2.18 shows the common source amplifier based on QFG MOST in (a) and its small signal equivalent circuit in (b), where the previous capacitors are shown, however the floating gate–bulk capacitance is ignored, because it has no influence on signal path. The operation principle of the QFG MOST is similar to the FG MOST.

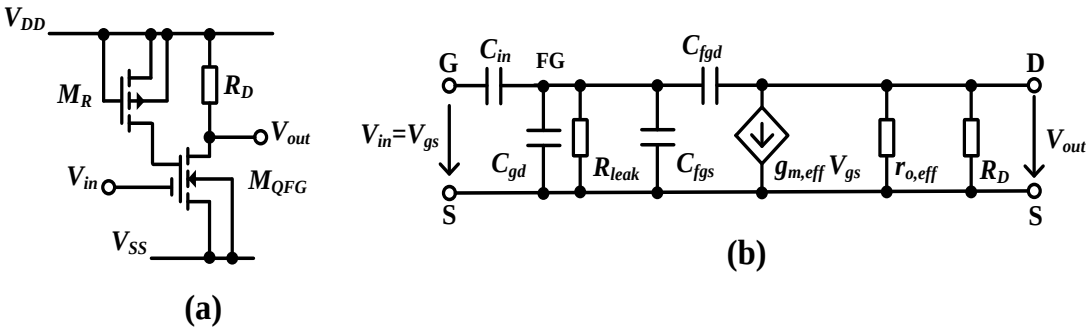


Fig. 2.18. Quasi–floating–gate MOST: (a) common source amplifier with single input terminal, (b) small signal model equivalent of (a).

The effective transconductance of QFG MOST is larger than the effective transconductance of FG–MOST but, it is still smaller than the transconductance of conventional GD MOST. It is given by:

$$g_{m,eff} = \frac{C_{in}}{C_{Total}}\, g_m\,, \tag{2.43}$$

where g_m is the transconductance seen from the floating gate.

To calculate transition frequency of QFG MOST, let's consider the AC circuit and its small signal equivalent circuit in Fig. 2.19:

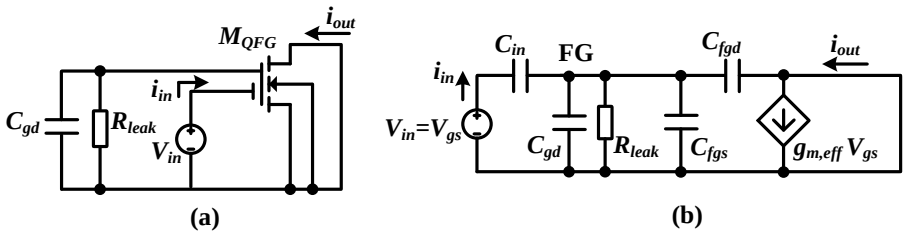


Fig. 2.19. Circuit to calculate transition frequency of QFG MOST: (a) ac schematic, (b) small signal equivalent circuit.

Assume that R_{leak} is extremely large, then the small signal input current is:

$$i_{in} = s\left[\frac{C_{in}(C_{gd}+C_{fgs}+C_{fgd})}{C_{Total}}\right]v_{gs}. \tag{2.44}$$

If the current through C_{fgd} is neglected then:

$$i_{out} \approx g_{m,eff}\,v_{gs}. \tag{2.45}$$

From (2.44) and (2.45) the current gain can be found:

$$\frac{i_{out}}{i_{in}} = \frac{g_{m,eff}}{s\left[\frac{C_{in}(C_{gd}+C_{fgs}+C_{fgd})}{C_{Total}}\right]}. \tag{2.46}$$

By following the same steps that were done previously, then the transition frequency equation of QFG–MOST is:

$$f_{T,QFG} = \frac{g_{m.eff}}{2\pi\left[\frac{C_{in}(C_{gd}+C_{fgs}+C_{fgd})}{C_{Total}}\right]}. \tag{2.47}$$

Assume that C_{fgs} is much greater than C_{fgd} and compensate the effective transconductance from (28), then the transition frequency can be expressed by:

$$f_{T,QFG} = \frac{g_m}{2\pi(C_{fgs}+C_{gd})}. \tag{2.48}$$

The input referred noise of the QFG MOST is similar in form to that of FG MOST, since the input signal path in both MOSTs is the same, then:

$$v_{noise,QFG}^2 = \left(\frac{C_{Total}}{C_{in}} \right)^2 v_{noise,GD}^2 . \quad (2.49)$$

As it is clear QFG MOST suffers from higher input referred noise than GD MOST, however, but on the other hand, the input referred noise of QFG MOST is smaller than it of FG MOST, since $C_{Total,QFG} < C_{Total,FG}$.

The effective output conductance of QFG MOST is greater than the output conductance of GD MOST, and it is given by the same form of the FG MOST conductance:

$$g_{ds,eff} = g_{ds} + g_m \frac{C_{fgd}}{C_{Total}} . \quad (2.50)$$

Advantages

1) No initial charge trapped at the floating gate.
2) Does not need a programming technique as FG MOST does.
3) Consumes smaller occupied chip area than FG MOST does.
4) The effective transconductance and transition frequency are relatively higher than the effective transconductance and transition frequency of FG MOST.

Disadvantages

1) Greater effective output conductance than the effective output conductance of FG MOST and the output conductance of GD MOST.
2) Floating gate voltage must not exceed the cut–in voltage of the p–n junction of the diode connected transistor M_R.
3) High–pass filters the applied signal.

2.1.2.4 Bulk–driven floating–gate and bulk–driven quasi–floating–gate approach

In fact, the BD, FG and QFG techniques are quite suitable for ultra LV LP applications mainly battery–powered implantable and wearable medical devices. Even though these non–conventional techniques offer design simplicity and good performance they still suffer from several drawbacks. The FG and QFG MOS transistors have lower transconductances and transient frequency values than the conventional gate–driven (GD) MOST [78]. Regarding the BD MOST it has much lower transconductance and transient frequency values than the conventional GD MOST [93, 94].

Therefore, novel techniques BD–FG MOST and BD–QFG MOST were introduced by Khateb [95–97], these techniques appear as attractive approaches to overcome the above mentioned drawbacks of the BD, FG and QFG techniques.

Fig. 2.20 shows the symbols of the novel BD–FG MOST (a) and BD–QFG MOST (b), whereas Fig. 2.21 shows the possible realization in MOS technology. The idea of utilizing the BD–FG and BD–QFG MOSTs came from the necessity of increasing the total

transconductance and the transient frequency of the FG and QFG MOSTs for applications requiring these features.

As shown in Fig. 2.20 (a) the BD–FG MOST is obtained by connecting the input–gate "G_{in}" with the bulk–terminal "B" of the FG MOST and the bias–gate "G_{bias}" must be connected to a suitable bias voltage. In case of BD–QFG MOST as shown in Fig. 2.20 (b) the input–gate "G_{in}" is also connected to the bulk–terminal "B" of the QFG MOST and the bias–gate "G_{bias}" must be connected to a suitable bias voltage through a large resistor "R_{Large}" which is practically realized by MOST operating in the cutoff region as shown in Fig. 2.21 (b).

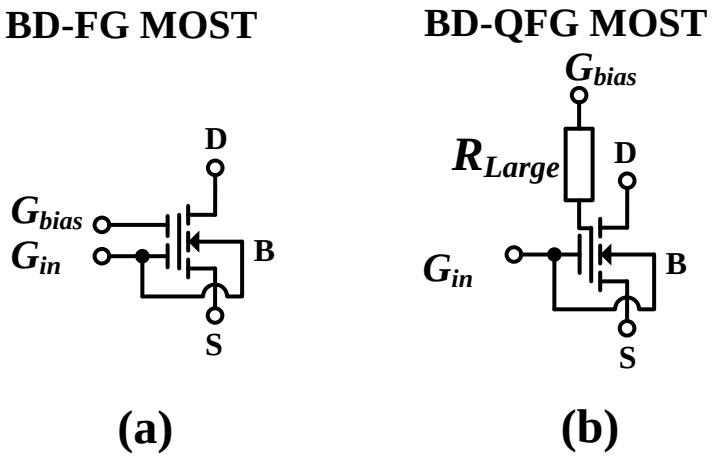


Fig. 2.20. Symbols of the BD–FG MOST (a) and BD–QFG MOST (b).

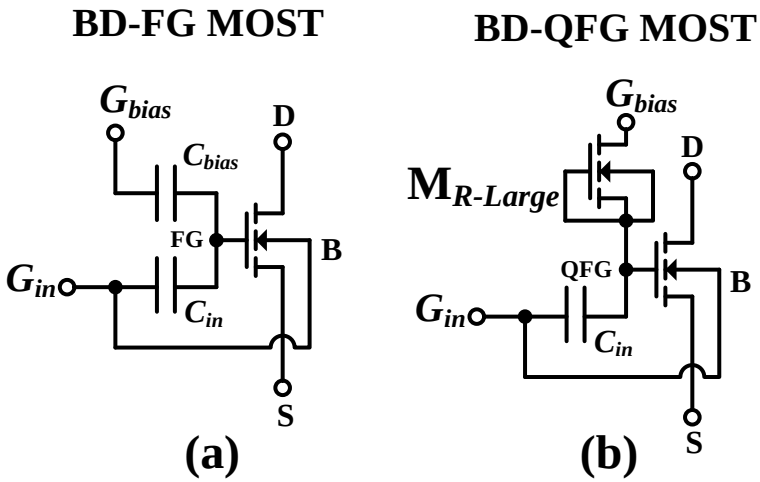


Fig. 2.21. Realization in MOS technology for BD–FG MOST (a) and BD–QFG MOST (b).

Assuming that the "S" terminals of BD–FG and BD–QFG MOSTs at Fig. 2.21 are grounded then their small–signal models are presented in Fig. 2.22 (a) and (b), respectively.

As the signal is applied to the bulk contact, the threshold voltage obstruction no longer appears in the signal path and the common mode range is extended. In this manner, it is possible to expand the applicability of any analog cell to extremely LV environments.

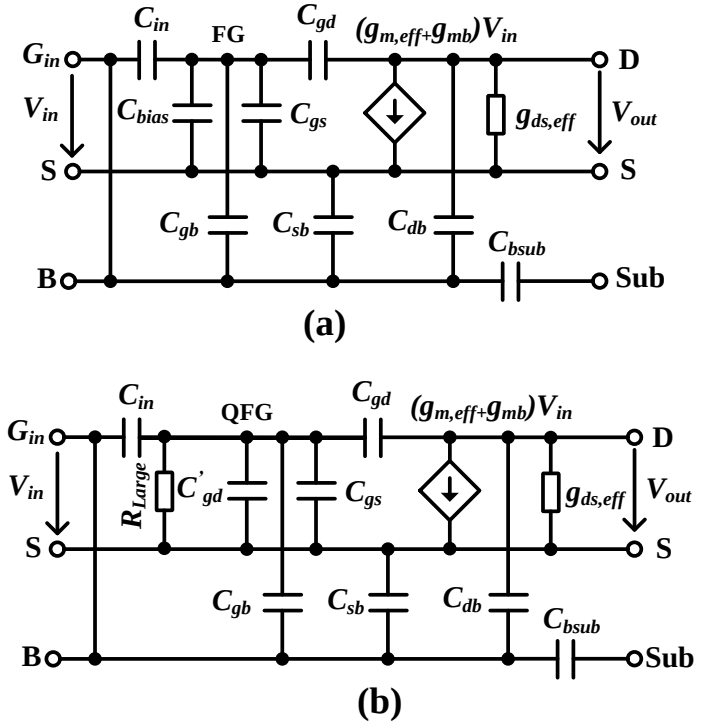


Fig. 2.22. Small–signal models for BD–FG and BD–QFG MOSTs.

The output conductance of BD–FG and BD–QFG MOST is given by:

$$g_{ds,BD-FG,BD-QFG} \approx \frac{C_{gd}}{C_{total}} g_m + g_{ds} . \tag{2.51}$$

The transconductance of BD–FG and BD–QFG MOST is given by:

$$g_{m,BD-FG,BD-QFG} = g_{m,eff} + g_{mb} \approx (0.7-1) g_m . \tag{2.52}$$

By following the same steps that were done previously, the transition frequency equation of BD–FG and BD–QFG MOST is:

$$f_{T,BD-FG,BD-QFG} \approx \frac{g_{m,BD-FG,BD-QFG}}{2\pi(C_{bs} + C_{bsub} + C_{gs})} . \tag{2.53}$$

From (2.52) and (2.53), it is clear that the BD–FG and BD–QFG MOSTs offer better parameters than the BD, FG and QFG MOSTs. Both transconductance and transient frequency are increased. However, the parasitic capacitance between the “B” and substrate “Sub” terminal i.e. C_{bsub} degrades the transient frequency of the BD–FG and BD–QFG

MOSTs. Therefore, for applications that require high transient frequency the Silicon on Insulator SOI technology should be used rather than bulk CMOS one.

It is worth mentioning here that that total capacitance seen from the floating–gate MOST is higher than the one seen from quasi–floating–gate, because the value of C_{bias} in FG is usually larger than gate–drain parasitic capacitance of the $M_{R-Larage}$ in QFG. This results in the transconductance of the QFG MOST being larger than FG MOST, also the transconductance of the BD–QFG MOST is larger than BD–FG MOST.

Advantages

1) Higher transconductance and transient frequency than other non–conventional low–voltage techniques.
2) Can process DC and AC signals.
3) Low supply voltage requirements and power consumption.
4) Threshold voltage requirement is completely removed from the signal path.
5) Rail–to–rail voltage swing capability.

Disadvantages

1) Lower transconductance, transient frequency and output impedance than gate–driven MOST.
2) When V_{BS} is critically large (more than the turn–on voltage of the bulk–channel PN junction diode), latch–up incurs.
3) BD–FG MOST consumes larger silicon area compared with the MOS transistor due to the added input capacitors and traps uncertain amount of charge might remain at the FG during fabrication.
4) In BD–QFG the FG voltage must not exceed the cut–in voltage of the p–n junction of the diode connected transistor M_R.

2.1.2.5 Comparison between non–conventional low–voltage techniques

Tab. 2.2 shows relations for transconductance, threshold voltage, output conductance, and transient frequency of the GD, BD, FG, QFG, BD–FG and BD–QFG MOSTs operating in saturation region [98].

Tab. 1.2. Relations of transconductance, threshold voltage, output conductance and transient frequency for GD, BD, FG, QFG, BD–FG, and BD–QFG MOSTs operating in saturation region.

	Transconductance	**Output conductance**	**Threshold voltage**	**Transient frequency**
GD	$g_m = K\frac{W}{L}(v_{gs} - V_T)$	$g_{ds} = \lambda I_{ds}$	$V_T = V_{T0} \pm \gamma\left(\sqrt{2\lvert\phi_F - v_{bs}\rvert} - \sqrt{2\lvert\phi_F\rvert}\right)$	$f_T \approx \frac{g_m}{2\pi C_{gs}}$
BD	$g_{mb} = \frac{C_{BC}}{C_{GC}} g_m \approx (0.2-0.4) g_m$	$g_{ds} = \lambda I_{ds}$	removed	$f_{Tb} \approx \frac{g_{mb}}{2\pi(C_{bs} + C_{bsub})} \approx (0.3-0.5) f_T$
FG & QFG	$g_{m,eff} = \frac{C_{in}}{C_{total}} g_m \approx (0.5-0.6) g_m$	$g_{ds,eff} = \frac{C_{gd}}{C_{total}} g_m + g_{ds}$ increased	$V_{T,FG,QFG} = \frac{V_T - V_{bias} k_2}{k_1}$ reduced or removed *here:* $k_1 = \frac{C_{in}}{C_{total}}$ and $k_2 = \frac{C_{bias}}{C_{total}}$	$f_{T,FG,QFG} \approx \frac{g_{m,eff}}{2\pi C_{gs}} \approx (0.5-0.6) f_T$
BD–FG & BD–QFG	$g_{m,BD-FG,BD-QFG} = g_{m,eff} + g_{mb} \approx (0.7-1) g_m$	$g_{ds,BD-FG,BD-QFG} \approx \frac{C_{gd}}{C_{total}} g_m + g_{ds}$ increased	removed	$f_{T,BD-FG,BD-QFG} \approx \frac{g_{m,BD-FG,BD-QFG}}{2\pi(C_{bs} + C_{bsub} + C_{gs})} \approx (0.7-0.9) f_T$

where:

C_{sb}	Source–bulk parasitic capacitance	V_T	Threshold voltage
C_{gb}	Gate–bulk parasitic capacitance	C_{gs}	Gate–source parasitic capacitance
C_{GC}	Total gate channel parasitic capacitance	C_{BC}	Total bulk channel parasitic capacitance
C_{total}	Total capacitance seen from the floating–gate/quasi–floating–gate of the FG–MOST/QFG–MOST	V_{T0}	Threshold voltage at V_{bs}=0
C_{gd}	Gate–drain parasitic capacitance	V_{bs}	Bulk–source voltage
C_{bsub}	Bulk–substrate parasitic capacitance	γ	Bulk–threshold parameter
C_{db}	Drain–bulk parasitic capacitance	K	Transconductance parameter
C_{in}	Input capacitance between FG/QFG and input terminal of the FG–MOST/QFG–MOST	Φ_F	Surface potential
C_{bias}	Bias capacitance between FG– and bias terminal of the FG–MOST	λ	Channel length modulation coefficient
f_T	Transient frequency	$g_{m,eff}$	Effective transconductance of the FG–MOST/QFG–MOST
g_m	Gate transconductance	g_{ds}	Output conductance
g_{mb}	Bulk transconductance	$g_{ds,eff}$	Effective output conductance of FG–MOST/QFG–MOST
R_{Larage}	Gate–drain resistance of $M_{R–Larage}$,	C'_{gd}	Gate–drain parasitic capacitance of $M_{R–Larage}$

To demonstrate a comparison study between the non–conventional techniques, Fig. 2.23 shows a principle of the common–source amplifier based on a GD MOST (a), BD MOST (b), FG MOST (c), and QFG MOST (d), BD–FG MOST (e) and BD–QFG MOST (f), as an example.

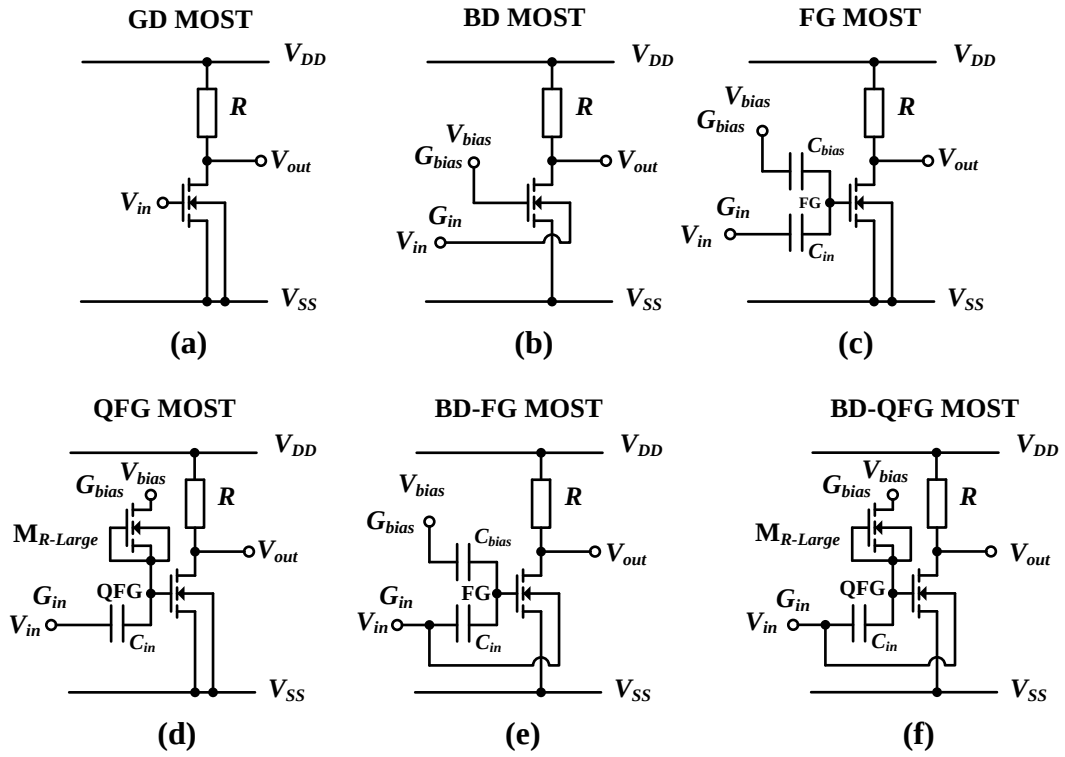


Fig. 2.23. Common–source amplifier based on: conventional GD (a), BD (b), FG (c), QFG (d), BD–FG (e), and BD–QFG (f) MOSTs.

Fig. 2.24 shows the drain currents versus gate–source of GD MOST, bulk–source of BD MOST, gate–source of FG–MOST, gate–source of QFG–MOST, gate–bulk–source of BD–FG–MOST and BD–QFG–MOST voltages of N–MOSTs from Fig. 2.24. It is obvious that the drain current in a conventional GD MOST increases when the gate–source voltage exceeds the threshold voltage. In bulk–driven MOST, the gate–source voltage is biased on a constant voltage V_{bias} and the input signal V_{in} is applied at the bulk–terminal, thus the threshold voltage in this set–up is removed from the signal path. In the FG–MOST and QFG–MOST, the bias–gate is set on bias voltage whereas the input–gate is used for the input signal; here the threshold voltage could be decreased or completely removed from the signal path. For BD–FG MOST and BD–QFG MOST the threshold voltage is completely removed from the signal path and the transconductance value is closed or slightly lower to the conventional MOST.

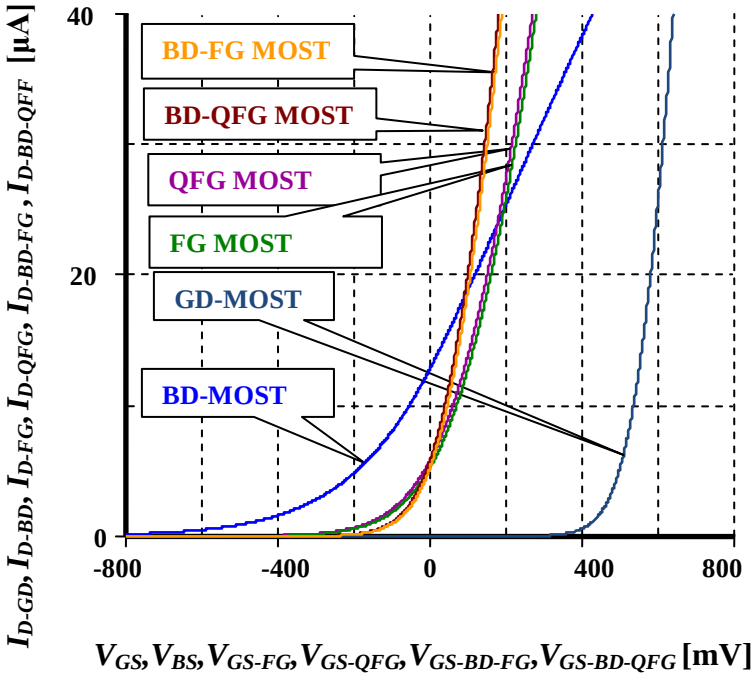


Fig. 2.24. Drain currents versus gate–source of GD MOST, bulk–source of BD MOST, gate–source of FG–MOST, gate–source of QFG–MOST, gate–bulk–source of BD–FG–MOST and BD–QFG–MOST voltages of N–MOSTs from Fig. 2.23.

It is worth noting that the models of FG MOST and BD–FG MOST are based on connecting high value resistors in parallel with the input capacitors as presented in [99].

2.2. SUB–CONCLUSION

To achieve low–voltage low–power capability, we have to utilize either developed technologies or design techniques. Developed technologies are out of the scope of this thesis. Both conventional and non–conventional design techniques have advantages and drawbacks. Examples of these advantages and disadvantages include, but not limited to, the following: rail–to–rail operating range circuits with acceptable signal–to–noise ratio but suffer from complexity to obtain a constant transconductance value. Sub–threshold circuits have low biasing currents but have very low transition frequency. Level shifter technique offers low input resistance and high bandwidth but suffers from the offset current. Self–cascode structure offers similar to a regular cascode but suffers from limited input common mode range and small output swing. Bulk–driven MOSTs offer better linearity and larger input common mode range but suffer from limited gain and cut–off frequency. Floating–gate MOSTs offer good linearity and rail–to–rail operation but consume much larger silicon area and have smaller output impedance, as well as they need a programming technique to get rid of the trapped charge in the floating gate. Quasi–floating–gate MOSTs do not consume much larger silicon area and do not need a programming technique as floating–gate MOSTs do, but they high–pass filter the applied signal. Bulk–driven floating–gate and bulk–driven quasi–floating–gate combine the most advantages of bulk–driven, floating–gate and quasi–floating–gate technique, but concurrently combine some disadvantages of them.

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3. THESIS OBJECTIVES AND RESULTS

In the last decade, many low–voltage low–power configurations have been introduced in the literature, but there is still some headroom for creativity since the domain of low–voltage low–power circuits' applicability is rather wide.

In references there are plenty of examples of analog basic building blocks (such as differential operational amplifiers, current mirrors, current conveyors, operational transconductance amplifiers, voltage followers, converters, buffers, oscillators, multipliers, filters and more) implemented utilizing some of the LV LP techniques. Besides the conventional building blocks, over the course of past twenty years, designers have searched for new active elements for several reasons such as increasing the universality of the element, eliminating parasitic effects and minimizing the number of these elements in their applications. As a consequence, new circuit elements have appeared such as OTRA (Operational Trans–Resistance Amplifier), CDBA (Current Differencing Buffered Amplifier), CDTA (Current Differencing Transconductance Amplifier), CTTA (Current–Through Transconductance Amplifier) VDTA (Voltage Differencing Transconductance Amplifier), and others.

The main goal of this thesis is to design and simulate novel CMOS structures of basic building blocks and active elements so they can operate at very low power supply voltage levels (average of 0.6 V) and consume very low power (average of 20 μW) for 0.18 μm CMOS technology, extending common–mode dynamic range while preserving other characteristics acceptable for many applications.

In this chapter, I will implement and improve several types of circuits based on LV LP techniques and blocks. Moreover, in order to validate the functionality of active elements, they are further utilized in various interesting applications.

3.1. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

In the late sixties, The Radio Corporation of America (RCA), then General Electric (GE), came out with the Operational Transconductance Amplifier, hereafter called OTA. The name means essentially a controllable resistance amplifier. OTA is a key functional block used in many analog and mixed–mode circuits. It is a special case of ideal active element, and its implementation in IC form makes it indispensable today in discrete and fully integrated analog network design. The ideal OTA as shown in Fig. 3.1 can be considered as differential voltage–controlled current source (DVCCS); its transconductance "g_m" represents the ratio of the output current to the differential input voltage, i.e., $I_{out}/(V_1–V_2)$. This transconductance is used as a design parameter and it is usually adjustable by the amplifier bias current (I_{bias}). The benefit of this adjusting possibility is acquiring the ability of electronic orthogonal tunability to circuit parameters. It could be noted that tunability has a main role in integrated circuits, especially to satisfy a variety of design specifications. Thus OTA has been implemented widely in CMOS and bipolar and also in BiCMOS and GaAs technologies [1].

The OTA is similar to the standard operation amplifier (OPA) in the sense of infinite input impedances, but its output impedance is much higher, and that makes OTA more desirable than any ordinary amplifier. Recently, the multiple–output– OTA (MO–OTA) has been introduced and used, on par with the ordinary operation amplifier, as a basic block in many applications, particularly for realizing universal filters which are able to implement several second–order transfer functions with a minimum of adjustments. The literature provides numerous examples of OTA–based biquad structures, as well as active elements such as Current Conveyor (CC), Current Differencing Transconductance Amplifier (CDTA), Current–Through Transconductance Amplifier (CTTA), and Current–Conveyor Transconductance Amplifier (CCTA).

The symbol and the equivalent circuit of ideal OTA are shown in Fig. 3.1 (a) and (b) respectively [1].

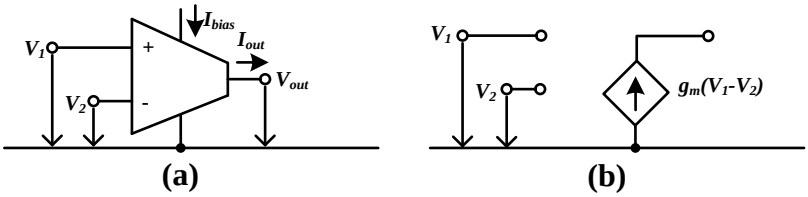


Fig. 3.1. Ideal operational transconductance amplifier, (a) symbol and (b) equivalent circuit.

Simple applications of the OTA include voltage amplification, Voltage–Variable Resistor (VVR), voltage summation, integration, gyrator realization, practical OTAs, current conveyor, and active RC filters. In addition, one of OTA's principal uses is in implementing electronically controlled applications such as variable frequency oscillators and variable gain amplifier stages which are more difficult to implement with standard OPAs.

3.1.1. Bulk–driven quasi–floating–gate operational transconductance amplifier (BD–QFG OTA)

A new LV LP BD–QFG OTA is presented. The proposed circuit is designed using 0.18 µm CMOS technology. The supply voltage of 0.6 V and the quiescent bias current of 5 µA are used. The PSpice simulation result shows that the power consumption of the proposed BD–QFG OTA is 13.4 µW. Thus, the circuit is suitable for low–power. Fig. 3.2 shows the proposed configuration.

The circuit is consisted of two stages. The first stage is consisted of a bulk–driven quasi–floating–gate differential input M_1 and M_2. The gates of these transistors are tied to the negative supply voltage V_{SS} through extremely high value resistors constructed by transistors M_{b1} and M_{b2} which are operating in cutoff region. The input terminals are connected to M_1 and M_2 from two sides: capacitively coupled to the quasi–floating gates via C_1 and C_2 from one side, and connected to bulk terminals from other side. Transistors M_4, M_5, M_6 and M_7 act

as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit. Transistors M_5 and M_6 form the active load and transistor M_3 acts as tail current source for the differential input stage. The input voltage terminals are connected to the bulk terminals of M_1 and M_2, therefore high input impedances are achieved.

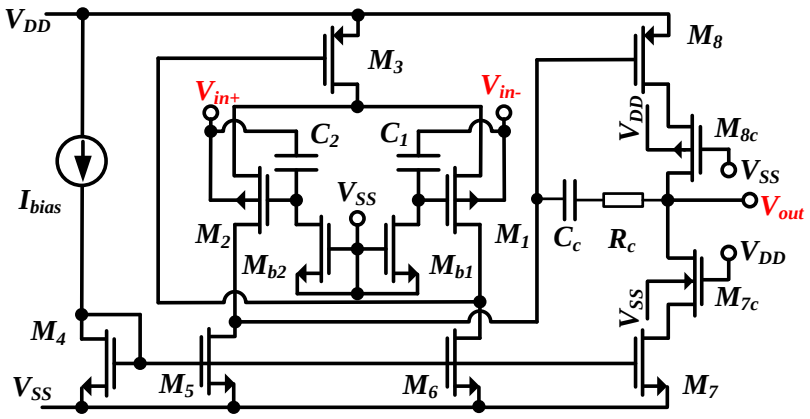


Fig. 3.2. The internal structure of BD–QFG OTA.

The use of bulk–driven quasi–floating–gate flipped voltage follower for the differential input stage makes the minimum power supply voltage $V_{DD\,(\min)}$. The supply voltage is given by:

$$V_{DD\,(\min)} = V_{GS\,(M3)} + V_{DS\,(M5)}. \tag{3.1}$$

Equation (3.1) shows the capability of the proposed BD–QFG OTA structure for operation under lower supply voltage.

The second stage is consisted of M_7, M_{7c} and M_8, M_{8c}. Cascode structure is used to implement the gain stage in order to provide significantly high–value output impedance, consequently to achieve high voltage gain. Output impedance can be calculated from the following equation:

$$r_o = \frac{1}{\frac{g_{o,M7}g_{o,M7c}}{g_{m,M7c}+g_{mb,M7c}} + \frac{g_{o,M8}g_{o,M8c}}{g_{m,M8c}+g_{mb,M8c}}}. \tag{3.2}$$

3.1.1.1 BD–QFG OTA–based diode–less precision rectifier

A precision rectifier is one of important nonlinear circuits extensively used in analog signal processing systems. In precision rectification, a bi–directional signal is converted to one–direction signal. Typically, a conventional rectifier could be realized by using diodes for it rectification, but diode cannot rectify signals whose amplitudes are less than the threshold voltage (approximately 0.7 V for silicon diode and approximately 0.3 V for germanium diode). As a result, diode–only rectifiers are used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers, but for applications requiring accuracy the range of threshold

voltage the diode–only rectifier cannot be used. This can be overcome by using integrated circuit rectifiers instead.

Traditional methods of realizing precision rectifier circuits include the use of operational amplifiers, resistors, and either diodes [16–20] or alternating source–followers [21]. A number of current conveyors–based current–mode rectifier circuits are existed in the literature [22–28]. The rectifier circuits in [22–24] employ diodes and resistors in addition to CCIIs. The circuit proposed in [25] employs bipolar current mirrors in addition to a CCII and a number of resistors. The rectifier circuit in [26] employs four CCCIIs and resistors. However, the use of resistor makes these circuits not ideal for integration. Therefore, precision rectifiers by using all–MOS transistors are proposed [29–38]. Authors in [39] proposed a circuit which employs two CCII and two MOS transistors. Authors in [41] presented a circuit which employs an amplifier and a simple voltage comparator. On the other hand, differential difference current conveyors–based current–mode rectifiers have recently seen the light since DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability). Thus, author in [39] presented a rectifier which employs two differential difference current conveyors (DDCCs). A new technique for realizing precision half–wave voltage rectifier in CMOS technology is proposed, this technique is based on bulk–driven quasi floating–gate operational transconductance amplifier (BD–QFG OTA).

Diode–less half wave rectifier based on bulk–driven quasi–floating gate OTA is shown in Fig. 3.3. This circuit is a WTA–like (winner take all) circuit. The principle of work is as follow: if we applied a voltage signal to V_{in} terminal and a zero to V_{off} terminal, the output voltage would equal to the maximum voltage of both inputs. In other words, the positive half of the signal wave is passed, while the other half is blocked. For an input voltage V_{in} the ideal half–wave rectified output V_{out} is given by:

$$V_{out} = \begin{cases} V_{in} & if\ V_{in} > 0 \\ 0 & otherwise \end{cases}. \tag{3.3}$$

It is worth mentioning that the same configuration shown in Fig. 3.3 could be used as full–wave rectifier just by applying $-V_{in}$ (an identical signal of V_{in} shifted 180°) to V_{off} terminal.

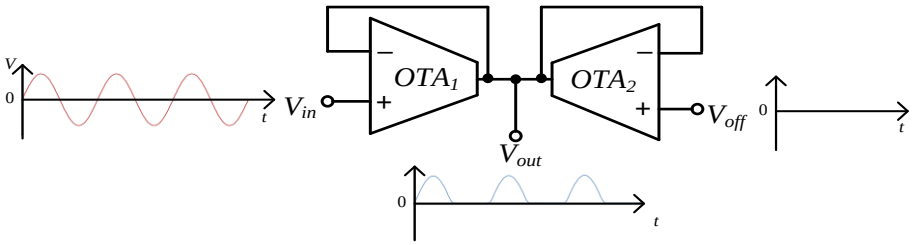


Fig. 3.3. BD–QFG half–wave rectifier.

3.1.1.2 Simulation results

The proposed BD–QFG OTA was designed and simulated using TSMC 0.18 μm *N*–well CMOS. The used PSpice model is available on [41]. The supply voltage was ±0.3 V, the biasing current was I_{bias} = 5 μA and the power consumption was 13.4 μW. The optimal transistor aspect ratios and the values of components are given in Tab. 3.1. Tab. 3.2 shows a list of measured operational amplifier benchmarks used to evaluate proposed OTA. Features of the circuit (shown in Fig. 3.2) are listed in the first column, along with values of other works listed in other columns.

Fig. 3.4 shows the simulated magnitude of output impedance of OTA. Z_{out} is high as expected; its value is 7.83 MΩ. The AC gain and phase responses of the BD–QFG OTA with 3 pF load capacitance are shown in Fig. 3.5. The open–loop gain is 80 dB and the gain–bandwidth product is 6.4 MHz. The phase margin is 65º which guarantees the circuit stability. The voltage follower frequency response of the proposed circuit, which obtains 15 MHz, is shown in Fig. 3.6.

Tab. 2.1. Transistors aspect ratios for Fig. 3.2.

BD–QFG OTA	**W/L [μm/μm]**
M_1, M_2	20/0.3
M_{b1}, M_{b2}	30/2
M_3, M_8	100/0.3
M_4 , M_5, M_6	4/0.3
M_7	8/0.3
M_{7c}	45/2
M_{8c}	100/2
C_1= C_2=0.4 pF	
R_c= 10 kΩ, C_c = 3 pF	

Tab. 3.2. BD–QFG OTA performance benchmark indicators.

Parameters		**Proposed OTA**	**Koziel [105]**	**Majumdar [106]**	**Li [107]**	**Zhang [108]**
CMOS Technology	[µm]	0.18	0.5	0.35	0.35	0.18
Power supply	[V]	± 0.3	± 2.5	3.3	3.3	1.8
Power consumption	[µW]	13.4	6800	3370	2330	590
Transistors number	[/]	12	37	14	22	68
AC Gain	[dB]	51	65	80.4	65	55
Linearity range	[mV]	± 0.3	± 0.75	± 0.1	/	± 0.27
Output resistance	[MΩ]	0.317	3.4	/	1.2	8.3
–3dB bandwidth	[MHz]	59	100	123.2	100	200

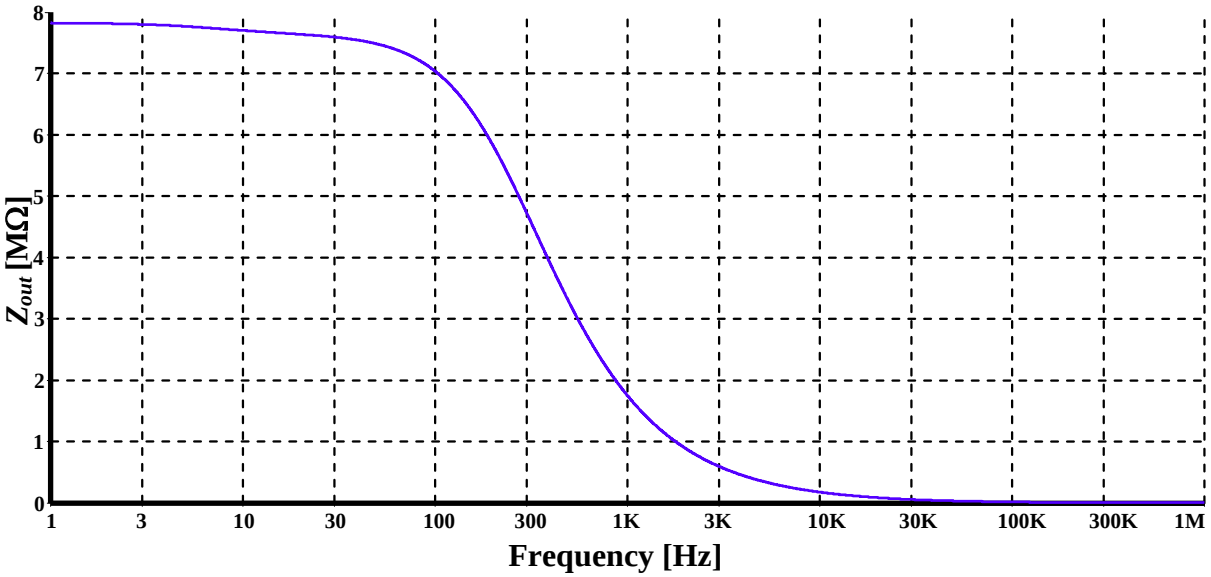


Fig. 3.4. Output impedance versus frequency.

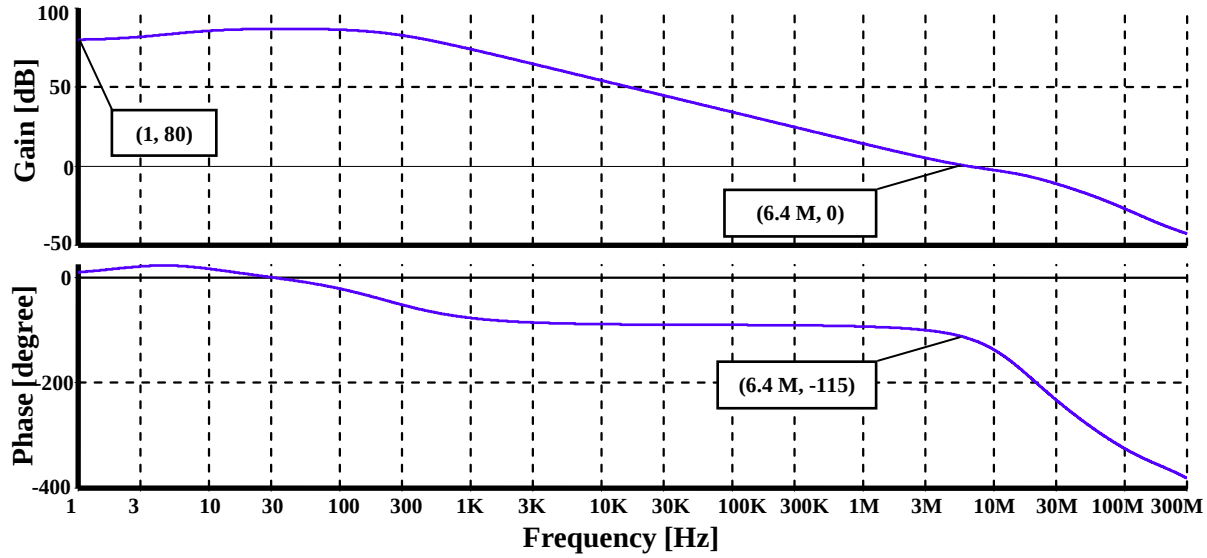


Fig. 3.5. Frequency response of BD–QFG OTA.

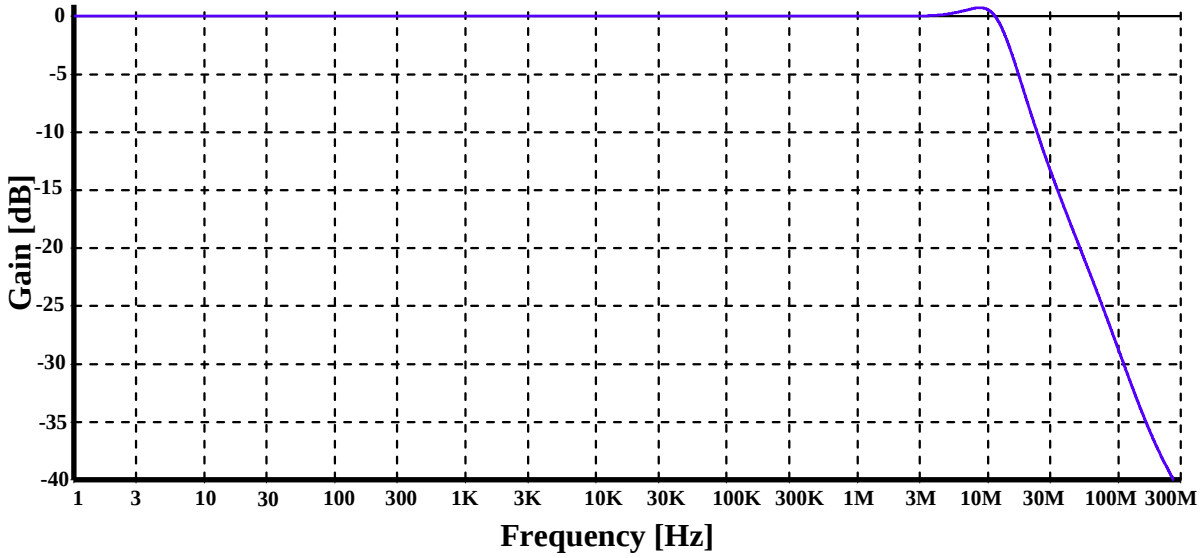


Fig. 3.6 Frequency response of OTA as a voltage follower.

Fig. 3.7 presents the DC transfer characteristic of the BD–QFG OTA. For input voltage range from –266 to 266 mV the voltage error is below 4 mV, out of this range this error is increased. Therefore, using V_{off} = 0 V and maximum input amplitude $V_{m.max}$ of ±250 mV, the OTA is not expected to have strong impact to the overall rectifier accuracy.

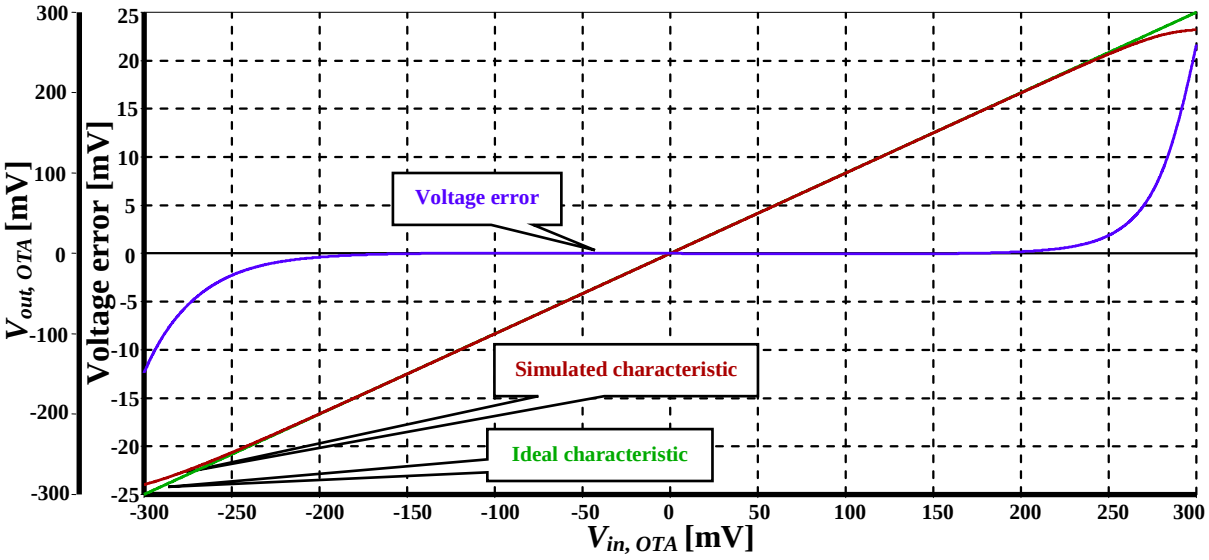


Fig. 3.7. DC transfer characteristic and voltage error of the BD-QFG OTA of Fig. 3.2.

The diode–less half–wave precision rectifier shown in Fig. 3.3 was simulated using BD–QFG OTA shown in Fig. 3.2. The supply voltage of ±0.3 V and the bias current of I_{bias} = 5 µA for OTAs were used. The circuit consumes 26.8 µW. Fig. 3.8 shows the DC transfer characteristic of BD–QFG half–wave rectifier in comparison with the ideal one and it confirms the precise rectification for input amplitude ranging ±250 mV.

Fig. 3.9 shows the transient response of the output waveforms for input signal of 15 kHz and amplitudes from 50 mV to 125 mV with step of 25 mV. It is obvious from that the rectifier is capable to rectify a wide range of amplitudes. Fig. 3.10 shows the transient responses of the input and output waveforms with amplitude 100 mV and frequency 10 kHz, 20 kHz, 30 kHz, 40 kHz and 50 kHz. The load capacitor C_{load} for measurements done in Fig 3.9 and Fig 3.10 was set to 5 pF.

To demonstrate the temperature performance of proposed circuit, the proposed circuit was simulated at the frequency of 10 kHz by changing temperature. Fig. 3.11 shows the output waveforms of the proposed rectifier at temperatures of 0 °C, 27 °C and 100 °C. From Fig. 3.11, it can be seen that the proposed circuit provides excellent temperature stability without any compensation technique.

To evaluate the quality of the rectification process as a function of the amplitude and the frequency of the input signal, two types of characteristics are proposed [74]. The type first is P_{AVR} (AVR=Average Value Ratio) which is the ratio of the average value of the rectified output signal v_{out} and the average value of the sinusoidal input signal after its ideal half–wave rectification:

$$P_{AVR} = \frac{\frac{1}{T}\int_0^{\frac{T}{2}} v_{(out)}.dt}{\frac{1}{\pi}V_m}. \qquad (3.4)$$

where T and V_m are the period and amplitude of the sinusoidal input signal. The ideal operation of the rectifier is then characterized by the value P_{AVR} = 1. With increasing the frequency and decreasing the amplitude of the input signal, the deviation from the ideal operation is indicated by a change, mostly a decrease in P_{AVR} below one.

The second type of characteristic is defined more rigorously as a ratio of two Root Mean Square "RMS" values, the RMS of the difference of the real and ideal output signals, v_{out} and v_{ideal}, and the RMS value of the ideal signal:

$$P_{RMSE} = \frac{\sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} [v_{out}(t) - v_{ideal}(t)]^2 \, dt}}{\frac{1}{2}V_m}. \tag{3.5}$$

Here, the suffix RMSE is an abbreviation of the term "Root Mean Square Error". For ideal circuit operation, i.e., $v_{out}(t) = v_{ideal}(t)$, the result is P_{RMSE} = 0, while in the case of total attenuation of the output signal P_{RMSE} = 1. For extra high distortions, when the mutual energy of signals v_{out} and v_{ideal} can be negative, one can obtain $P_{RMSE} > 1$. Fig. 3.12 shows the P_{AVR} (a) and P_{RMSE} (b) versus frequency in range of 10 kHz up to 500 kHz for three amplitudes of the input voltage (50, 100, 150) mV. As one can notice from the figure, over the full range of frequency, the value of P_{AVR} is ranging between 1 and 0.85 and the value of P_{RMSE} is below 0.1. The values of P_{AVR} and P_{RMSE} achieved confirm the quality of the rectification process of the proposed rectifier.

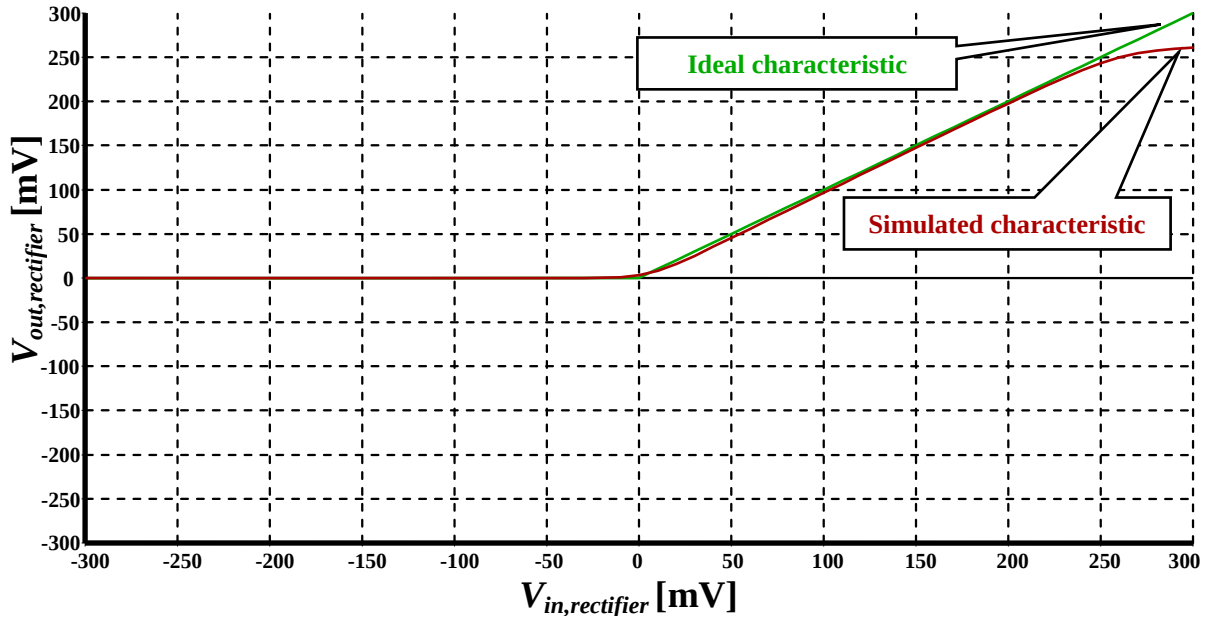


Fig. 3.8. DC transfer characteristic of BD-QFG Half-wave rectifier.

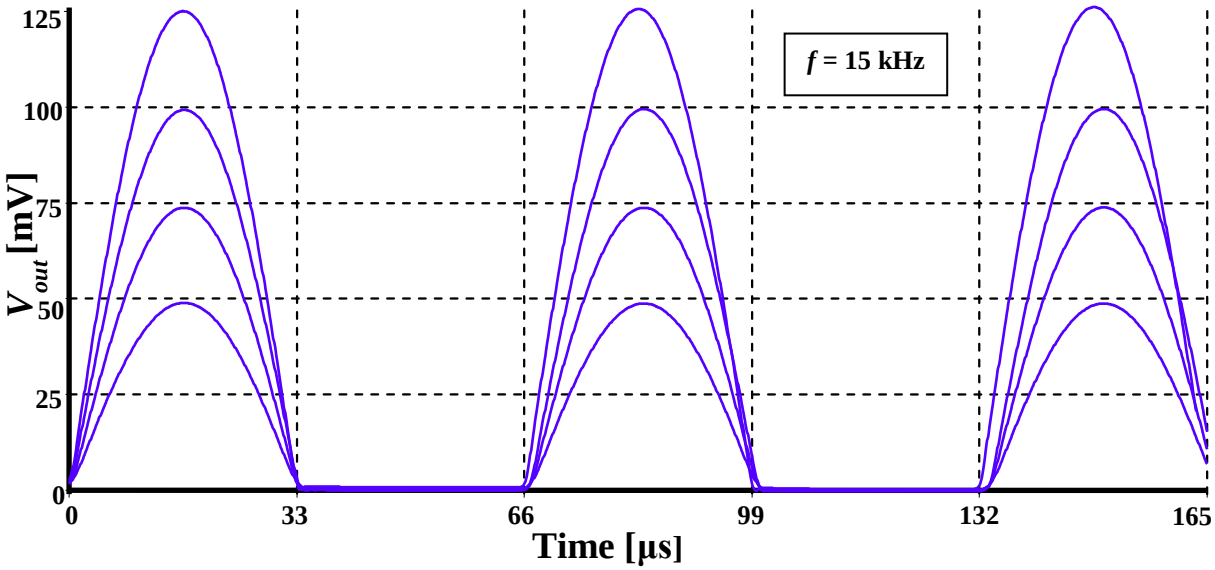
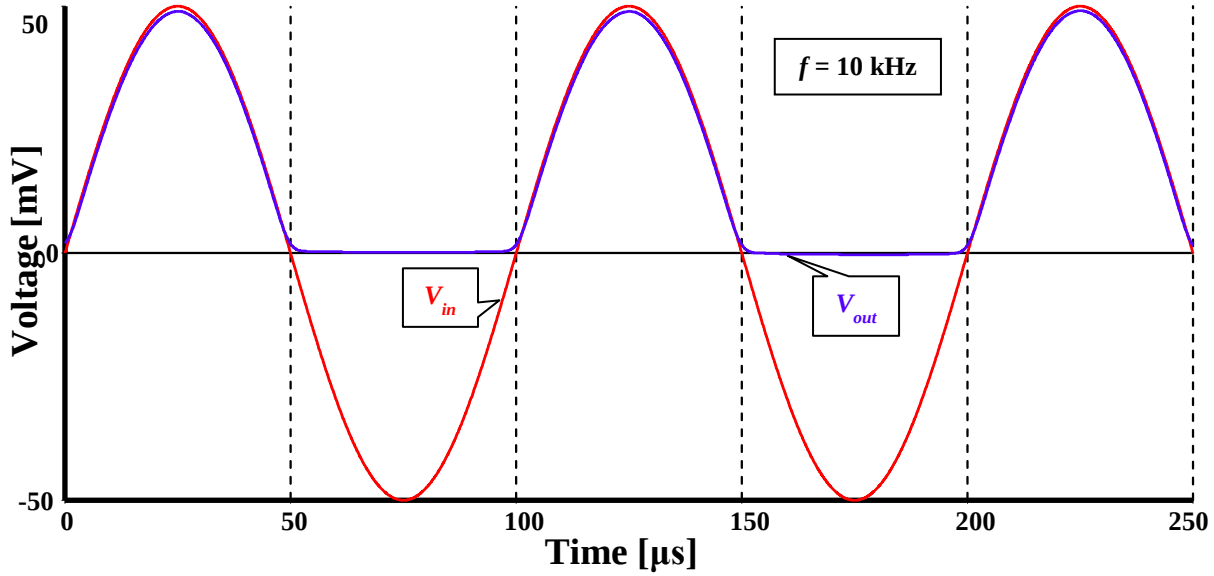
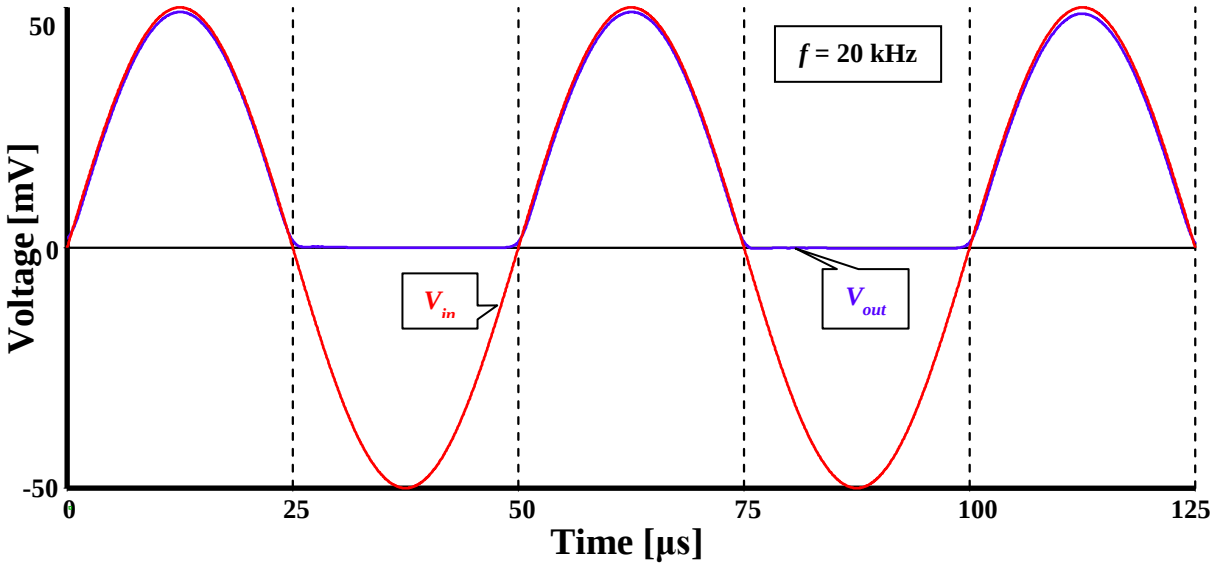


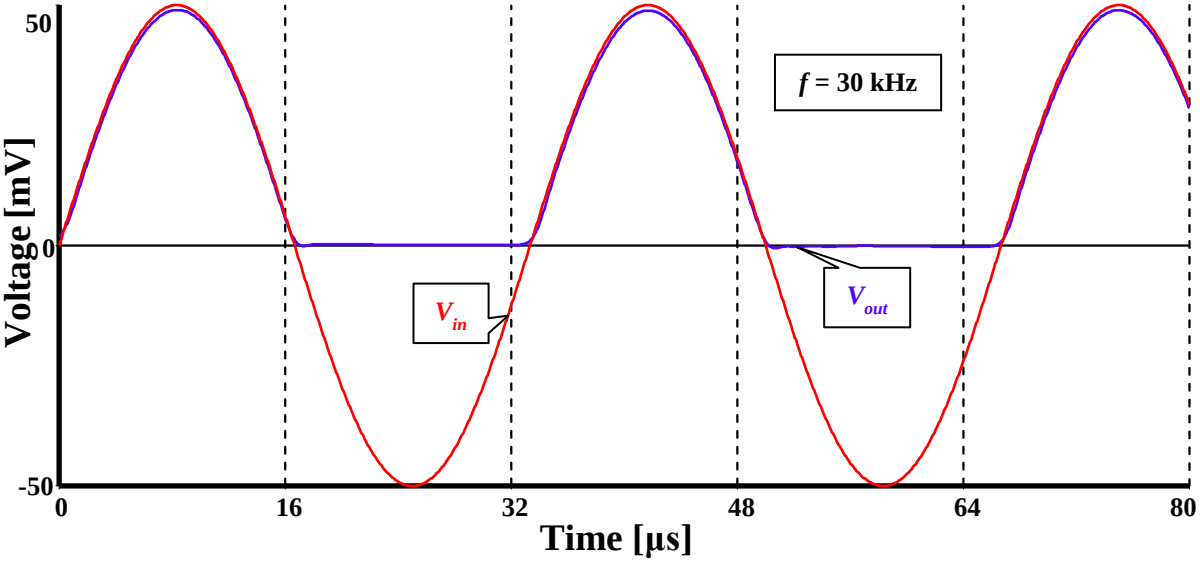
Fig. 3.9. Transient analyses of output waveforms with 15 kHz and various amplitudes of the input signal.



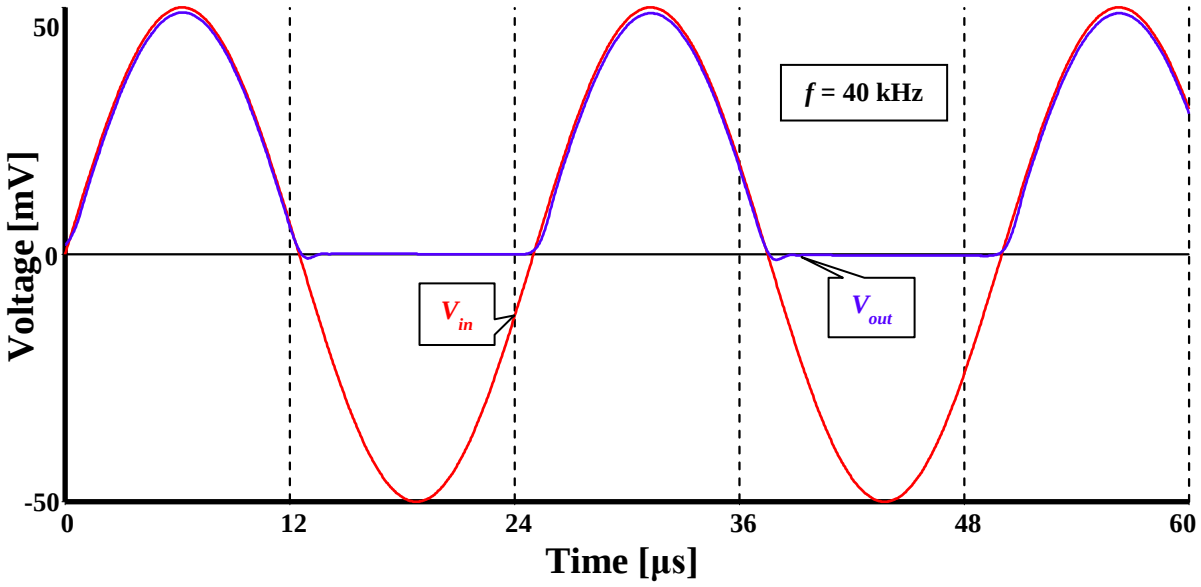
(a)


50
0
-50
Voltage [mV]
f = 20 kHz
V in
V out
0
25
50
75
100
125
Time [µs]

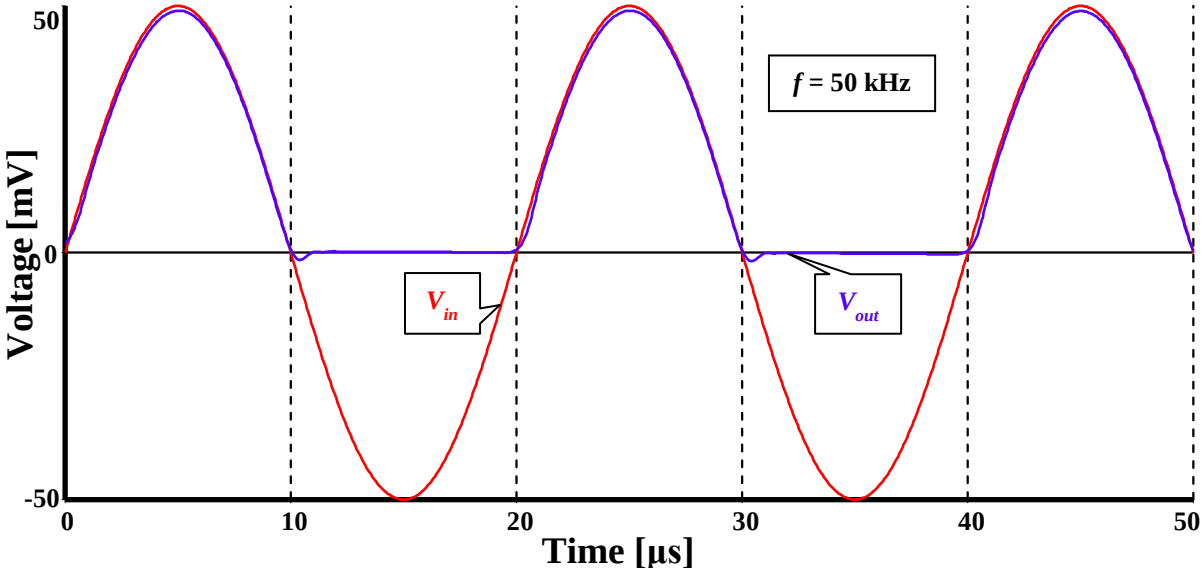
(b)


50
0
-50
Voltage [mV]
f = 30 kHz
V in
V out
0
16
32
48
64
80
Time [µs]

(c)



(d)



(e)

Fig. 3.10. Transient analyses of input and output waveforms with V_m= 50 mV and (a) 10 (b) 20 (c) 30 (d) 40 and (e) 50 kHz.

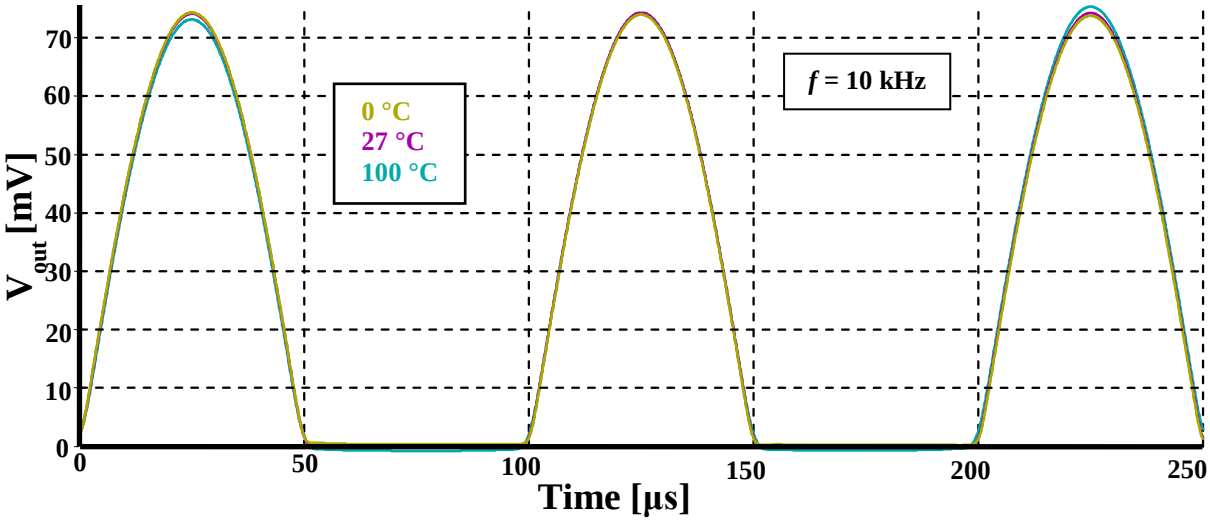
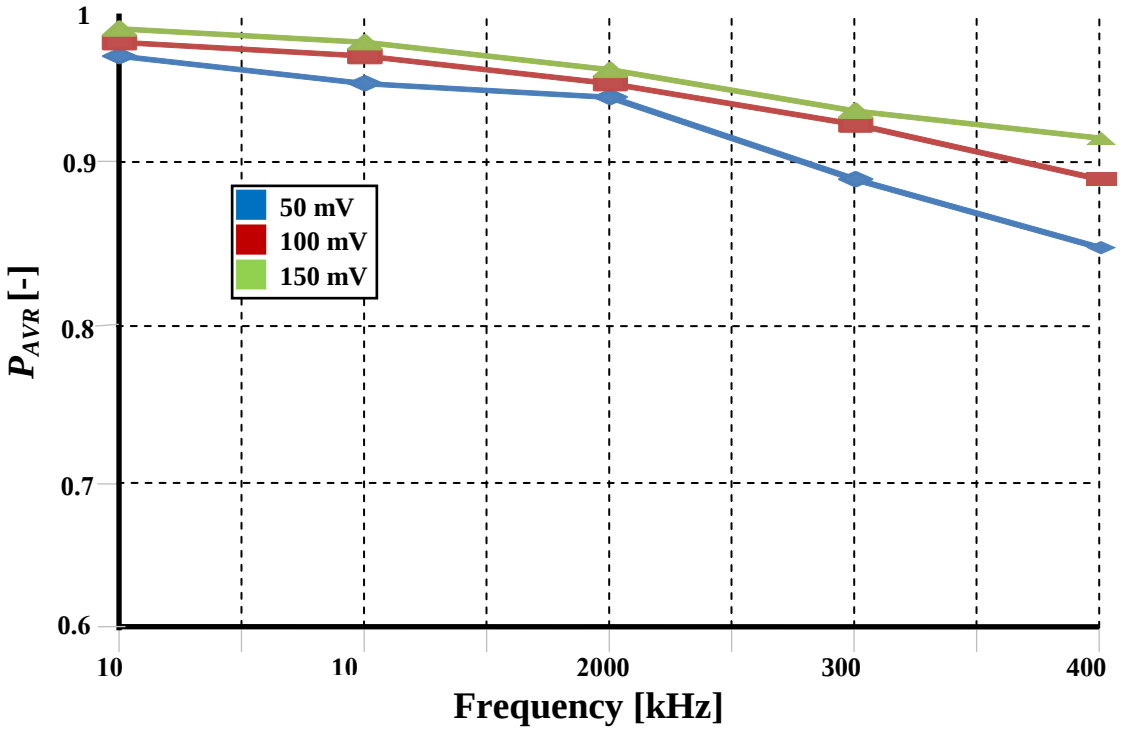
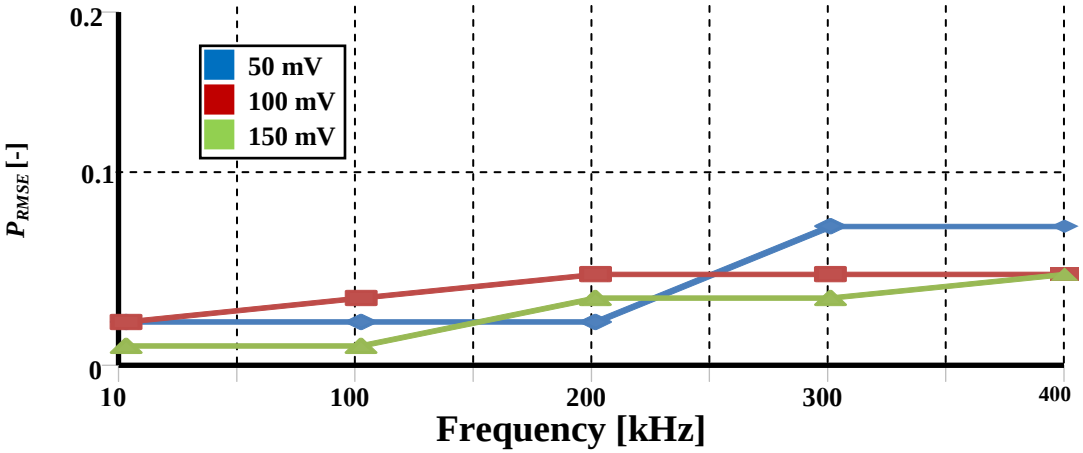


Fig. 3.11. Outputs waveforms at different temperatures.



(a)



(b)

Fig. 3.12. AVR (a) and RMSE (b) versus frequency for three amplitudes of the input voltage (50, 100, 150) mV.

3.1.2. Floating–gate operational transconductance amplifier (FG OTA)

A configuration of operational transconductance amplifier (OTA) based on floating–gate MOSTs for low–power, low–voltage, and low–frequency applications is presented. The circuit presented is a two–stage transconductance amplifier. The scheme uses *P*–channel floating–gate transistors at the input, M_1 and M_2, each with two gates. Of course, it is possible to use a complementary scheme with *N*–channel input transistors. As specified by the name, the circuit is the cascade of two stages: The first is a differential amplifier which consists of input devices M_1, M_2 and the current mirror M_3, M_4 which is acting as an active load, the second stage is a conventional inverter with M_5 as a driver and M_6 as an active load. See Fig. 3.13.

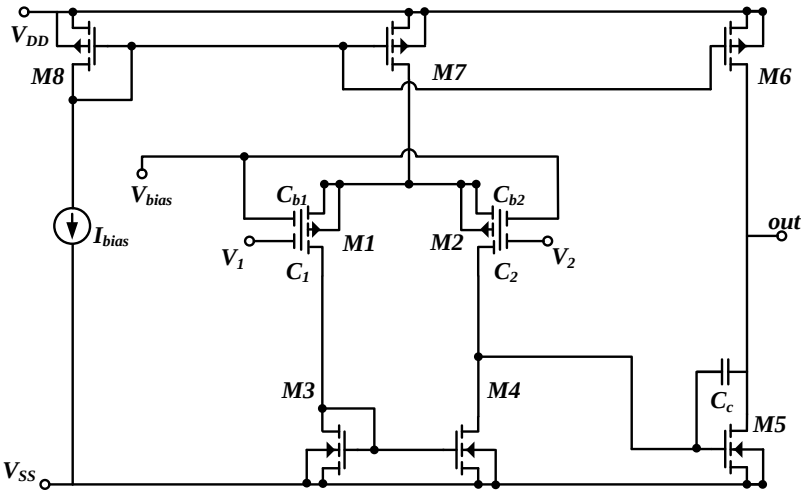


Fig. 3.13. The circuit of two–stage OTA using FG–MOSTs.

The current of M_1 is mirrored by M_3, M_4 and subtracted from the current comes from the drain of M_2, then the signal contributions of the two currents multiplied by the output

resistance of the first stage give the single–ended first stage output voltage. This resulting signal constitutes the input of the second gain stage.

It is important to notice that all transistors are working in the saturation area. Compensation capacitor C_C takes care of compensation requirements since it connects gain stage's output of the OTA with its input. By the means of C_C, the dominant (first) pole's frequency is shifted down from 100 kHz to 3 kHz. This action is named pole splitting, and it enhances the stability of the circuit since it affects phase margin (*PM*) value as explained in (3.6) [71]:

$$PM = \pm 180° - a\tan\frac{GBW}{|W_{P1}|} - a\tan\frac{GBW}{|W_{P2}|}, \tag{3.6}$$

where w_{p1} and w_{p2} are the angular frequencies of the first and second poles, respectively. Indeed, stability is paid for by a reduction in the gain bandwidth because lowering dominant pole's frequency would reduce it, but one has to take a decision here for some trade–off between the conflicting requirements of gain bandwidth and stability.

3.1.2.1 FG OTA based tunable voltage differencing transconductance amplifier (FG VDTA)

Tunable active circuit element VDTA (Voltage Differencing Transconductance Amplifier) based on floating–gate MOSTs is proposed in this section. The mentioned VDTA is brought as the convenient element for current mode signal processing, which might be very suitable for variety of applications such as biquad filters since the circuit has the advantage of being tunable. VDTA is supposed for usage mostly in current mode circuits but it is also good choice in case of voltage mode and/or hybrid (voltage–current) circuits as well. This active circuit element is a type of analog block consists of two multiple–output operational transconductance amplifiers (MO–OTAs) using floating–gate MOSTs as input stage. The internal structure of the VDTA is shown in Fig. 3.14.

Output current of input stage flows out of the VDTA terminal "z" into an outside load if desired. The voltage across the z–terminal is converted through a transconductance g_{mx} into two or more output currents with opposite polarity. To increase the universality of the element, it is completed of the I_z copy, this attribute can be implemented by several methods, and the one addressed in [72] is adopted.

To further increase the versatility of the configuration, it is designed to allow orthogonal tuning capability through transconductance control by the amplifier bias current (I_{bias}) of each OTA, the main component of the proposed circuit. The VDTA can be remarkably used in filters; it can implement low–pass, band–pass, high–pass, band–notch, and all–pass filters.

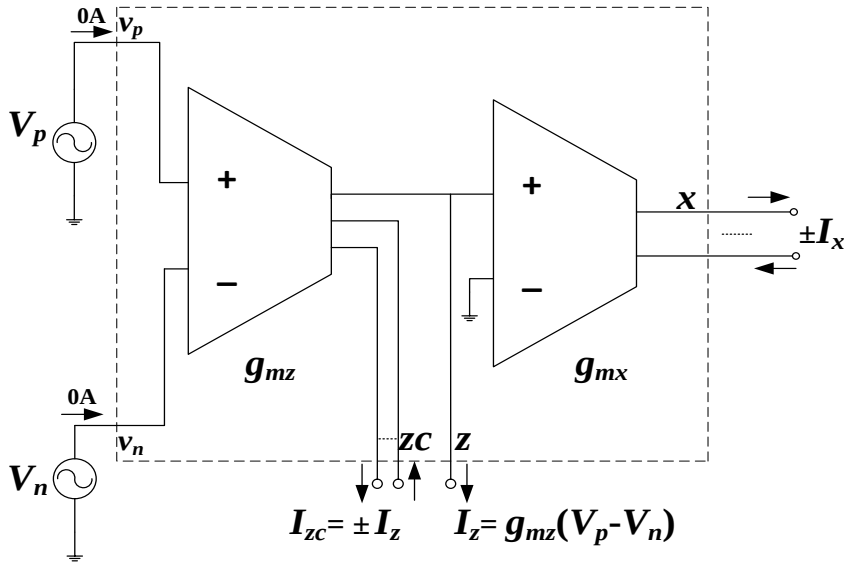


Fig. 3.14. VDTA element as a connection of two MO–OTAs.

As an application example of the proposed FG VDTA, a biquad filter is implemented as shown in Fig. 3.15. [73]. Fig. 3.15 presents a SIMO OTA–C filter based on VDTA configuration.

Circuit analysis yields the following transfer functions:

$$I_{o1}=sC_2g_{m1}I_{in}/\Delta. \quad (3.7)$$

$$I_{o2} = g_{m1}g_{m2}I_{in}/\Delta. \quad (3.8)$$

Where:

$$\Delta = s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}. \quad (3.9)$$

Thus:

- Band–pass function is obtained from I_{o1}.
- Low–pass function is obtained from I_{o2}.

The resonance angular frequency ω_o and the quality factor Q of proposed network is given by:

$$\omega_o = (g_{m1}g_{m2}/C_1C_2)^{1/2}. \quad (3.10.a)$$

$$\omega_o/Q = g_{m1}/C_1. \quad (3.10.b)$$

But $C_1 = C_2$ and $g_{m1} = g_{m2}$ as mentioned earlier. By substituting in (3.10) we obtain:

$$\omega_o = g_{mx}/C_x, \quad (3.11.a)$$

where $x = 1$ or 2.

$$Q = 1. \quad (3.11.b)$$

It is obvious from (3.11.b) that quality factor Q has no sensitivity to passive components and that gives the designer a margin of freedom in designing progress.

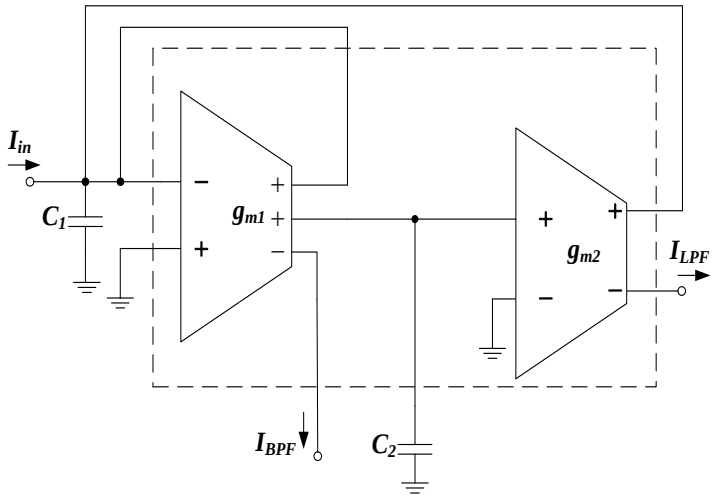


Fig. 3.15. Single–input multiple–output biquad filter based on FG VDTA.

3.1.2.2 Simulation results

Tab. 3.3 summarizes the performance of OTA in proposed VDTA. It is clear from Tab. 3.3 that the circuit is stable with phase margin of 83◦, which is an important factor in determining the efficiency of the circuit. A point that is worthwhile underlining is that the configuration offers rail–to–rail voltage capability at a low supply voltage of ±0.5 V.

The measurement results of the transconductance of OTA for five values of I_{bias} are presented in Tab. 3.4. Component values are given in Tab. 3.5, transistor aspect ratios as well as their biasing currents are given in Tab. 3.6. Results in Tab. 3.5 are taken under the condition I_{bias} = 10 μA. Tab. 3.7 shows a list of measured operational amplifier benchmarks used to evaluate proposed OTA. Features of the circuit (shown in Fig. 3.13) are listed in the first column, along with values of other works listed in other columns.

The AC gain and phase responses of the FG OTA with 1 pF load capacitance are shown in Fig. 3.16. The open–loop gain is 51 dB and the gain–bandwidth product is 3.15 MHz. The phase margin is 80º which guarantees the circuit stability.

Fig. 3.17 shows simulated transient responses of the FG OTA. The input range has been determined with the OTA connected as a buffer, and a 10 kHz sinusoidal input signal, allowing a maximum total harmonic distortion (THD) at the output of 0.93%.

We notice from Fig. 3.17 that the configuration has rail to rail operation for 1V input signal, the negligible offset voltage has the very small value of 179 μV, and this unavoidable offset can be explained by offset contributions from transistor components, especially from differential pair and current mirror.

Fig. 3.18 shows the curve of Z_{out}, please observe the value of impedance at low frequency, which is R_{out}. The value of R_{out} is about 160 kΩ.

Tab. 3.3. Summary of the performance for OTA.

Characteristics	Simulated results
Voltage gain	51 dB
CMRR	61 dB
Offset voltage	176 μV
GBW	3.15 MHz
Phase margin	80◦
Power consumption	36 μW
Slew rate	4.35 V/μs
Settling time	670 ns
Input range	0.8 V_{pp} = 0.78 V_{DD}
Output impedance	160 kΩ

Tab. 3.4. Measurement results of the transconductance.

	Results of Transconductance g_m for Different Values of Bias Current I_{bias}				
I_{bias} [μA]	5	10	15	20	25
g_m [mA/V]	1.1	2	2.8	3.6	4.2

Tab. 3.5. Measurement conditions of the circuit.

Parameter	Value
C_{b1}, C_{b2}	0.3 pF
C_1, C_2	0.1 pF
C_c	1 pF
V_b	–0.3 V

Tab. 3.6. Transistors dimensions.

Device	Type	L/W [μm]	I_d [μA]
M_1, M_2	PMOS	0.2/10	2.3
M_3, M_4	NOMS	0.8/10	2.3
M_5	NOMS	0.6/40	9.7
M_6	PMOS	0.8/40	9.5
M_7	PMOS	0.8/20	4.6
M_8	PMOS	0.8/20	5

Tab. 3.7. FG OTA performance benchmark indicators.

Parameters		**Proposed OTA**	**Koziel [105]**	**Majumdar [106]**	**Li [107]**	**Zhang [108]**
CMOS Technology	[μm]	0.18	0.5	0.35	0.35	0.18
Power supply	[V]	± 0.5	± 2.5	3.3	3.3	1.8
Power consumption	[μW]	36	6800	3370	2330	590
Transistors number	[/]	8	37	14	22	68
AC Gain	[dB]	51	65	80.4	65	55
Linearity range	[mV]	± 0.5	± 0.75	± 0.1	/	± 0.27
Output resistance	[MΩ]	0.16	3.4	/	1.2	8.3
–3dB bandwidth	[MHz]	2	100	123.2	100	200

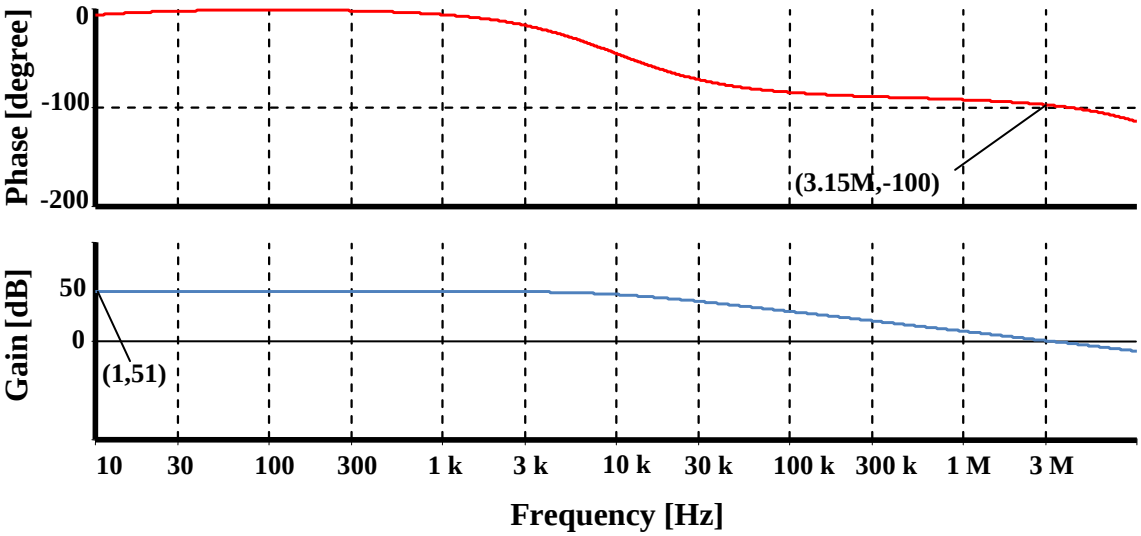


Fig. 3.16. Frequency response of FG–OTA.

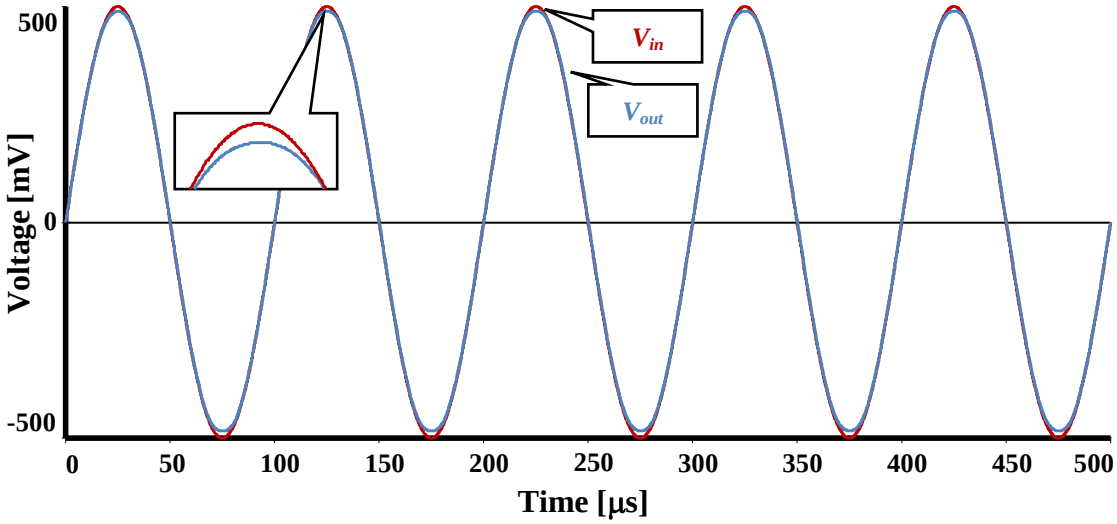


Fig. 3.17. Input and output signals vs. time.

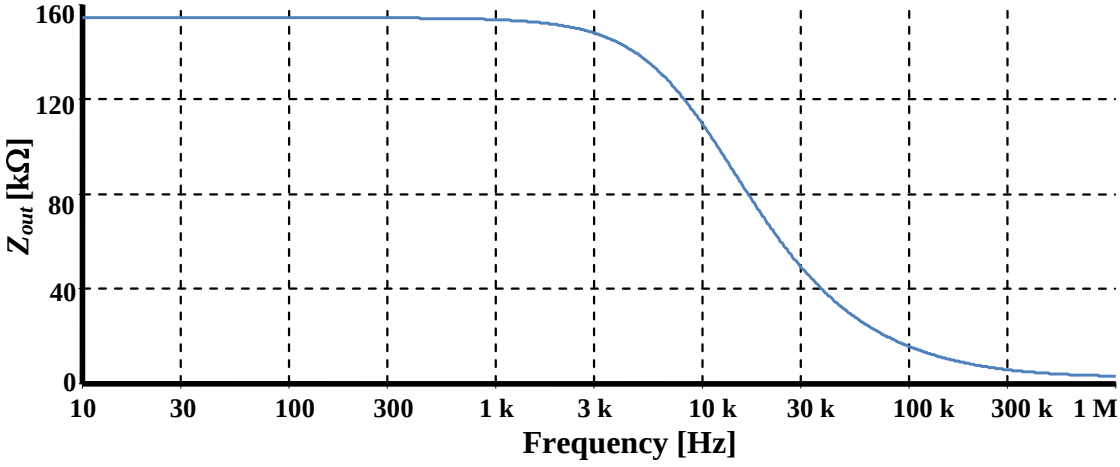


Fig. 3.18. Z_{out} vs. frequency.

Fig. 3.19 shows the simulated low–pass and band–pass results. We observe from the figure some peaking in the low–pass filter response; the reason is the value of Q (Q is 1.225 > 0.707). We can avoid this by reducing Q's value to remain under 0.707 by altering the value of g_{m1} according to (3.10.b), which is possible thanks to tunability of the circuit. It must be mentioned here; that increasing I_{bias1} more than adequate could affect the operation of the MOSFETs in OTA_1 and might push them out of the saturation region. On the other hand, ω_o is proportional to g_{m1} and g_{m2}. Hence, changing the value of g_{m1} must be done precisely. The amount of peaking for the low–pass filter vs. Q is indicated in Fig. 3.20.

The selectivity of the band–pass filter could be changeable by varying the bias current follows through OTA_1 or OTA_2; Fig. 3.21 shows a variety of curves with different natural (resonance) frequencies when I_{bias2}, thus G_{m2}, is variable. Values of I_{bias2} and corresponding frequency range and bandwidth for each value are given in Tab. 3.8. We notice from the table that bandwidth is increasing with the increase of frequency range, and both of them are proportional to the bias current I_{bias2}.

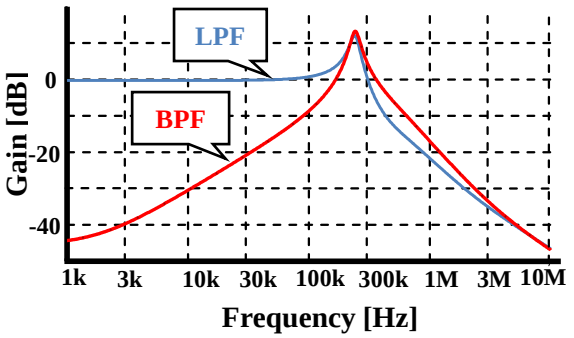


Fig. 3.19. Simulated frequency responses of low-pass and band–pass signals shown in Fig. 3.6.

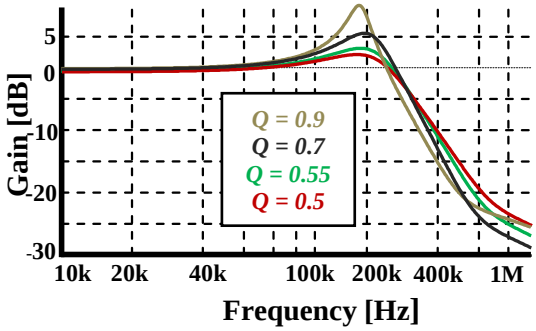


Fig. 3.20. Low-pass filter peaking vs. Q (G_{m1} is variable).

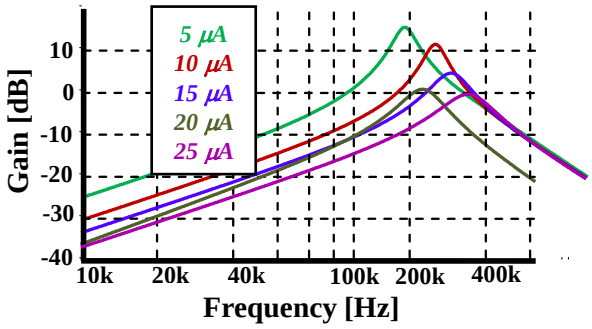


Fig. 3.21. Band–pass filter when I_{bias2} is varied (G_{m2} is variable).

Tab. 3.8. Frequency ranges and bandwidths for different values of I_{bias2}.

Bias current I_{bias2} [μA]	Frequency range [kHz]	Bandwidth [kHz]
5	171–208	37
10	224–278	54
15	247–340	93
20	261–384	123
25	272–417	145

3.2. CURRENT CONVEYOR (CC)

The current conveyor (CC) is a basic block that can be implemented in analog circuit design using a like–OPA approach; it also represents an effective alternative to the same OPA for designers. Sedra and Smith introduced the current conveyors in 1968 [43, 44] but their real advantages and innovative impact were not immediately clear at that time. Only in recent

years, with the growing diffusion of the current–mode approach as a way to design LV LP circuits, current conveyors have gained an increased popularity.

The original example presented by Sedra and Smith in 1968 was generically named by the authors “current conveyor”. The first block was identified as “first generation current conveyor”, or CCI, only when its evolved topology was called “second generation current conveyor”, or CCII, in 1970 [44,45]. CCI is a three–terminal device, schematically represented in Fig 3.22.

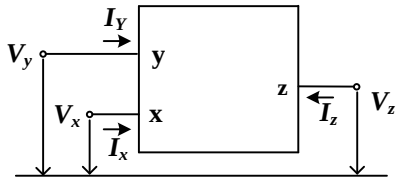


Fig. 3.22. CCI block representation.

It operates as follows: if a voltage is applied to Y node, the same voltage will appear at X node, while the opposite happens to currents. In fact, the current flowing at Y node is equal to the one flowing at X node; this current is “CONVEYED” to the output Z node, too. As can be seen, the potential of “x”, being set by that of “y”, is independent of the current being forced into port “x”. Similarly, the current through input “y”, being fixed by that of “x”, is independent of the voltage applied at “y”.

Current at Z node can flow in the direction of Ix or in the opposite one. In the matrix description reported in Fig. 3.23 (a), we assume that sign + stays for currents flowing in the same direction (positive CCI or CCI+), while sign – stays for the opposite situation (negative CCI or CCI–), considering CCI as reference. X and Y nodes have a low impedance level, ideally zero, whereas Z node shows a high impedance level, ideally infinite (Fig. 3.23 (a)). It is possible to represent CCI using the nullator–norator (nullor) formalism as in Fig. 3.23 (b) [44].

As stated before, the current conveyor success came only when CCII was introduced, two years later than CCI. Basically, there is only a little difference between the two blocks, but in the practical applications CCII has shown to be much more versatile and helpful than CCI.

CCII is topologically very similar to its predecessor. The electrical characteristics of the new block as well as a complete matrix description are reported in Fig. 3.23 (c). Compared to the previous version, the innovation of CCII is represented by the absence of current in the Y node, owing to its high impedance (ideally infinite). A complete nullator–norator model for CCII is represented in Fig. 3.23 (d) [44].

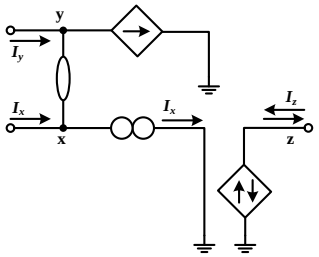
The wide spread of possible applications has led to the development of evolutions and improvements of the basic CCII topology such as dual output CCII (DOCCII), Current Gain CCII (CGCCII), Current Controlled CCII (CCCII), and third generation CCII (CCIII).

The operation of CCIII is identical to that of CCI with one difference; this difference consists in the position of I_Y. Here, an input current I being forced into terminal "x" will result in an opposite amount of current flowing into terminal "y". Ideally the terminal "x" exhibits short circuit input. In mathematical terms, the input–output characteristics of CCIII can be described by the hybrid equation from Fig.3.23 (e). The nullator–norator model for CCIII is represented in Fig. 3.23 (f). Third generation current conveyors may be useful, for example, in current sensing applications.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

CCI Node	Impedance level
X	Low (ideally 0)
Y	Low (ideally 0)
Z	High (ideally ∞)

(a)

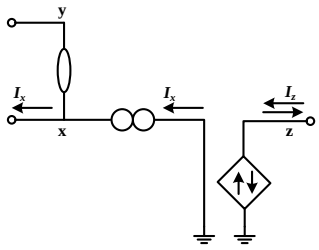


(b)

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

CCII Node	Impedance level
X	Low (ideally 0)
Y	High (ideally ∞)
Z	High (ideally ∞)

(c)

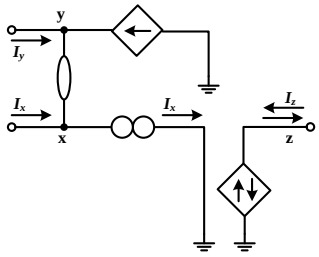


(d)

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

CCIII Node	Impedance level
X	Low (ideally 0)
Y	Low (ideally 0)
Z	High (ideally ∞)

(e)



(f)

Fig. 3.23. Matrix description of (a) CCI, (c) CCII and (e) CCII. Nullator–norator model for: (b) CCI, (d) CCII and (f) CCIII.

3.2.1 Bulk–driven second–generation current conveyor (BD CCII)

Second–generation current conveyors (CCIIs) have received considerable attention due to fact that they enjoy advantages such as large signal bandwidth, great linearity, wide dynamic range and simple circuitry. Therefore, many CCII–based analog circuits have been proposed in technical literature as in [22], [109–111]. However, the use of conventional CCII makes these circuits not suitable for working at low voltage (LV) supplies. There are several bulk–driven CCIIs (BD–CCIIs) proposed in [112], [113]. However, the structure in [112] suffers from the complexity while the structure in [113] consumes the power of 30 μW.

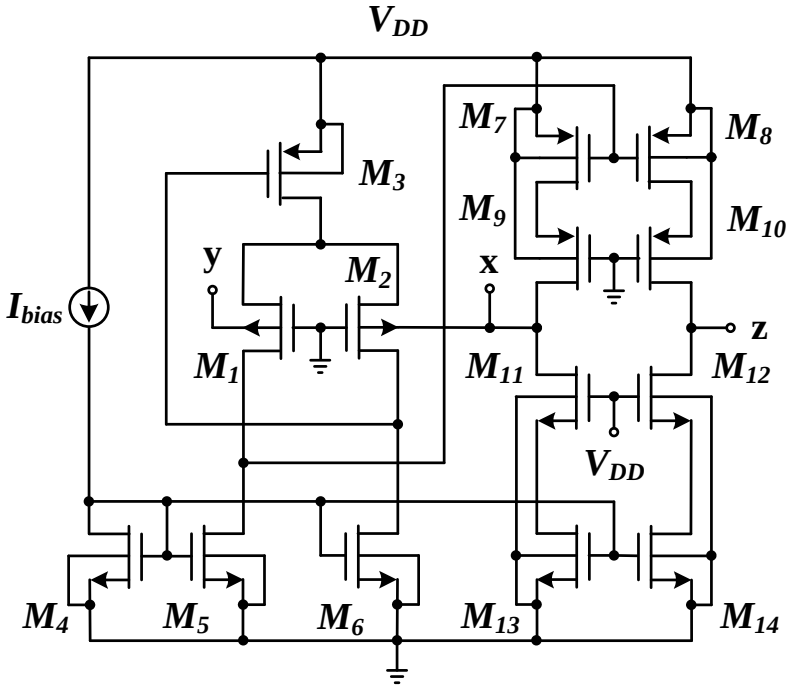


Fig. 3.24. Proposed BD–CCII.

A LV LP CCII using bulk–driven MOSs is shown in Fig. 3.24. The circuit is consisted of two stages, namely voltage and current followers. The voltage follower is consisted of a bulk–driven differential input M1 and M2 while current follower is consisted of M7 to M12. Transistors M4, M5, M6, M13 and M14 act as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit. Transistors M5 and M6 form the active load and transistor M3 acts as tail current source for the differential input stage. The current follower that consists of transistors M7 to M12 provides a current copy of x terminal to z terminal. Theoretically, the impedance of the z terminal should be high level. To achieve this requirement, the cascode technique was employed in BD–CCII MOS structure to achieve a high resistance value for z terminal and to improve the accuracy between z and x currents. The input voltage terminal y is connected to the bulk terminal of M1, therefore terminal y possesses high–input impedances. The use of bulk–driven flipped voltage follower for the differential input stages makes the minimum power supply voltage $V_{DD\ (min)}$. The supply voltage is given by:

$V_{DD\,(min)} = V_{GS\,(M3)} + V_{DS\,(M6)}.$ (3.12)

Equation (3.12) shows the capability of the proposed BD–CCII structure for operation under lower supply voltage.

3.2.1.1 BD–CCII–based inductance simulations

As an application example of the proposed BD–CCII, inductance simulations are implemented as shown in Fig. 3.25 [114]–[117]. Fig. 3.25 presents a grounded inductance which its equivalent impedance Z_{in1} can be written as:

$Z_{in1} = sC_1(R_{x1} + R_1)(R_{x2} + R_2),$ (3.13)

where R_{x1} and R_{x2} are the resistances at x terminal of BD–CCII$_1$ and BD–CCII$_2$, respectively.

Therefore, LV LP inductance simulations can be obtained using BD–CCII as active element. Moreover, other applications of LV LP analog signal processing such as amplifier, V–I converters, oscillators and filters could be also achieved using this device as active element.

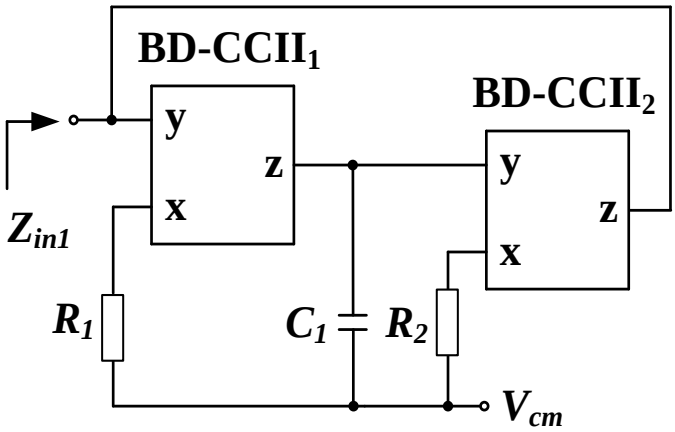


Fig. 3.25. BD–CCII–based grounded inductance simulations.

3.2.1.2 Simulation results

The proposed BD–CCII was simulated using PSpice simulator. The circuit was simulated using the 0.18 µm TSMC CMOS parameters [41]. The transistor aspect ratios of Fig. 3.24 are listed in Tab. 3.9. The supply voltage is 0.5 V, the biasing current I_{bias} and the common–mode voltage V_{CM} were, respectively, taken as 0.5 µA and 0.25 V. First test, the characteristic of proposed BD–CCII was investigated. Fig. 3. 26 shows the DC curves V_x versus V_y and the voltage error. It is obvious from Fig. 3. 26 that an accuracy between V_x and V_y with very low voltage offset of –0.19 mV when $V_y = 0$, also for V_y in range of –200 to 200 mV the voltage error is less than 2.5 mV.

Fig. 3.27 shows the DC curves I_z versus I_x and the current error. It is clear the accuracy between I_z and I_x with low current offset of 25 pA when $I_x = 0$, also for I_x in range of –4 to 4 µA the error is less than 8 nA.

The grounded inductance simulation in Fig. 3.25 was simulated using BD–CCIIs in Fig. 3.24. The supply voltage of V_{DD} = 0.5 V and the bias current of I_{bias} = 0.5 µA for BD–CCIIs were used. The resistor was set as $R_1 = R_2$ = 100 kΩ while the capacitor was set as C_1 = 1nF. Fig. 3.28 shows the simulated magnitude of the impedance of Fig. 3.25. The theoretical value is also included in the figure. At the frequency of 1 kHz, the simulated impedance is 64.4 kΩ while the theoretical value is 62.8 kΩ. Therefore, the error is about 2.5 %. The circuit consumes 9.6 µW. Fig. 3.29 shows simulated transient responses of Fig. 3.25 when the signal 1 kHz of 200 mV_{p-p} was applied. It is evident from Fig. 3.29 that the phase difference of voltage and current is 90 degrees.

Tab. 3.9. Transistors aspect ratios for Fig.3.24.

MOS transistors	W/L(µm/µm)
M_1–M_2	10/0.3
M_3	18/0.3
M_4–M_6	4/0.3
M_7–M_8	100/0.3
M_9–M_{10}	100/2
M_{11}–M_{12}	50/2
M_{13}–M_{14}	40/0.3

Tab. 3.10. Summarized performances of proposed BD–QFG–FDCCII

Parasitic	Value
Technology	0.18 µm
Supply voltage	0.5V
Common–mode voltage	0.25V
DC voltage range	400 mV
DC current range	–4 µA to 4 µA
–3dB bandwidth V_x/V_y	15.8 MHz
–3dB bandwidth I_z/I_x	25 MHz
R_y, C_y	30 GΩ, 4.68 fF
R_x, L_x	0.95 kΩ, 500 µH
R_z, C_z	10.9 MΩ, 0.137 pF
Power dissipation	4.7 µW

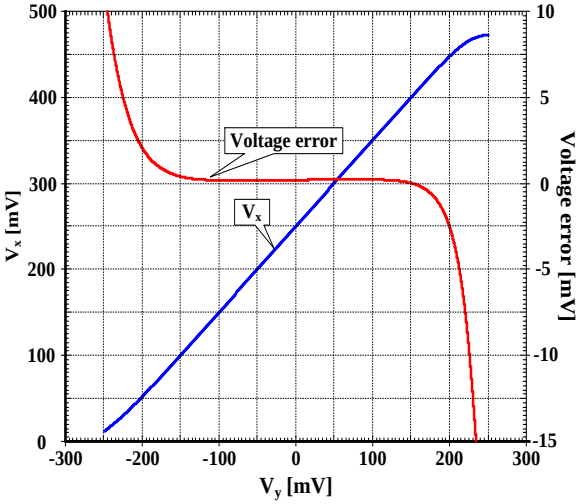


Fig. 3.26. DC curve V_x versus V_y and errors (V_{CM}=0.25V).

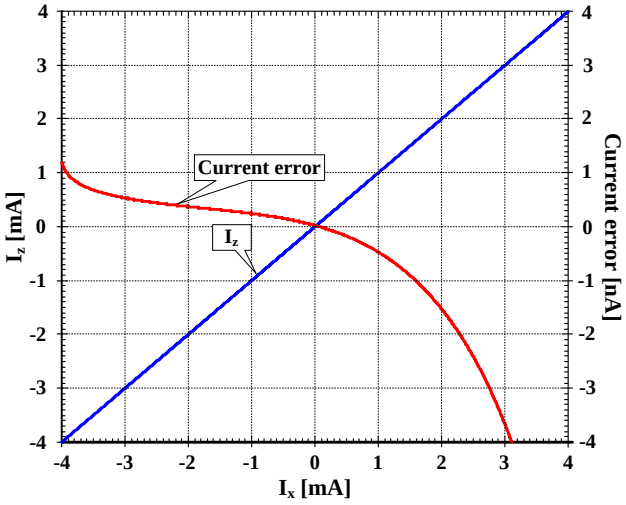


Fig. 3.27. DC curve I_z versus I_x and error.

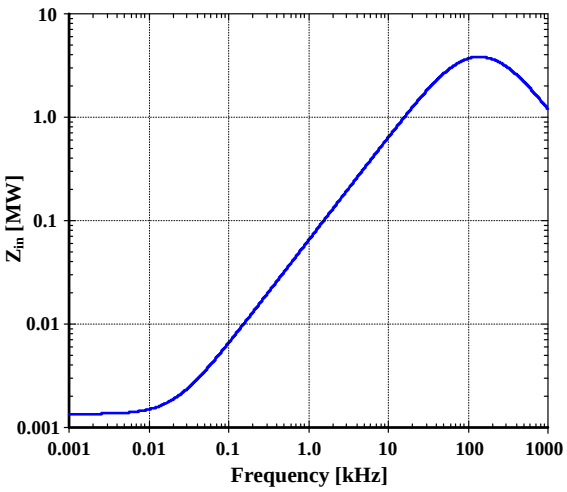


Fig. 3.28. Simulated impedance value versus frequency.

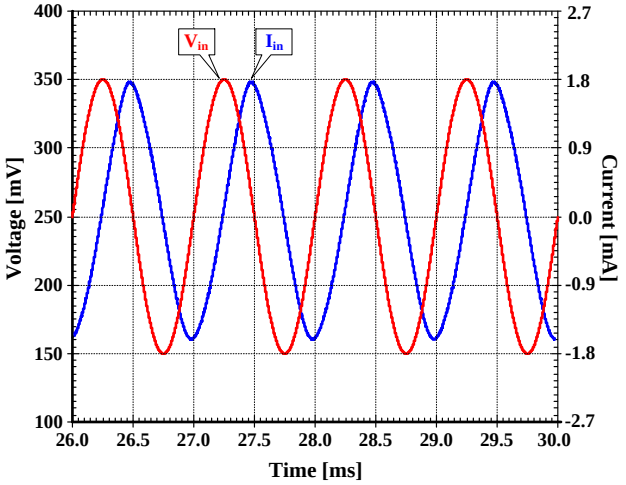


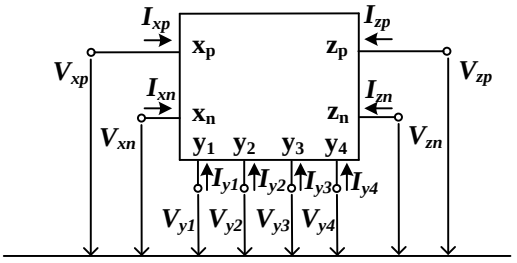
Fig. 3.29. Simulated transient responses response with input signal 1 kHz and amplitude 200 mV_{p-p}.

3.3. FULLY DIFFERENTIAL CCII (FD–CCII)

Second generation current conveyors are powerful and simple at the same time, but on the other hand, they show some drawbacks. For example, only one of the input terminals presents a high impedance level. This can be a problem if differential signals have to be handled. To overcome this problem, more complicated basic blocks which can be designed from simple modifications of the basic CCII are implemented by authors. These blocks include Differential CCII (DCCII), universal CCII (UCCII), differential voltage CCII (DV–CCII), and fully differential CCII (FD–CCII).

FD–CCII –which is the natural evolution of DV–CCII– was first introduced in 2000 [2] to improve the dynamic range and the suppression of all undesirable common–mode signals. It may be considered as the most versatile building block that can be designed starting from the basic CCII. It is an eight–terminal analog active device which matrix characteristic and block scheme are shown in Fig. 3.30 (a) and (b), respectively.

$$\begin{pmatrix} V_{xp} \\ V_{xn} \\ I_{zp} \\ I_{zn} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{xp} \\ I_{xn} \\ V_{y1} \\ V_{y2} \\ V_{y3} \\ V_{y4} \end{pmatrix}$$



(a) **(b)**

Fig. 3.30. FD–CCII (a) matrix characteristic (b) block scheme.

Because of this device has four y–terminals (two differential difference amplifiers), plus/minus x–terminals and plus/minus z–terminals; hence the arithmetic operation capability of voltage signals and addition/subtraction of current signals can be easily obtained. Therefore, many analog circuits using FDCCII as active elements were presented; see for example [3–12]. However, these circuits are not capable to work with low–voltage (LV) supply and low–power (LP) consumption, because the FDCCII that used in these circuits has the feature of high power supply (≥1.5 V).

3.3.1 Bulk–driven fully differential current conveyor (BD FD–CCII)

A new LV LP FDCCII using bulk–driven technique is shown in Fig. 3.31. The differential input stages are consisted of three bulk–driven differential amplifiers M_1–M_2, M_3–M_4 and M_5–M_6. Since the differential input stages are based on the bulk–driven flipped voltage follower, the minimum needed power supply voltage can be expressed by:

$$V_{DD\,(min)} = V_{GS\,(M7,M8,M9)} + V_{DS\,(M10,M11,M12)}. \quad (3.14)$$

If the voltages V_{GS} of M_1 to M_6 are lower than their threshold voltages, then these transistors will operate in sub–threshold region. Transistors M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28} and M_{29} act as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit. The power consumption of the circuit can be controlled appropriately by setting I_{bias} and V_{DD}. Transistors M_{10}, M_{11} and M_{12} are common for the differential input stages and they form the active load for them. Transistors M_7, M_8 and M_9 act as tail current sources for the first, second and third differential input stages, respectively. The second stage of three differential input stages is created by cascoding transistors M_{14}–M_{16}, M_{18}–M_{21}, M_{22}–M_{24} and M_{26}–M_{28}. The negative feedback connection between the drain

terminals of M_{16}, M_{18} and M_{24}, M_{26} and the input terminals of M_1 and M_6, respectively, is used to achieve the voltage transfers between x and y.

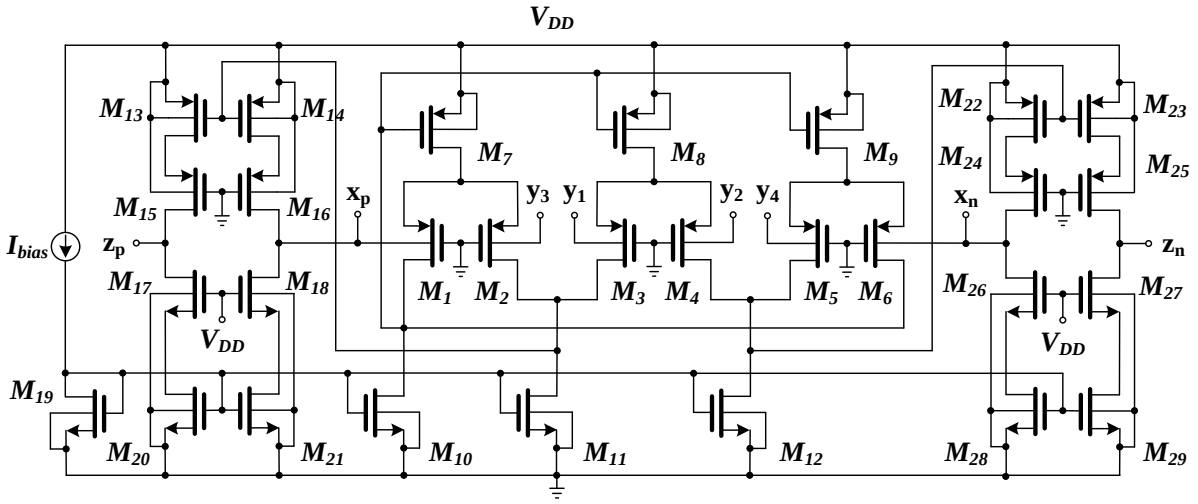


Fig. 3.31. Proposed BD–FDCCII.

Using small–signal equivalent circuit, the resistances of the x_p and x_n can be expressed, respectively, as:

$$R_{xp} \approx \frac{1}{g_{mb(M1)} r_{out1} g_{m(M14)}}, \tag{3.15}$$

$$R_{xn} \approx \frac{1}{g_{mb(M6)} r_{out2} g_{m(M22)}}, \tag{3.16}$$

where r_{out1} and r_{out2} are the output impedances of the first and second stages of BD–DDCC, respectively, and are given by:

$$r_{out1} \approx \frac{1}{g_o(M2) + g_o(M3) + g_o(M11)}. \tag{3.17}$$

$$r_{out2} \approx \frac{1}{g_o(M5) + g_o(M4) + g_o(M12)}. \tag{3.18}$$

Note that the low value of the bulk transconductances $g_{mb(M1)}$ and $g_{mb(M6)}$ on the denominators of (3.15) and (3.16) lead to high value of R_{xp} and R_{xp}. Hence, the values of R_{xp} and R_{xp} must be simply taken in account during application design.

On the other hand, the cascode transistors M_{13}–M_{15}, M_{17}–M_{20}, M_{23}–M_{25} and M_{27}–M_{29} create the output stage for BD–FDCCII at the outputs and they provide the current copies of the x_p terminal to the z_p terminal and the x_n terminal to the z_n terminal. Also the use of cascade technique makes the proposed BD–FDCCII provide a high resistance value for z terminals and improve the accuracy between z and x currents. Using small–signal equivalent circuit, the resistances of the x_p and x_n can be expressed, respectively, as:

$$R_{zp} \approx \frac{1}{\frac{g_{o(M20)}g_{o(M17)}}{g_{m(M17)}+g_{mb(M17)}} + \frac{g_{o(M13)}g_{o(M15)}}{g_{m(M15)}+g_{mb(M15)}}}, \tag{3.19}$$

$$R_{zn} \approx \frac{1}{\frac{g_{o(M29)}g_{o(M27)}}{g_{m(M27)}+g_{mb(M27)}} + \frac{g_{o(M23)}g_{o(M25)}}{g_{m(M25)}+g_{mb(M25)}}}, \tag{3.20}$$

where g_m and g_{mb} denote the gate and bulk transconductance of MOS transistor, respectively, g_o is the transistor output conductance. The cascode M_{13}–M_{15}, M_{17}–M_{20}, M_{23}–M_{25} and M_{27}–M_{29} are used to achieve significantly high value of R_{zp} and R_{zn} as shown in (3.19) and (3.20).

3.3.1.1 BD–FDCCII–based universal filter

In order to confirm that the proposed BD–FDCCII can be used in analog signal processing, the BD–FDCCII–based universal filter as shown in Fig. 3.32 is an example application. This filter employs one BD–FDCCII, two capacitors and two resistors. Because BD–FDCCII uses single power supply (0.5V), the common–mode voltage (V_{CM}) is needed. Using the equation in Fig. 3.30 (a), the output signals V_{o1}, V_{o2}, V_{o3} and V_{o4} of Fig. 3.32 can be obtained as:

$$V_{o1} = \left[\left(s^2R_1R_2C_1C_2\right)V_{in1} + \left(s^2R_1R_2C_1C_2 + sR_1C_1\right)V_{in2} + V_{in3}\right]/D(s), \tag{3.21}$$

$$V_{o2} = \left[(sR_1C_1C+1)V_{in1} + V_{in2} - V_{in3}\right]/D(s), \tag{3.22}$$

$$V_{o3} = \left[\left(s^2R_1R_2C_1C_2 + sR_1C_1\right)V_{in1} + sR_2C_2V_{in2} - sR_2C_2V_{in3}\right]/D(s), \tag{3.23}$$

$$V_{o4} = \left[sR_1C_1V_{in1} + (sR_2C_2+1)V_{in2} - (sR_2C_2+1)V_{in3}\right]/D(s), \tag{3.24}$$

where $D(s) = s^2R_1R_2C_1C_2 + sR_1C_1 + 1$. (3.25)

It is clearly seen from (3.21)–(3.24) that the filtering functions can be obtained appropriately connecting the input and the output terminals. As an example, high–pass (HPF), low–pass (LP), band–pass (BP) and band–stop (BS) filters can be obtained, respectively, as:

- HPF: $V_{in1}=V_{in}$, $V_{in2}=V_{in3}=V_{CM}$ and $V_{o1}=V_{out}$,
- LPF: $V_{in2}=V_{in}$, $V_{in1}=V_{in3}=V_{CM}$ and $V_{o2}=V_{out}$,
- BPF: $V_{in1}=V_{in}$, $V_{in2}=V_{in3}=V_{CM}$ and $V_{o4}=V_{out}$,
- BSF: $V_{in1}=V_{in3}=V_{in}$, $V_{in2}=V_{CM}$ and $V_{o1}=V_{out}$.

It should be noted that these filtering functions are obtained using only one BD–FDCCII. This is the advantage of this active building block that provides the arithmetic operation capability of voltage signals and addition/subtraction of current signal.

The natural frequency (ω_o) and the quality factor (Q) can be given by:

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}}. \tag{3.26}$$

$$Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}} \quad . \tag{3.27}$$

From equations (3.26) and (3.27), the parameter Q can be given by setting C_1/C_2 while parameter ω_o can be given by setting resistors R_1 and R_2.

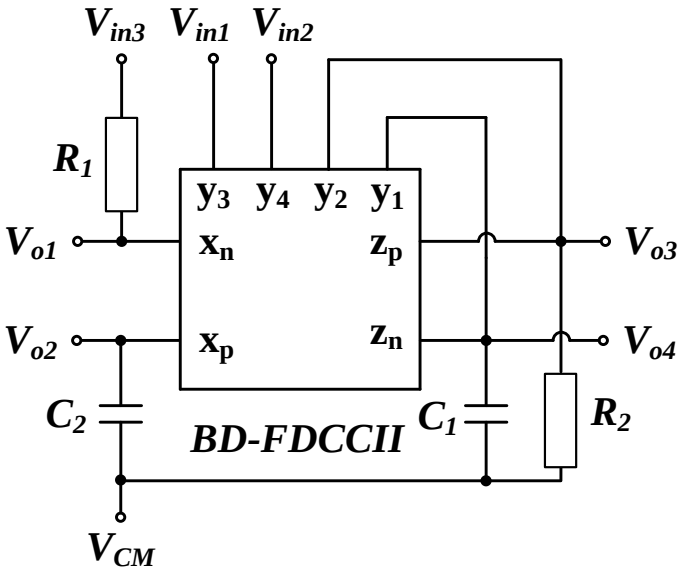


Fig. 3.32. BD–FDCCII–based universal filter.

3.3.1.2 Simulation results

The proposed BD–FDCCII was simulated by PSpice simulator using the 0.18 μm TSMC CMOS parameters. The transistor aspect ratios of Fig. 3.31 are listed in Tab. 3.11. The supply voltage is 0.5 V, while the biasing current I_{bias} was chosen as 2 μA and the common–mode voltage (V_{CM}) is 0.25 V. Fig. 3.33 shows the DC voltage characteristics of the two terminals X_p and X_n versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. Fig. 3.34 shows the output currents I_{zp} and I_{zn} versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. In this case, the terminals X_p and X_n were connected to 10 kΩ resistances and the terminals Z_p and Z_n were connected to 50 kΩ resistances.

Tab. 3.11. Transistors aspect ratios for Fig. 3.31.

MOS transistors	W/L(μm/μm)
M_1–M_6	20/0.3
M_7–M_9	20/0.3
M_{10}–M_{12}, M_{19}	4/0.3
M_{13}, M_{14}, M_{22}, M_{23}	100/0.3
M_{15}, M_{16}, M_{24}, M_{25}	200/4
M_{17}, M_{18}, M_{26}, M_{27}	100/4
M_{20}, M_{21}, M_{28}, M_{29}	16/0.3

Tab. 3.12. Summarized performances of proposed BD–FDCCII.

Parameters	Value
Technology	0.18 μm
Supply voltage	0.5 V
DC voltage range	–150 mV to 150 mV
DC current range	–4 μA to 4 μA
–3dB bandwidth voltage follower	≤ 8.6 MHz
–3dB bandwidth current follower	≤ 9.6 MHz
R_{yi}, C_{yi} (i = 1, 2, 3, 4)	47 GΩ, 27 fF
R_{xp}, R_{xp} L_{xp}, L_{xn}	10.2 kΩ, 2 mH
R_{zp}, R_{zp} L_{xp}, L_{xn}	4.2 MΩ, 0.25 pH
Power dissipation	13.6 μW

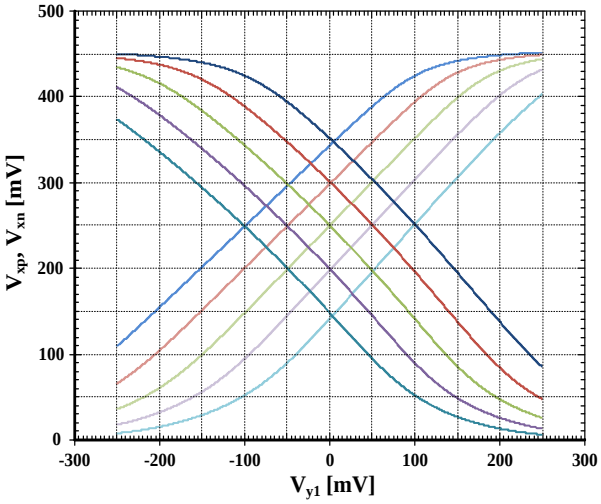


Fig. 3.33. Simulated V_{xp} and V_{xn} versus V_{y1} for different of V_{y2}.

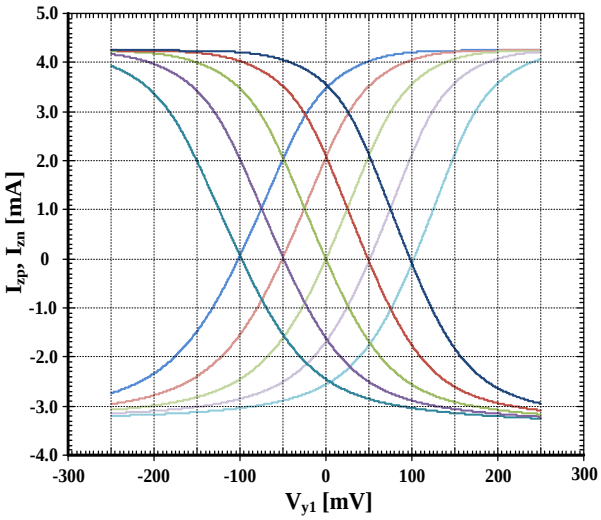


Fig. 3.34. Simulated I_{zp} and I_{zn} versus V_{y1} when R_{xp}=R_{xn}=10 kΩ.

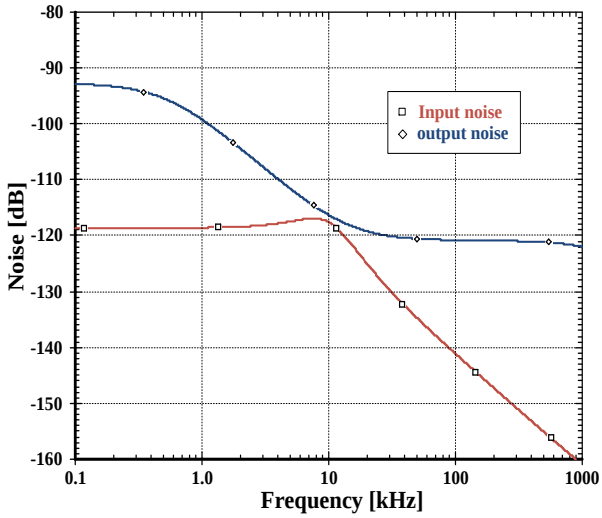


Fig. 3.35. The equivalence input and output noise against frequency.

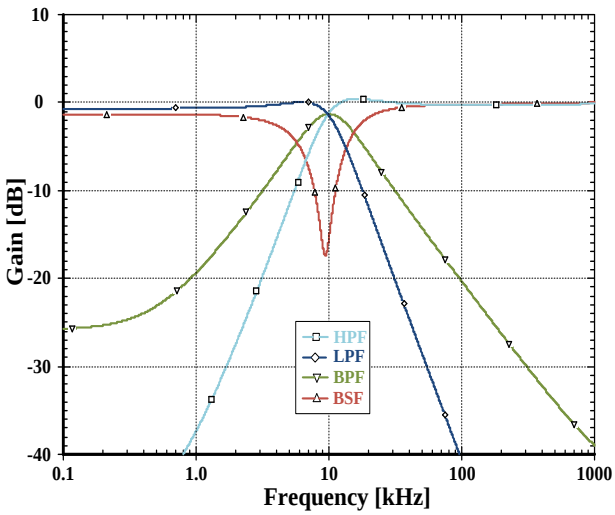


Fig. 3.36. Simulated HPF, LPF, BPF and BSF responses.

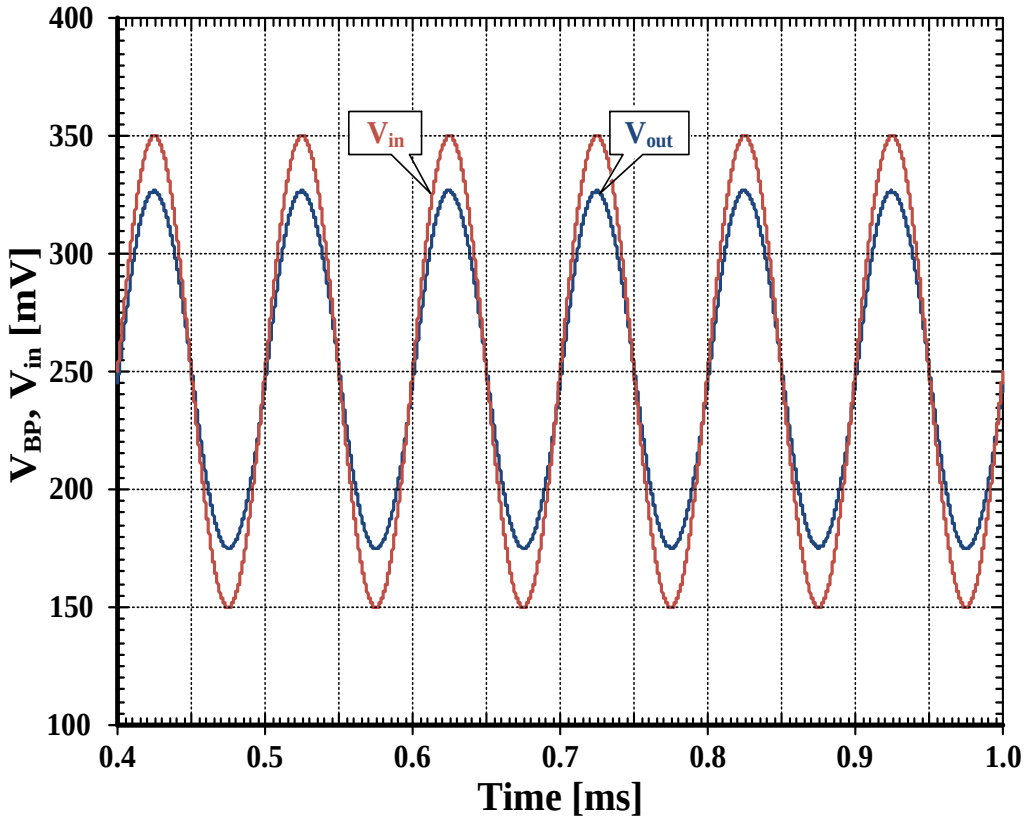


Fig. 3.37. The input and output waveforms of the BPF response for a 10 kHz sinusoidal input voltage of 100 mV (peak).

The simulated results of the proposed BD–FDCCII are also summarized in Tab 3.12. From this table, the values of R_{xp} and R_{xn} of 10.2 kΩ seem to be high; hence the values of R_{xp} and R_{xp} must be taken in account during application design.

The filter in Fig. 3.32 was also simulated using PSpice simulators. The BD–FDCCII as shown in Fig. 3.31 was used. As an example design, the capacitors $C_1 = C_2 = 50$ pF and the resistors $R_1 = R_2 = 345$ kΩ are given. This setting were chosen to obtain the HPF, LPF, BPF and BSF responses with $f_o = 10$ kHz and $Q = 1$. Fig. 3.35 shows the simulated input and output noise amplitude responses for BPF with INOISE and ONOISE. The simulated equivalent input noise and total output noise are respectively 22.7 μV/√Hz and 1.42 μV/√Hz for the frequency between 100 Hz to 1 MHz. The simulated results for the HPF, LPF, BPF, and BSF characteristics are shown in Fig. 3.36. For these results, the power consumption of only 16.1 μW was obtained. Fig. 3.37 shows that the input dynamic range of the BPF response with $R_1 = R_2 = 345$ kΩ and $C_1 = C_2 = 50$ pF, which extends up to amplitude of 100 mV (peak) without signification distortion. The THD about 2.2 % was defined from this figure.

3.3.2 Bulk–driven quasi–floating–gate fully differential current conveyor (BD–QFG FD–CCII)

The proposed BD–QFG FDCCII is shown in Fig. 3.38. The input stages are consisted of three BD–QFG differential amplifiers M_1–M_2 and M_{b1}–M_{b2}, M_3–M_4 and M_{b3}–M_{b4}, M_5–M_6 and M_{b5}–M_{b6}. Transistors M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5} and M_{b6} are operating in cutoff region to create large resistance value for providing the negative supply voltage to each gate of transistors M_1, M_2, M_3, M_4, M_5 and M_6. For this structure the minimum needed power supply voltage $V_{DD\,(\min)}$ can be expressed by:

$$V_{DD\,(min)} = V_{GS\,(M7,M8,M9)} + V_{DS\,(M10,M11,M12)}. \tag{3.28}$$

If the voltages V_{GS} of M_1 to M_6 are lower than their threshold voltages, these transistors will be operated as sub–threshold region. Transistors M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28} and M_{29} act as a multiple output current mirror applying the constant current source I_B to each branch of the circuit. The power consumption of the circuit can be controlled appropriately by setting I_{bias} and V_{DD}. Transistors M_{10}, M_{11} and M_{12} are common for the differential input stages and they form the active load for them. Transistors M_7, M_8 and M_9 act as tail current sources for the first, second and third differential input stages, respectively. The second stage of the three differential input stages is created by cascoding transistors M_{14}–M_{16}, M_{18}–M_{21}, M_{22}–M_{24} and M_{26}–M_{28}. Due to the negative feedback connection between the drain terminals of M_{16}, M_{18} and M_{24}, M_{26} and the input terminals of M_1 and M_6, respectively, the voltage transfers between x and y terminals is achieved. The compensation network R_{c1}, C_{c1} and R_{c2}, C_{c2} are used to ensure the stability of the BD–QFG FDCCII. Using small–signal equivalent circuit, the resistances of the x_p and x_n can be expressed, respectively, as:

$$R_{xp} \approx \frac{1}{g_{m(BD-QFG)(M1)} r_{out1} g_{m(M14)}}, \tag{3.29}$$

$$R_{xn} \approx \frac{1}{g_{m(BD-QFG)(M6)} r_{out2} g_{m(M22)}}, \tag{3.30}$$

where r_{out1} and r_{out2} are the output impedances of the first and second stages of BD–QFG FDCCII , respectively, and are given by:

$$r_{out1} \approx \frac{1}{g_o(M2) + g_o(M3) + g_o(M11)}. \tag{3.31}$$

$$r_{out2} \approx \frac{1}{g_o(M5) + g_o(M4) + g_o(M12)}. \tag{3.32}$$

On the other hands, the cascode transistors M_{13}–M_{15}, M_{17}–M_{20}, M_{23}–M_{25} and M_{27}–M_{29} create the output stage for BD–QFG FDCCII at the outputs and they provide the current copies of x_p and x_n to z_p and z_n terminals, respectively. Also the use of cascode technique makes the proposed BD–QFG FDCCII provide a high resistance value for z terminals and

improve the accuracy between z and x currents. Using small–signal equivalent circuit, the resistances of the x_p and x_n can be expressed, respectively, as

$$R_{zp} \approx \frac{1}{\frac{g_{o(M20)}g_{o(M17)}}{g_{m(M17)}+g_{mb(M17)}}+\frac{g_{o(M13)}g_{o(M15)}}{g_{m(M15)}+g_{mb(M15)}}}\ , \tag{3.33}$$

$$R_{zn} \approx \frac{1}{\frac{g_{o(M29)}g_{o(M27)}}{g_{m(M27)}+g_{mb(M27)}}+\frac{g_{o(M23)}g_{o(M25)}}{g_{m(M25)}+g_{mb(M25)}}}\ , \tag{3.34}$$

where g_m and g_{mb} denote the gate and bulk transconductance of MOS transistor, g_o is the transistor output conductance. As shown in (3.33) and (3.34) the value of R_{zp} and R_{zn} are significantly high due to using the cascode technique.

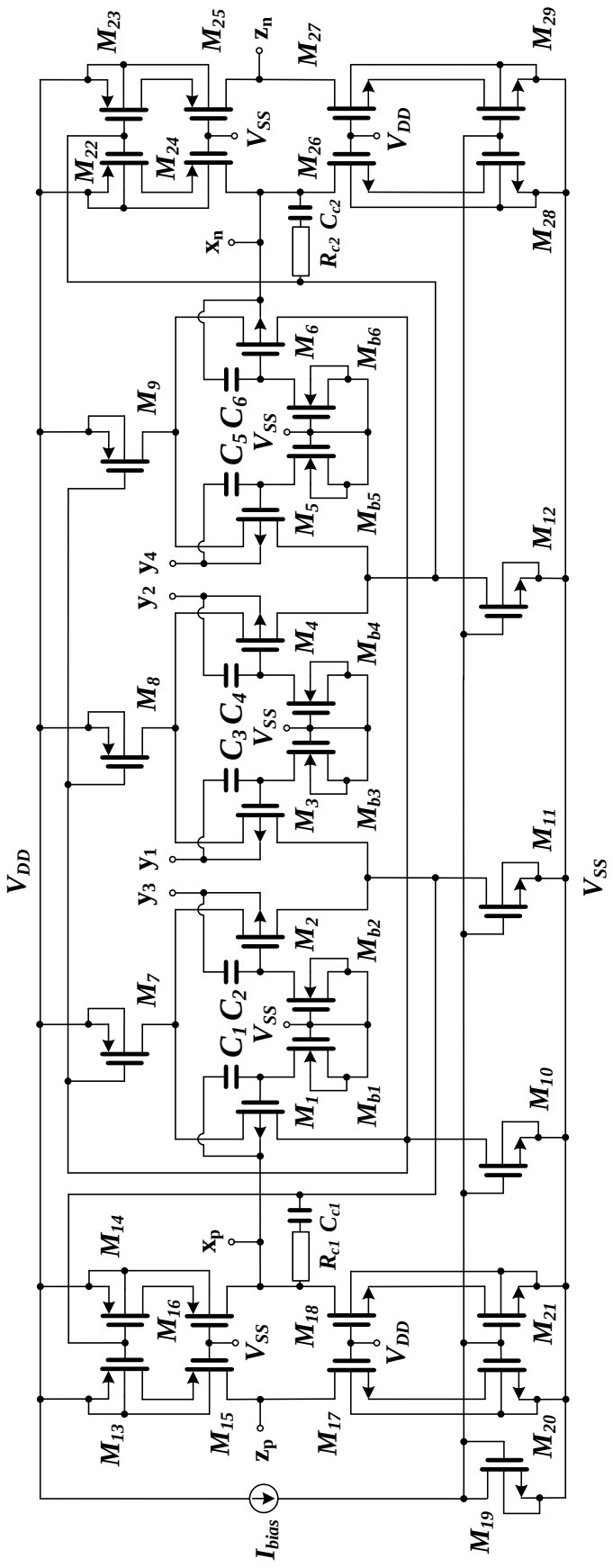


Fig. 3.38. Proposed BD–QFG–FDCCII.

3.3.2.1 BD–QFG–FDCCII–based universal filter

To confirm that the proposed BD–QFG FDCCII can be used in analog signal processing, the BD–QFG FDCCII–based universal filter as shown in Fig. 3.39 is an example application. This filter employs three BD–QFG FDCCIIs, two grounded capacitors and four grounded resistors. It should be noted that the input voltage V_{in} of the filter is applied to the y_2 of the first BD–QFG FDCCII. Thus, the filter has the feature of high–input impedance, which is suitable for cascading in voltage–mode operation. The use of all grounded passive components makes the filter particularly attractive for integrated circuit point of view [46]. Using the equation in Fig. 3.30 (a) and nodal analysis, the voltage transfer function of Fig. 3.39 can be expressed as:

$$\frac{V_{o1}}{V_{in}} = \frac{s^2 C_1 C_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 + s R_2 C_2 \left(R_4 / R_3\right) + 1}. \tag{3.35}$$

$$\frac{V_{o2}}{V_{in}} = -\frac{s^2 C_1 C_2 R_1 R_2 + 1}{s^2 C_1 C_2 R_1 R_2 + s R_2 C_2 \left(R_4 / R_3\right) + 1}. \tag{3.36}$$

$$\frac{V_{o3}}{V_{in}} = \frac{s R_2 C_2 \left(R_4 / R_3\right)}{s^2 C_1 C_2 R_1 R_2 + s R_2 C_2 \left(R_4 / R_3\right) + 1} \quad . \tag{3.37}$$

$$\frac{V_{o4}}{V_{in}} = \frac{1}{s^2 C_1 C_2 R_1 R_2 + s R_2 C_2 \left(R_4 / R_3\right) + 1} \quad . \tag{3.38}$$

$$\frac{V_{o5}}{V_{in}} = -\frac{s^2 C_1 C_2 R_1 R_2 - s R_2 C_2 \left(R_4 / R_3\right) + 1}{s^2 C_1 C_2 R_1 R_2 + s R_2 C_2 \left(R_4 / R_3\right) + 1}. \tag{3.39}$$

From (3.35)–(3.39), it can be seen that the high–pass filter (HPF), band–stop filter (BSF), band–pass filter (BPF), low–pass filter (LPF) and all–pass filter (APF) voltage responses are obtainable at the node voltage V_{o1}, V_{o2}, V_{o3}, V_{o4} and V_{o5}. It should be mentioned that the circuit is absent from component–matching condition for realization all the filtering functions. It is also to be noted that the output terminals V_{o3} and V_{o4} of Fig. 3.39 are not in low–output impedances. If low–output impedance terminal is needed, it can be obtained by connecting these terminals to the input $V_{in}^{'}$ and node voltage V_{o6} will become the new low–output impedance terminal. Therefore, the filter is possible for providing the high–input impedance and low–output terminal. The natural frequency (ω_o) and the quality factor (Q) can be given by:

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}. \tag{3.40}$$

$$Q = \frac{R_3}{R_4}\sqrt{\frac{R_1 C_1}{R_2 C_2}}. \tag{3.41}$$

From (3.40) and (3.41), it can be seen that the ω_o for all the filter responses can be controlled by R_1 and R_2, simultaneously, without affecting the parameter Q, while keeping C_1 and C_2 constant. The Q value can be controlled by the R_3/R_4, where the high–Q biquads can be

achieved when the suitable resistance ratio is selected. Therefore, the parameters ω_o and Q of the filter in Fig. 3.39 can be orthogonal controlled. It can be concluded via the application example that the filter can be provided all requirements of universal filters, namely, five standard filtering functions, grounded passive components, high–input and low–output impedance terminals, and orthogonal control of parameters Q and ω_o. This is the advantage of FDCCII that provides the arithmetic operation capability of voltage signals and addition/subtraction of current signal.

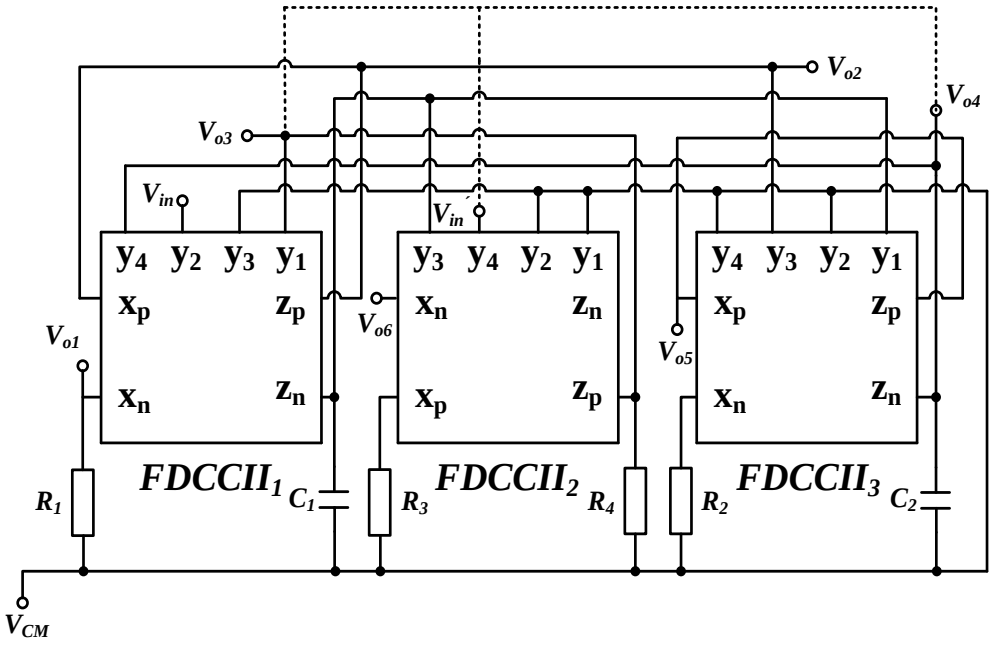


Fig. 3.39. Universal filter using BD–QFG–FDCCII.

3.3.2.2 Simulation results

The proposed BD–QFG FDCCII was simulated by PSpice simulators using the 0.18 µm TSMC CMOS parameters. The transistor aspect ratios of Fig. 3.38 were listed in Tab. 3.13. The supply voltage and the biasing current I_{bias} were taken respectively as 0.5 V and 2 µA. The common–mode voltage (V_{CM}) was 0.25 V.

Fig. 3.40 shows the DC voltage characteristics of the two terminals X_p and X_n versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. Fig. 3.41 shows the output currents I_{zp} and I_{zn} versus V_{y1} when $V_{y3} = V_{y4} = V_{CM}$ (0.25 V) and V_{y2} is swept from –0.1 to 0.1 V in steps of 0.05 V. In this case, the terminals X_p and X_n were connected to 10 kΩ resistance value and the terminals Z_p and Z_n were connected to 50 kΩ resistance values. The simulated results of the proposed BD–QFG FDCCII were also summarized in Tab. 3.14. From this table, the values of R_{xp} and R_{xn} of 10.2 kΩ seem to be high; hence the values of R_{xp} and R_{xp} must be taken in account during application design.

The filter in Fig. 3.39 was also simulated using PSpice simulators. The BD–QFG FDCCII as shown in Fig. 3.38 was used. As an example design, the capacitors $C_1 = C_2 = 50$ pF

and the resistors $R_1 = R_2 = R_3 = R_4 = 100$ kΩ are given. This setting has been designed to obtain the HP, BS, BP, LP and AP filter responses with $f_o = 31.8$ kHz and $Q = 1$. The simulated results for the HPF, BSF, BPF, and LPF characteristics were shown in Fig. 3.42. The characteristic of AP filter was shown in Fig. 3.43. It is observed from Figs. 3.42 and 3.43 that the filter in Fig. 3.39 performs all the standard biquadratic filtering functions well, which can verify the theoretical analysis. In this case, the natural frequency and the power consumption of 31.6 kHz and 48.3 μW were respectively expressed. To demonstrate the controlling of the *Q*–value, the resistance value of R_3 was varied, while keeping resistors $R_1 = R_2 = R_4$ and the capacitors $C_1 = C_2$. The simulated responses of the BPF filter for different *Q*–value are given in Fig. 3.44. In order to test the input dynamic range of the filter, the simulation was repeated for a sinusoidal input signal at $f_o = 31.6$ kHz. Fig. 3.45 shows that the input dynamic range of the BP response, which extends up to amplitude of 200 mV (peak to peak) without signification distortion. From Fig. 3.45, the total harmonic distortion (THD) was 2.2 %. Tab. 3.16 shows the comparison of BD–QFG FDCCII–based filter with previously FDCCII–based filters and confirm the attractive features of the proposed structure.

Tab. 3.13. Component values and transistors aspect ratios for Fig. 3.38.

MOS transistors	W/L(μm/μm)
M_1–M_6	20/0.3
M_{b1}–M_{b6}	8/0.3
M_7–M_9	20/0.3
M_{10}–M_{12}, M_{19}	4/0.3
M_{13}, M_{14}, M_{22}, M_{23}	100/0.3
M_{15}, M_{16}, M_{24}, M_{25}	200/4
M_{17}, M_{18}, M_{26}, M_{27}	100/4
M_{20}, M_{21}, M_{28}, M_{29}	16/0.3
C_1, C_2, C_3, C_4, C_5, C_6, C_{C1}, C_{C2} = 0.1 pF	
R_{C1}, R_{C2} = 3 kΩ	

Tab. 3.14. Summarized performances of proposed BD–QFG–FDCCII.

Parameters	Value
Technology	0.18 μm
Supply voltage	0.5 V
Common–mode voltage	0.25 V
Power dissipation	16.1 μW
DC voltage range	–100 to 100 mV
DC current range	–4 μA to 4 μA
–3dB bandwidth voltage follower	≤ 8.6 MHz
–3dB bandwidth current follower	≤ 9.6 MHz
R_{yi}, C_{yi} (i = 1, 2, 3, 4)	47 GΩ, 27 fF
R_{xp}, R_{xp} L_{xp}, L_{xn}	10.2 kΩ, 2 mH
R_{zp}, R_{zp} L_{xp}, L_{xn}	4.2 MΩ, 0.25 pH
Input noise (1 kHz)	6.33 μV/√Hz
Dynamic range (THD=1%@1 kHz)	59 dB

Tab. 3.15. Performance comparison of BD–QFG FDCCII with other FDCCIIs.

Parameters		**Proposed FDCCII**	**Ref. [2]**	**Ref. [42]**	**Ref. [13]**	**Ref. [39]**
Technology	[µm]	0.18	1.2	0.18	0.18	0.35
Power supply	[V]	0.5	± 1.5	± 0.8	1	± 1.5
Power consumption	[µW]	16.1	–	3000	403.77	–
Input voltage linear range	[mV]	± 100	± 200	± 300	± 1000	2400
Input current linear range	[µA]	± 4	–	2000	± 1000	± 500
–3dB bandwidth V_X/V_Y	[MHz]	6.8	10	–	25.7	–
–3dB bandwidth I_Z/I_X	[MHz]	9.6	–	> 1000	30	–

Tab. 3.16. The comparison of BD–QFG FDCCII–based filter with previously FDCCII–based filters.

Circuits	**Number of FDCCIIs**	**Number of capacitors & resistors**	**All–grounded capacitors**	**Orthogonal control of ω_0 and Q**	**No need matching–condition**	**High input & low output impedance**	**Voltage supply**
BD–QFG FD–CCII	3	2–C & 4–R	Yes	Yes	Yes	Yes & Yes	0.5 V
Ref. [3] (2003)	1	2–C & 2–R	Yes	No	Yes	Yes & No	±5 V
Ref. [4] (2005)	1	2–C & 3–R	No	Yes	Yes	No & No	±1.25 V
Ref. [7] (2009)	1	2–C & 3–R	No	Yes	Yes	No & No	±1.65 V
Ref. [9] (2010)	2	2–R & 2–R	Yes	No	yes	Yes & No	±1.65 V
Ref. [10] (2011)	1	2–C & 2–R	No	No	Yes	No & No	±1.3 V

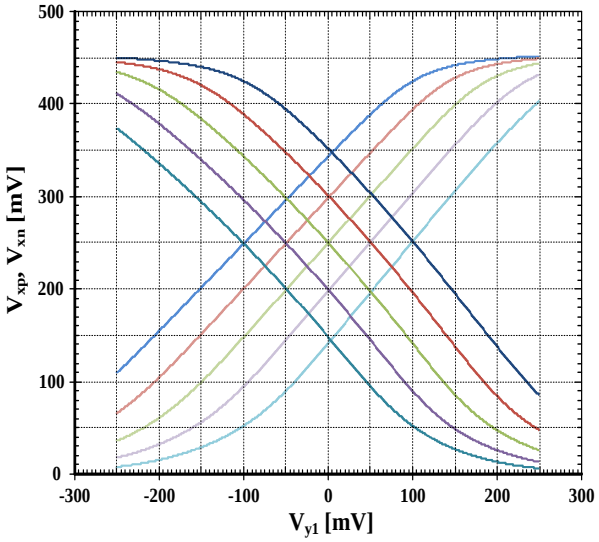


Fig. 3.40. Simulated V_{xp} and V_{xn} versus V_{y1} for different of V_{y2}.

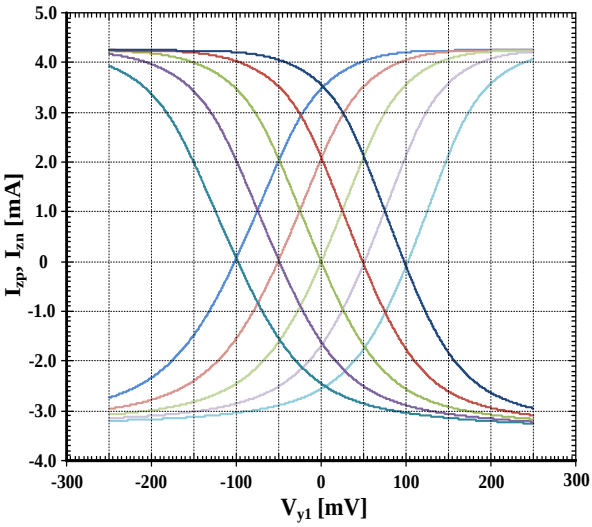


Fig. 3.41. Simulated I_{zp} and I_{zn} versus V_{y1} when $R_{xp} = R_{xn} = 10$ kΩ.

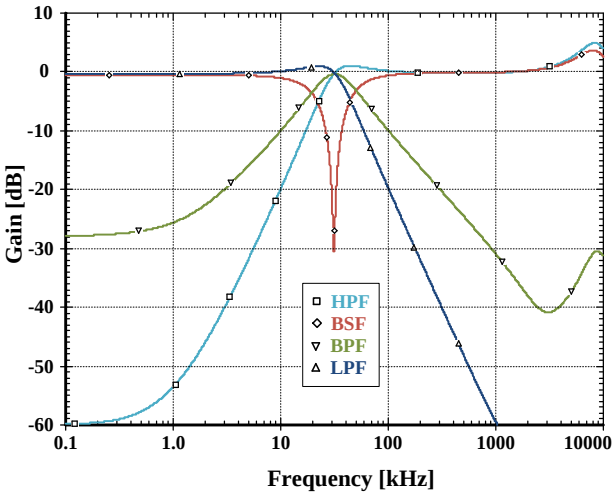


Fig. 3.42. Simulated HPF, BSF, BPF, and LPF responses.

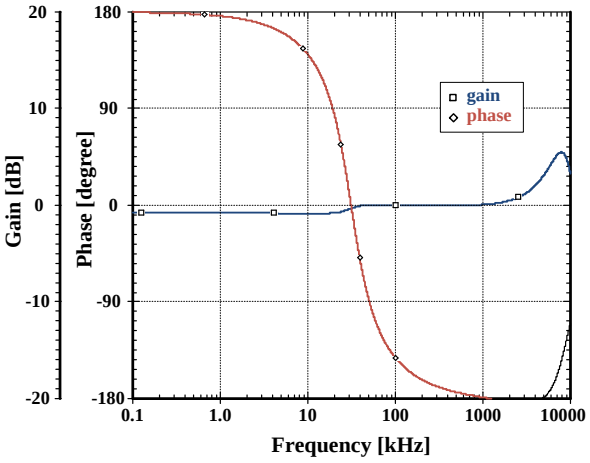


Fig. 3.43. Simulated gain and phase of APF responses.

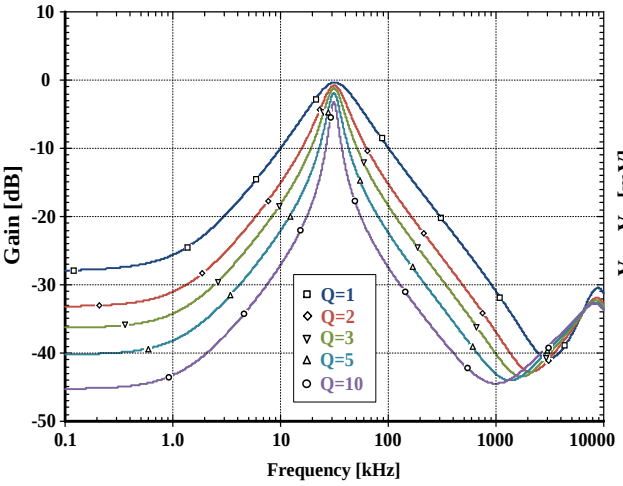


Fig. 3.44. Simulated BPF filter with adjustable *Q*.

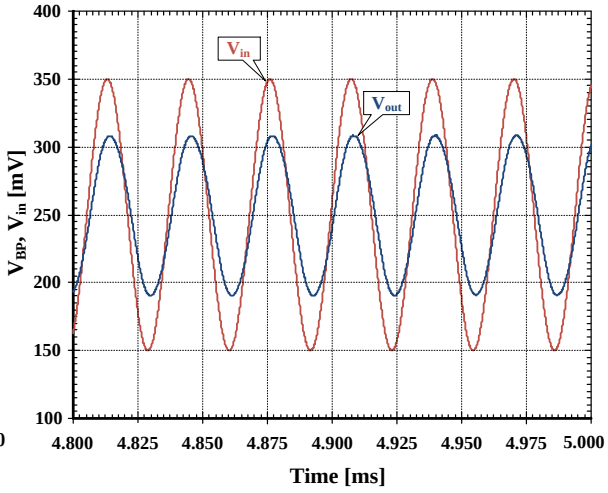


Fig. 3.45. The input and output waveforms of the BPF response for a 31.6 kHz sinusoidal input voltage of 100 mV (peak).

3.4.FULLY BALANCED DIFFERENTIAL DIFFERENCE AMPLIFIER (FB–DDA)

The differential difference amplifier (DDA) is a universal analog building block [48–57]. It is an extension of the concept of the op–amp, the main difference being that, instead of two single–ended inputs as in the case of op–amps, it has two differential input ports (V_{pp}–V_{pn} *) and (*V_{np}–V_{nn}*).* DDA–based circuits often provide high input impedance and simple external circuitry due to its feature of differential difference inputs [48]. DDA has been used in several applications such as telephone line adaptation [58], multiple–weighted input comparator [59], common–mode detection [60], [61], continuous–time filters [48], [60], [62], and switched capacitor circuits [50].

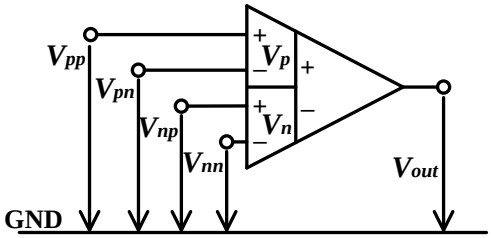
The DDA is a five–terminal device as shown in Fig. 3.46 (a). It has two differential inputs and one output, the output can be expressed as:

$$V_{out} = A_o\left[\left(V_{pp} - V_{pn}\right) - \left(V_{np} - V_{nn}\right)\right], \tag{3.42}$$

where *Ao* is the open–loop gain of the DDA. Analogous to the traditional op–amp, when a negative feedback is applied, the differential voltages of the two input ports become equal:

$$V_{pp} - V_{pn} = V_{np} - V_{nn} \text{ as } A_o \to \infty . \tag{3.43}$$

For a finite open–loop gain A_o, the difference between the two differential voltages increases as A_o decreases. Therefore, the open–loop gain should be as large as possible in order to achieve high–performance operation.



(a)

$$\begin{pmatrix} V_p \\ V_n \\ V_{out} \end{pmatrix} = \begin{pmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ A_o & -A_o & A_o & -A_o \end{pmatrix} \begin{pmatrix} V_{pp} \\ V_{pn} \\ V_{np} \\ V_{nn} \end{pmatrix}$$

(b)

Fig. 3.46. DDA (a) schematic symbol (b) matrix characteristic.

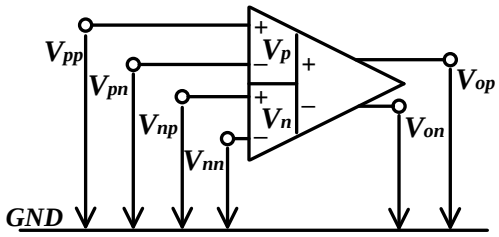
As in op–amp, DDA consists mainly of two stages: a differential– input single–ended output transconductance stage (differential pair with active loads) and a second gain stage (common–source amplifier with an active load). However, the DDA uses two differential pairs to realize the two input ports. For low–power operation and high current driving capabilities, a rail–to–rail output stage is usually employed.

Anyhow, the fully balanced differential difference amplifier (FB–DDA) is a versatile and interesting analog building block [63–67, 68–70]. The FB–DDA provides the solution for fully differential realizations of op–amp circuits where both of the op–amp inputs are floating [63–67]. Fully differential architectures improve the performance of analog and mixed analog/digital systems in terms of supply noise rejection, dynamic range, and harmonic distortion and reduce the effect of coupling between various blocks [63–67].

The FB–DDA is a six–terminal device as shown in Fig. 3.47. It has two differential input ports, (V_{pp}–V_{pn}) and (V_{np}–V_{nn}) and two output V_{op} and V_{on}. The output of the FB–DDA can be expressed as:

$$V_{op} = -V_{on} = A_o \left[\left(V_{pp} - V_{pn} \right) - \left(V_{np} - V_{nn} \right) \right], \tag{3.44}$$

where A_o is the open–loop gain of the FB–DDA. The symbol of FB–DDA and the matrix description are shown in Fig. 3.47.



(a)

$$\begin{pmatrix} V_p \\ V_n \\ V_{op} \\ V_{on} \end{pmatrix} = \begin{pmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ A_o & -A_o & A_o & -A_o \\ -A_o & A_o & -A_o & A_o \end{pmatrix} \begin{pmatrix} V_{pp} \\ V_{pn} \\ V_{np} \\ V_{nn} \end{pmatrix}$$

(b)

Fig. 3.47. FB–DDA (a) schematic symbol (b) matrix characteristic.

3.4.1 Bulk–driven quasi–floating–gate fully–balanced differential difference amplifier (BD–QFG FB–DDA)

A new structure of the FB–DDA based on the new technique BD–QFG is presented. The structure uses single supply voltage 0.5 V, hence it offers the lowest supply voltage compared to the previous conventional structures presented in the literature i.e.: ±5 V in [63], [69], 5 V in [64], ±1.5 V in [65], [66], 1.2 V in [67], 1.8 V in [68] and 3 V in [70].

The CMOS implementation of the FB–DDA with the common mode feedback circuit (CMFB) is shown in Fig. 3.48. The differential pairs are based on bulk–driven quasi–floating–gate technique. Thanks to using this technique the proposed circuit achieves higher gain and bandwidth. The BD–QFG transistor has a higher transconductance and transient frequency compared to bulk–driven and/or quasi–floating–gate transistor as mentioned earlier.

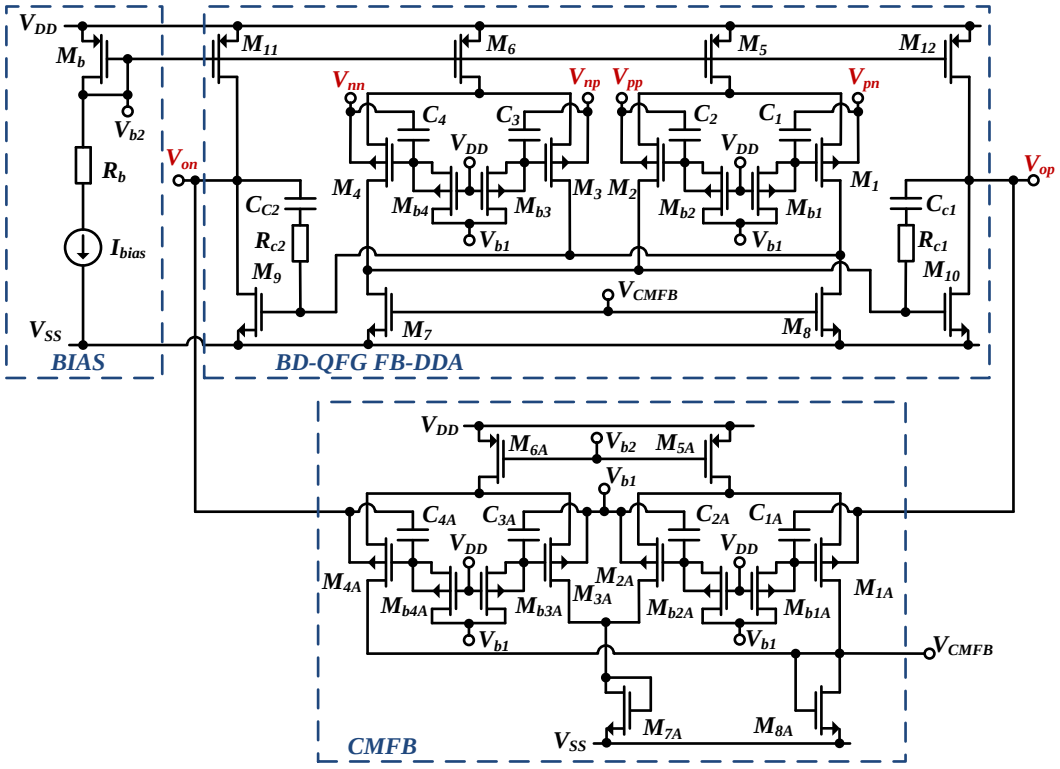


Fig. 3.48. CMOS implementation of the FB–DDA with CMFB circuit using BD–QFG transistors.

3.4.1.1 BD−QFG FB−DDA−based band–pass filter

The proposed BD–QFG FBDDA is used to realize Sallen–Key band–pass filter as an example application. The circuit is shown in Fig. 3.49. This filter employs one BD–QFG FBDDA, four capacitors and eight resistors. The transfer function of the filter are given by:

$$\frac{V_o}{V_{in}} = \frac{-ksC_2R_2}{s^2C_1C_2R_1R_2(1+k)+s(C_1R_1+C_2R_2+C_2R_1)+1}, \tag{3.45}$$

where $k = -\left(1+\frac{R_3}{R_4}\right)$. (3.46)

The pole frequency (ω_0) and the quality factor (Q) of the filter are described by:

$$\omega_o = \sqrt{\frac{1}{C_1C_2R_1R_2R_3(1+k)}}. \tag{3.47}$$

$$Q = \frac{\sqrt{C_1C_2R_1R_2(1+k)}}{(C_1R_1+C_2R_2+C_2R_1)}. \tag{3.48}$$

It is obvious from (3.47) and (3.48), that the pole frequency ω_0 can be adjusted independently from the pole frequency Q by adjusting the value of R_3. Thus, the parameter ω_0 can be orthogonal controlled.

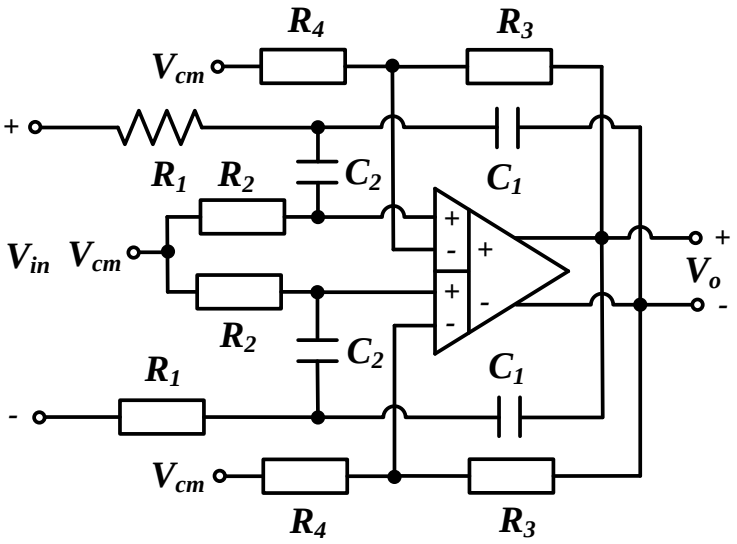


Fig. 3.49. Sallen–Key band–pass filter.

3.4.1.2 Simulation results

The simulations of the BD–QFG FB–DDA in Fig. 3.48 are performed using TSMC 0.18 μm *N*–well CMOS process with single voltage supply of 0.5 V and bias current was adjusted to I_{bias} = 80 nA. The used SPICE model is available on [41]. The optimal transistors aspect ratios are listed in Tab. 3.17.

Tab. 3.17. Component values and transistor aspect ratios for the BD–QFG FB–DDA in Fig. 3.48.

BD–QFG FB–DDA	W/L [µm/µm]
M_1, M_2, M_3, M_4, M_{1A}, M_{2A}, M_{3A}, M_{4A}	150/0.3
M_5, M_6, M_{5A}, M_{6A}, M_b	100/3
M_7, M_8, M_{7A}, M_{8A}, M_9, M_{10}	70/3
M_{11}, M_{12}	200/3
C_1, C_2, C_3, C_4, C_{1A}, C_{2A}, C_{3A}, C_{4A} = 2 pF C_{C1}, C_{C2} = 5 pF R_{C1}, R_{C2} = 4 kΩ R_b = 10 kΩ I_{bias} = 80 nA Vi_{DD} = 0.5 V V_{SS} = 0 V V_{b1} = V_{DD} /2 = 0.25 V	

The AC gain and phase responses of the BD–QFG FB–DDA with 5 pF load capacitance at each one of the outputs are shown in Fig. 3.50. The open–loop gain is 55 dB and the gain–bandwidth product is 17.3 kHz. The phase margin is 72º which guarantees the circuit stability.

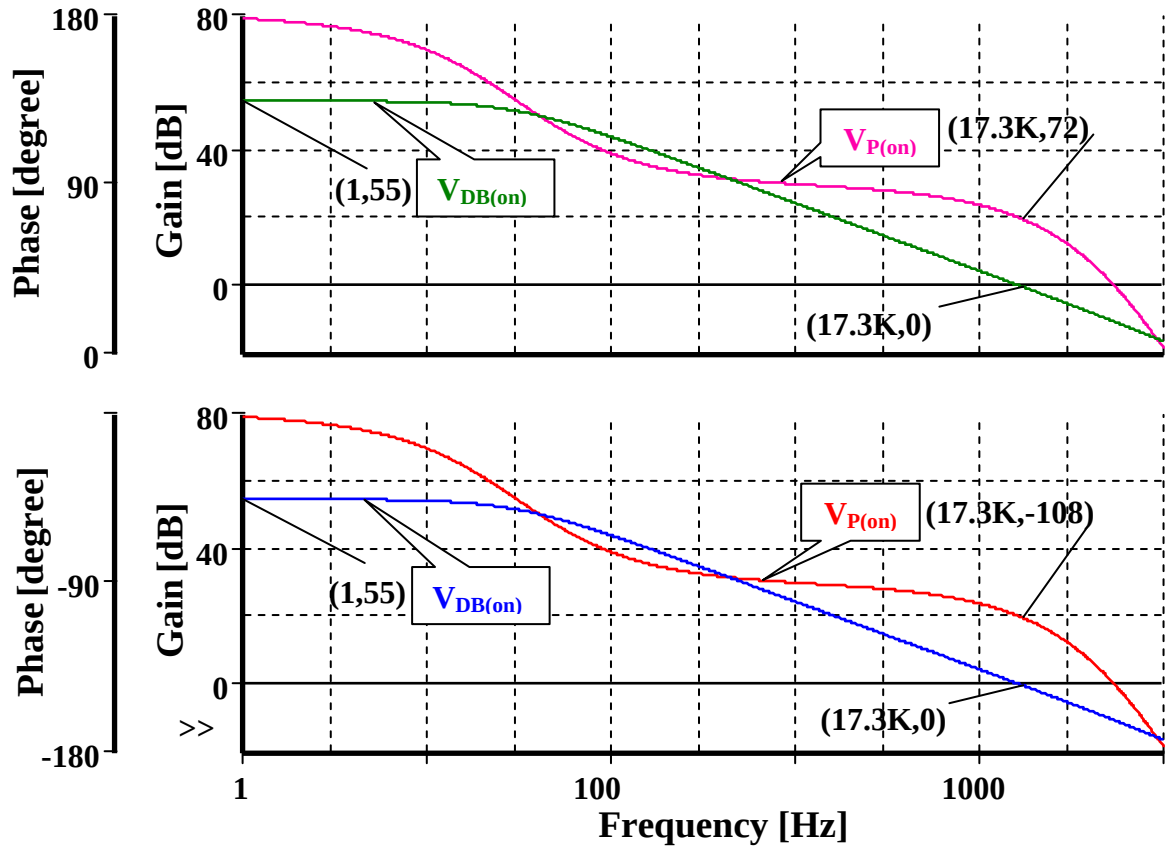


Fig. 3.50. The AC gain and phase responses.

It’s worthy to mention that the achieved bandwidth 17.3 kHz is sufficient for various low–voltage low–power applications as the wearable and implantable biomedical ones, since the biological signals have the attribute of extremely low frequency, i.e. in range of fraction of a hertz to several kilohertz. However, higher bandwidth could be achieved by simply increasing the bias current of the circuit.

The transient response of the BD–QFG FB–DDA with a fully differential voltage follower configuration is shown in Fig. 3.51. The input signal is set to 4 kHz and 80 mV amplitude, the total harmonic distortion (THD) is 1.4 %.

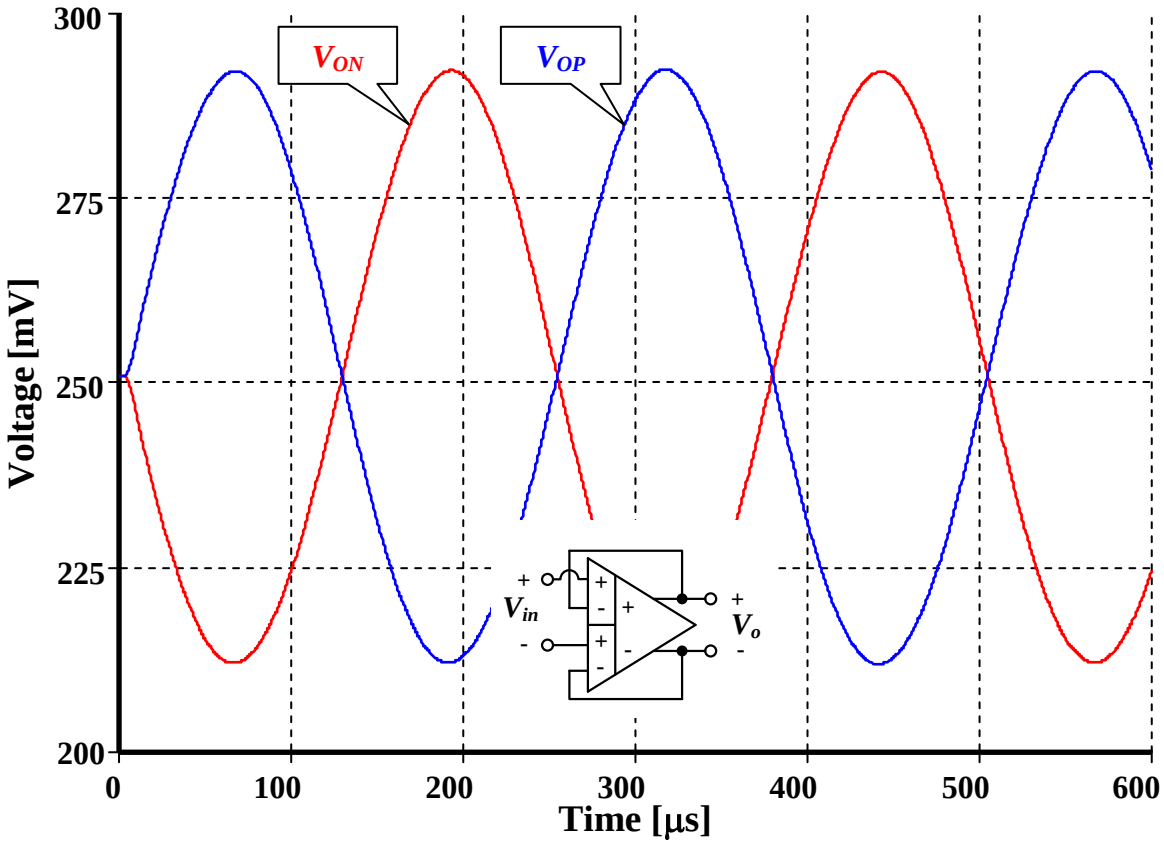


Fig. 3.51. The transient response with input signal 4 kHz and amplitude 80 mV where FB–DDA is connected as a fully differential voltage follower.

The DC response of the BD–QFG FB–DDA connected as a fully differential voltage follower is shown in Fig. 3.52. The wide voltage range of the proposed circuit is notable.

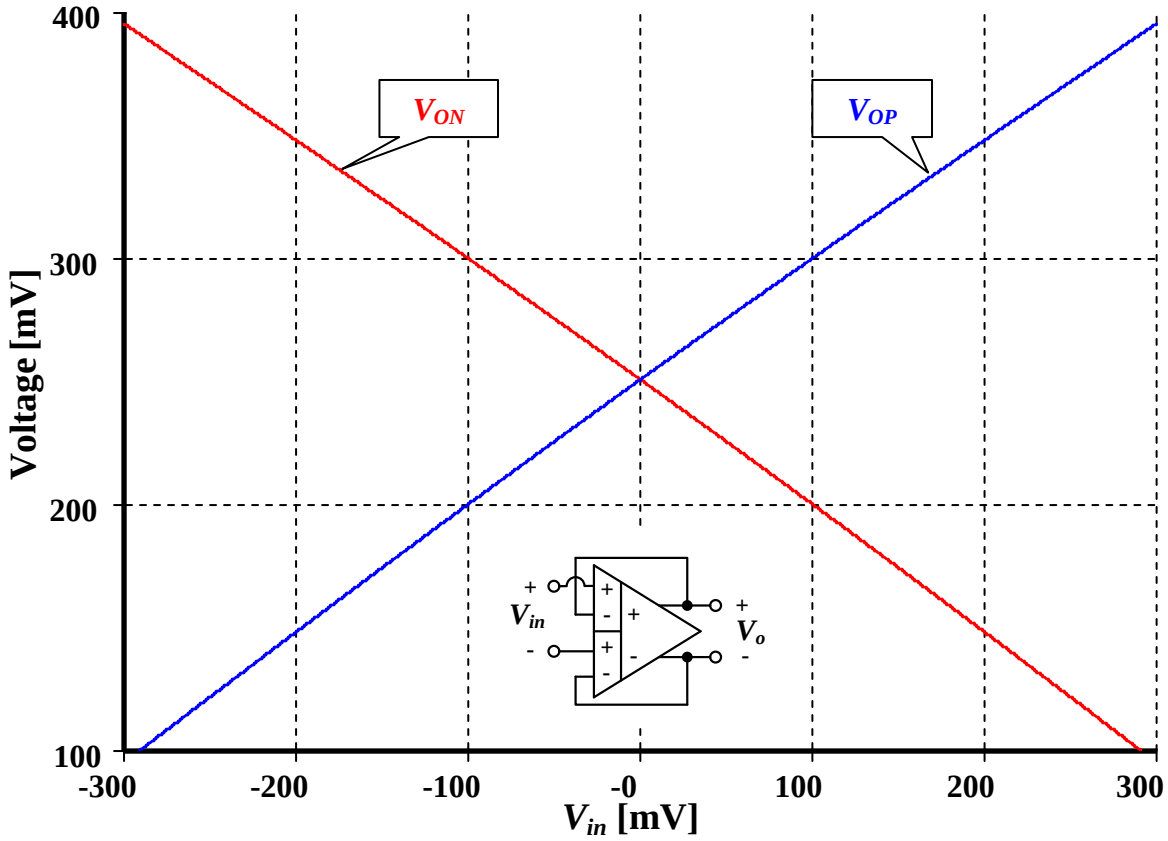


Fig. 3.52. The DC response of the BD–QFG FB–DDA connected as a fully differential voltage follower.

Finally, the simulation results of the proposed BD–QFG FB–DDA are summarized in Tab. 3.18. In addition, these results are compared to the DDA and FB–DDA presented, respectively, in [68, 69]. The attractive performances offered by the design are evident mainly the ultra–low voltage supply and the power consumption.

Tab. 3.18. Simulation results of the BD–QFG FB–DDA compared to DDA and FB–DDA.

	DDA [68]	FB–DDA [69]	BD–QFG FB–DDA
Voltage supply (V)	1.8	±5	0.5
Power consumption (µW)	15.12	54360	0.357
DC gain (dB)	130.1	84	110
Unity gain bandwidth (kHz)	940	6000	17.3
Phase margin (°)	59	50	72
CMRR (dB)	114 @ 10 Hz	–	108 @ 10 Hz 98 @ 100 Hz 78 @ 1 kHz
Input–referred noise (nV/√Hz)	471.7 @ 1 Hz	–	790 @ 10 Hz 290 @ 100 Hz 285 @ 1 kHz
Technology (µm)	0.18	2	0.18

The universal filter in Fig. 3.49 was also simulated. The proposed BD–QFG FB–DDA in Fig. 3.48 was used. As an example design, C_1 = C_2 = C_3 = C_4 = 5.53 nF R_1 = 1 MΩ, R_2 = 100 Ω, R_3 = 800 kΩ and R_4 = 100 kΩ were given. This setting has been designed to obtain the BP filter response with f_o= 200 Hz and Q = 3. The simulation result for the filter characteristics is shown in Fig. 3.53. For these results the power consumption of only 0.357 μW was obtained. In order to test the input dynamic range of the filter, the simulation has been repeated for a sinusoidal input signal at $f_o \cong$ 200 Hz. Fig. 3.54 shows that the input dynamic range of the BP response extends up to amplitude of 120 mV (peak–to–peak) without signification distortion. The total harmonic distortion (THD) is about 1.05 % from this figure.

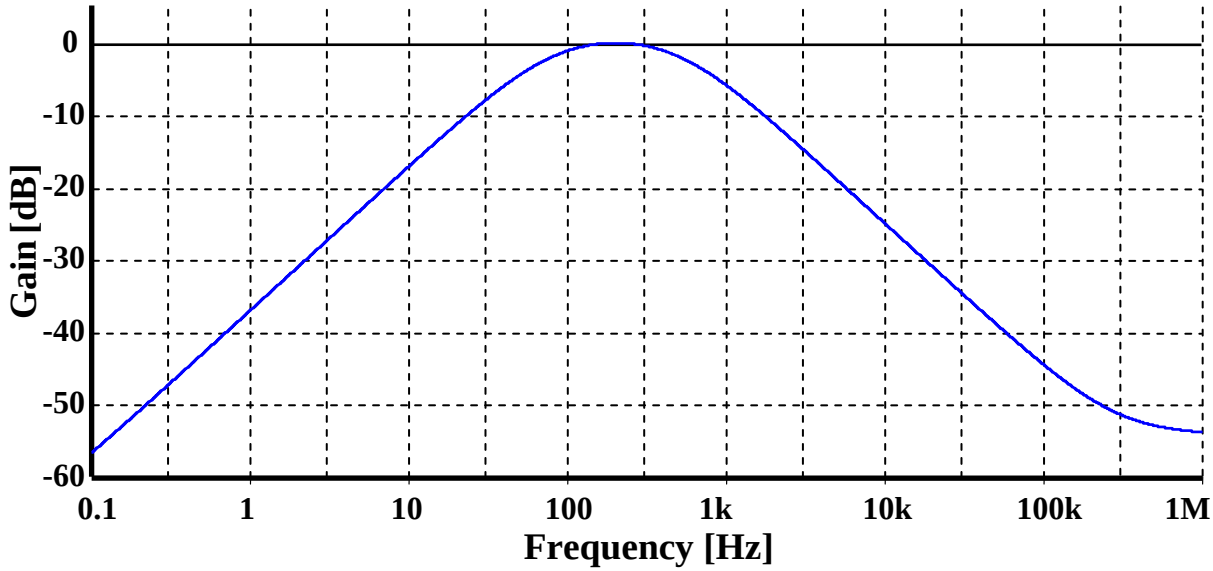


Fig. 3.53. Simulated magnitude response BP filter.

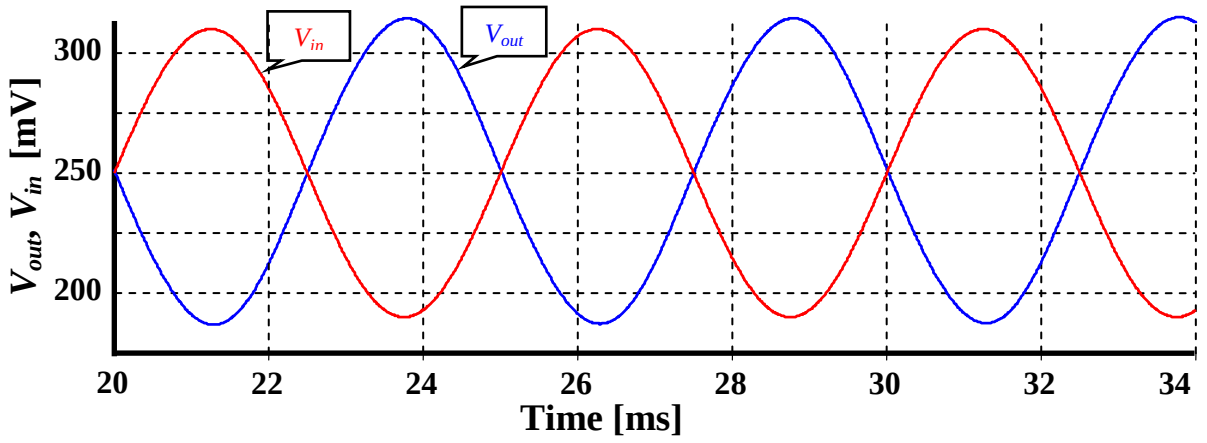


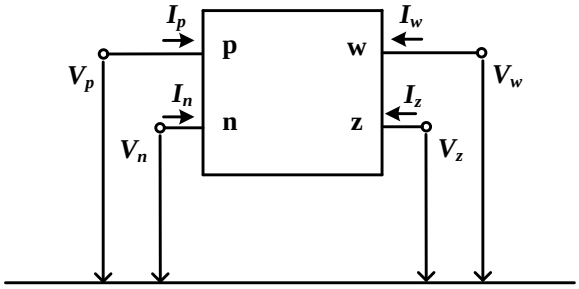
Fig. 3.54. The input and output waveforms of filter for a 200 Hz sinusoidal input voltage of 120 mV (peak-to-peak).

3.5. CURRENT DIFFERENCING BUFFERED AMPLIFIER (CDBA)

The CDBA (Current Differencing Buffered Amplifier) or more specifically CDVB (Current Differencing Voltage Buffer) or as so–called DCVC (Differential Current Voltage Conveyor) is introduced in year 1999 by Acar [75]. CDBA is a universal element for filter design, primarily for voltage–mode operation. Numerous papers were published about CDBA applications such as voltage mode and current mode filters [76–84] and oscillators [85–90]. Some of the applications profit from the basic CDBA feature, i.e. the non–problematic implementation of both non–inverting and inverting integrator as a building block of filters of arbitrary order. Matrix characteristic and block scheme are shown in Fig. 3.55 (a) and (b), respectively.

$$\begin{pmatrix} V_p \\ V_n \\ I_Z \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_p \\ I_n \\ V_Z \\ I_w \end{pmatrix}$$

(a)



(b)

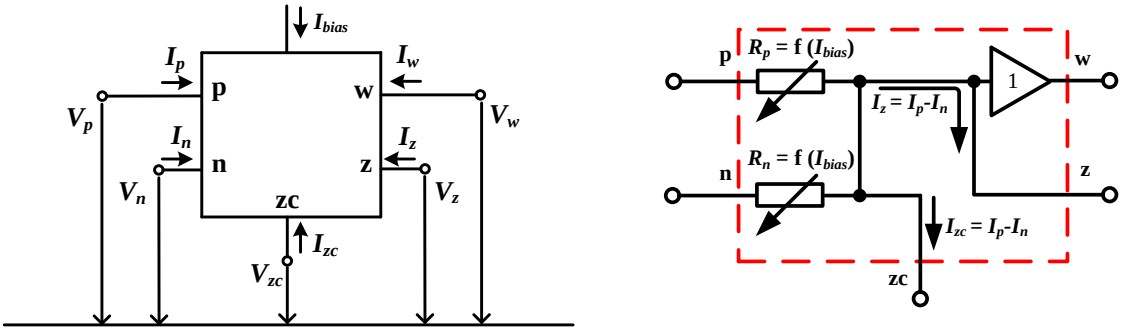
Fig. 3.55. CDBA (a) matrix characteristic (b) block scheme.

CDBA contains the so–called CDU (Current Differencing Unit) as an input stage and the voltage unity–gain buffer as output stage. Basically, CDU is a current conveyor of the MDCC (Modified Differential Current Conveyor) type: It has two low–impedance terminals, p and n. The difference of currents I_p and I_n flows out of the z terminal and the corresponding voltage drop on the external impedance is copied by the buffer to the w output. That is why the additional impedances are necessary for implementing the feedbacks from the voltage output to the current inputs. It is inconvenient from the point of view of simplicity and low power consumption. Another drawback is the impossibility of direct electronic control of circuit parameters such as that for the OTA–based applications. This problem is solved via CC CDBA (Current–Controlled CDBA).

The CC–CDBA is described in [91]. The nonzero parasitic resistances of p and n terminals of the CDU are controlled electronically via bias currents. The p and n terminals thus act as voltage input terminals. These voltages are then transformed into currents, whose values are electronically controlled. In fact, this approach represents a transition to a "pure" voltage mode.

3.5.1. Bulk–driven z–copy current–controlled current differencing buffered amplifier (BD ZC CC CDBA)

The ZC–CC–CDBA is a five terminal active element; two low impedance input terminals (p, n), two high impedance output terminals (z, zc), and one low impedance output terminal (w). The schematic symbol of the ZC–CC–CDBA and its equivalent circuit are depicted in Fig .3.56 (a) and (b), respectively.



(a) **(b)**

Fig. 3.56. ZC–CC–CDBA: (a) schematic symbol, (b) equivalent circuit.

Unlike the conventional CDBA, here the input voltages V_p and V_n are not equal to zero. Instead they have finite parasitic input resistances R_p and R_n, respectively. The input/ output behavior of the ZC–CC–CDBA circuit can be described by the following matrix:

$$\begin{pmatrix} V_p \\ V_n \\ I_z, I_{zc} \\ V_w \end{pmatrix} = \begin{pmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_p \\ I_n \\ V_z \\ I_w \end{pmatrix}. \tag{3.49}$$

The MOS internal structure of the proposed ZC–CC–CDBA is depicted in Fig. 3.57. Transistors M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, and M_{b6} represent multiple output current mirror providing the constant bias current I_{bias} to the circuit branches. The current differencing unit (CDU) is the cascade of two BD current followers M_1–M_4 and M_5–M_8. Each current follower is constructed from the flipped voltage follower current sensor structure (BD–FVFCS) [92] with enhanced BD current mirror [93]. This combination provides extremely low voltage operation capability and better linearity. The transistors M_4 and M_8 represent simple voltage source. The current I_B through these transistors is extremely small in comparison with the bias current I_{bias} to avoid extra undesired offset. The transistors M_9, M_{10} mirror the output current of the first current follower ($I_n + I_{bias}$) to be subtracted from the output current of the second current follower ($I_p + I_{bias}$). The resulting current ($I_p - I_n$) is lead away from z terminal. Transistors M_{11} and M_{12} provide a current copy of z terminal to zc terminal. The voltage follower (VF) consists of BD differential input stage M_{13}, M_{14}. Transistor M_{15} acts as a tail

transistor of the differential input stage. Transistors M_{b6} and M_{16} represent the second stage of the VF. Transistors M_{b4} and M_{b5} act as active loads. Transistors M_{13}–M_{15} construct BD flipped voltage follower differential structure (BD–DFVF) [92].

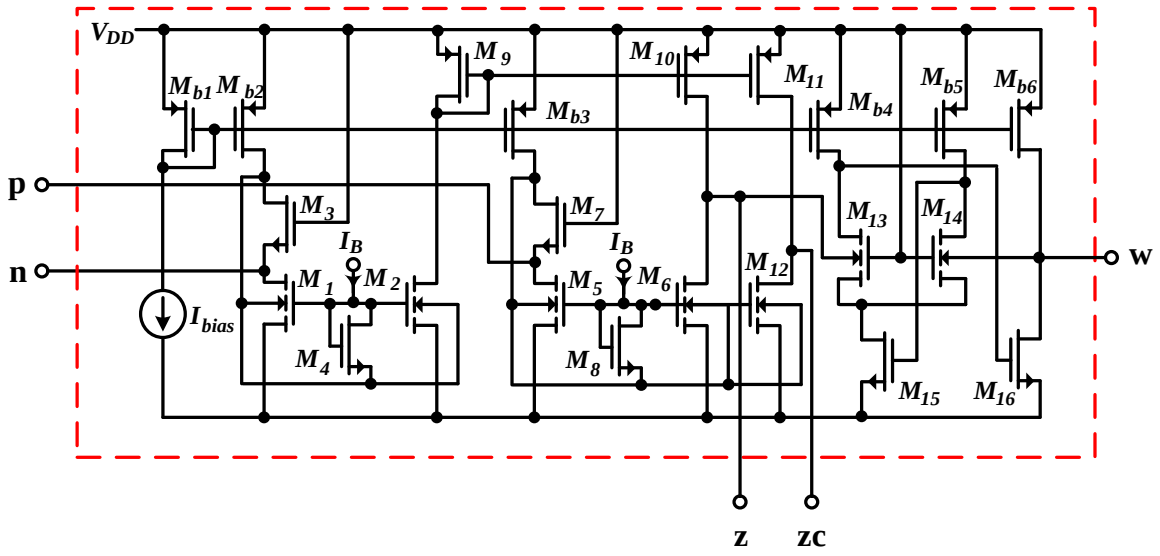


Fig. 3.57. The proposed MOS structure of the ZC–CC–CDBA.

Owing to use the BD flipped voltage follower structure in the proposed circuit, the minimum power supply voltage $V_{DD\,(min)}$ is given by:

$$V_{DD\,(min)} = V_{GS} + V_{DSat} \tag{3.50}$$

As it is obvious from (3.50), the proposed circuit is capable to operate under ULV conditions.

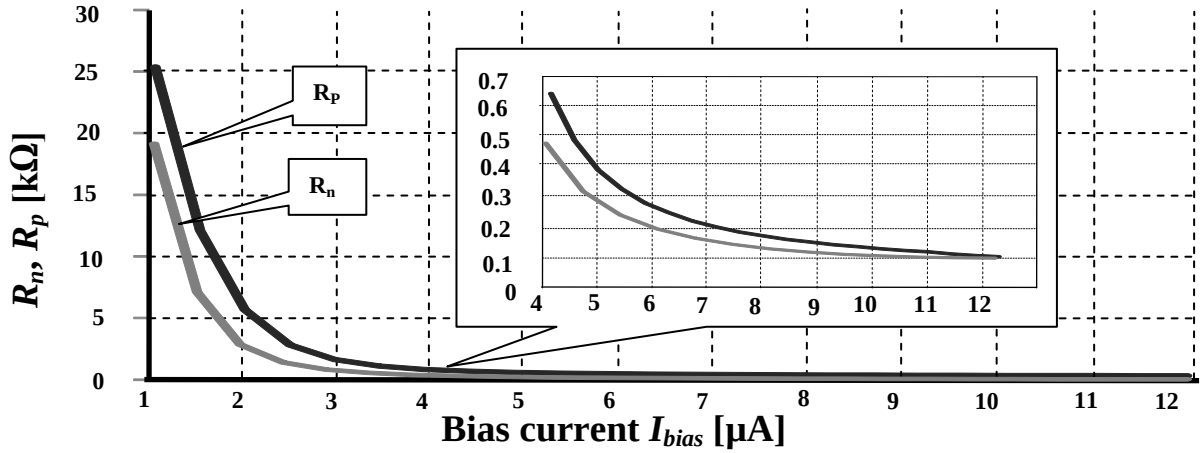


Fig. 3.58. Parasitic resistances R_p and R_n versus the bias current I_{bias}.

Moreover, the parasitic input resistances R_p, R_n can be adjusted via the bias current I_{bias} as it is shown in Fig. 3.58. Hence designers started to utilize these resistances instead of the passive resistors in several applications. Parasitic input resistances R_p, R_n can be described by:

$$R_{n,p} = \frac{1}{g_{m3,7} g_{mb1,5} r_{ds3,7}} . \tag{3.51}$$

3.5.1.1 BD–ZC–CC–CDBA–based universal filter

A current mode universal filter based on ZC–CC–CDBA is introduced in this section to confirm the functionality of the proposed circuit [94]. The multi–function current mode filter is depicted in Fig. 3.59. This filter performs three functions simultaneously: low pass, high pass, and band pass with high output impedance property. The parasitic resistances (R_{p1}, R_{n1}) of the ZC–CC–CDBA$_1$, (R_{p2}, R_{n2}) of the ZC–CC–CDBA$_2$, and (R_{p3}, R_{n3}) of the ZC–CC–CDBA$_3$ can be tuned via bias currents: I_{B1}, I_{B2}, and I_{B3}, respectively. The output currents I_{HPF}, I_{BPF} and I_{LPF} of this filter are flowing out the zc$_1$, zc$_2$ and zc$_3$ terminals, respectively. These currents are flowing into the working impedances directly.

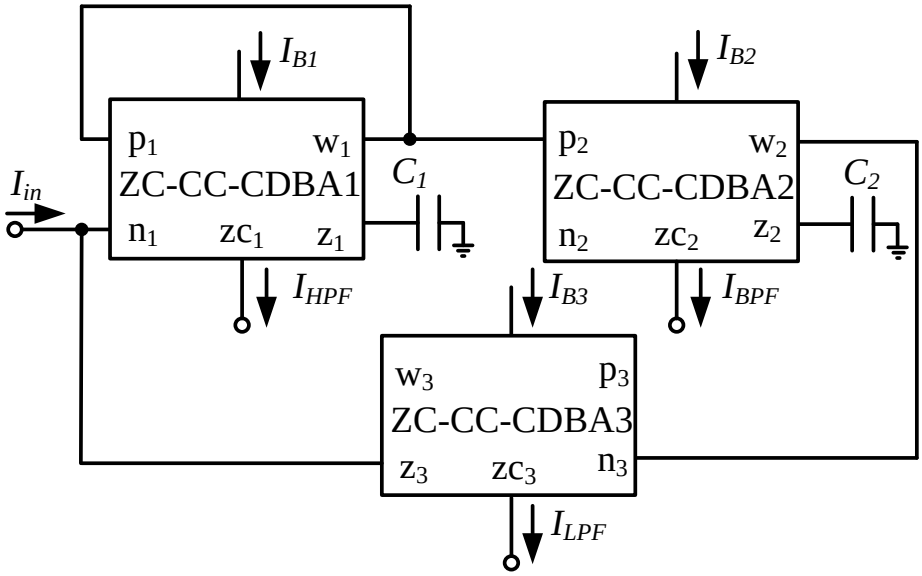


Fig. 3.59. Current mode biquad filter based on ZC–CC–CDBA.

The transfer functions of the filter are given by:

$$\frac{I_{HPF}}{I_{in}} = \frac{S^2}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad . \tag{3.52}$$

$$\frac{I_{BPF}}{I_{in}} = \frac{-S/C_1 R_{P2}}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad . \tag{3.53}$$

$$\frac{I_{LPF}}{I_{in}} = \frac{-1/C_1 C_2 R_{P2} R_{n3}}{S^2 + S\frac{1}{C_1 R_{P1}} + \frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad . \tag{3.54}$$

The pole frequency (ω_0) and the quality factor (Q) of the filter are described by:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_{P2} R_{n3}}} \quad . \tag{3.55}$$

$$Q = R_{P1}\sqrt{\frac{C_1}{C_2 R_{p2} R_{n3}}} \quad . \tag{3.56}$$

It is obvious from (3.55) and (3.56), that the quality factor Q can be adjusted independently from the pole frequency ω_0 by adjusting the value of R_{p1} via I_{B1}. Thus, the parameter Q can be orthogonal controlled.

3.5.1.2 Simulation results

The performances of the proposed ZC–CC–CDBA shown in Fig. 3.57 were simulated using PSpice simulator. The circuit was simulated using the 0.18 µm TSMC CMOS parameters [41]. The optimal transistors aspect ratios of the proposed circuit are listed in Tab. 3.19. The most important features of the proposed ZC–CC–CDBA are listed in Tab. 3.20.

All the simulations were performed for I_{bias}= 3 µA, I_B = 4 nA with an extremely low voltage supply of 0.65 V. The DC curves $I_{z,zc}$ versus I_n and I_p are depicted in Fig. 3.60. Thanks to utilizing enhanced BD current mirror, the proposed circuit offers high linearity of I_z versus I_n and I_p with extremely low current offset whose value is less than 0.05 µA. The DC curves I_z versus I_p for various values of I_n are shown in Fig. 3.61, whereas the current I_n vary from –3 µA to 3 µA with a step of 1 µA. The frequency responses of the current gains $I_{z,zc}/I_n$ and $I_{z,zc}/I_p$ are shown in Fig. 3.62. The current gains are unity at low frequencies. The cutoff frequencies of these gains are 2.4 MHz and 5.15 MHz of $I_{z,zc}/I_n$ and $I_{z,zc}/I_p$, respectively.

The frequency dependence of the parasitic impedance of the z terminal is shown in Fig. 3.63. The impedance of z terminal is very high about 2.67 MΩ at low frequencies.

The DC curve V_w versus V_z is shown in Fig. 3.64. Besides, the voltage error is depicted. The high linearity and the wide range operation can be observed. Furthermore, in the range from 0.04 V to 0.58 V, the voltage error is less than 1 mV. The frequency response of the voltage gain V_w/V_z is clarified in Fig. 3.65. The AC simulation is performed using capacitive load of 1pF. The cutoff frequency is 11.18 MHz with unity gain at low frequencies. The frequency response of the parasitic impedance of w terminal is depicted in Fig. 3.66. The value of this impedance at low frequencies is 1 kΩ.

The simulation results of the multi–function current mode biquad filter shown in Fig. 3.59 are depicted in Fig. 3.67, Fig. 3.68 and Fig. 3.69. The three ZC–CC–CDBAs are biased by I_{B1} = I_{B2} = I_{B3} = 1 µA. The components of the filter are C_1 = 5 nF and C_2 = 10 nF. That yields the pole frequency of 950 Hz, while the calculated pole frequency from (3.55) is 1 kHz. Thus the deviation is 5.2%. This error comes from the non–ideal parasitic properties of the ZC–CC–CDBA. The frequency responses of the current gains of the filter shown in Fig. 3.59 are presented in Fig. 3.67 for R_{load} = 1 Ω. It is obvious that this filter can provide low pass, band pass and high pass functions simultaneously, without any change in the circuit topology. The band pass gain responses for various values of I_{B1} are depicted in Fig. 3.68. It can be observed that by adjusting the R_{p1} value via I_{B1}, the quality factor can be tuned independent from the pole frequency as it was clarified in (3.55) and (3.56).

Moreover, Fig. 3.69 depicts the band pass filter gain responses for (I_{B1} = I_{B2} = I_{B3} = 0.5 µA, 1 µA and 1.5 µA), it is noticeable that the pole frequency can be adjusted without affecting the quality factor as it was described in (3.55) and (3.56).

Tab. 3.19. The transistors aspect ratios of the circuit shown in Fig. 3.57.

Transistor	W/L [µm/µm]
M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_{b5}, M_{b6}	15/1.5
M_9, M_{10}, M_{11}	80/3
M_3	3/0.3
M_7	8/0.3
M_1, M_2	40/2
M_5, M_6, M_{12}	40/3
M_4, M_8	80/1
M_{15}	20/3
M_{13}, M_{14}	30/3
M_{16}	15/3

Tab. 3.20. The most important characteristics of the circuit in Fig. 3.57.

Parameter	Value
Voltage supply, bias current	0.65 V, 3 µA
Power consumption for I_{bias}=3 µA	17 µW
3 dB bandwidth of $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	5.15 MHz, 2.4 MHz
Current offset	<50 nA
Current gains $I_{z,zc}/I_p$, $I_{z,zc}/I_n$	1.1
3 dB bandwidth of V_w/V_z	11.18 MHz
Voltage gain V_w/V_z	1
Voltage offset	<1 mV
Resistance of terminal Z	2.67 MΩ
Resistance of terminal w	1 kΩ

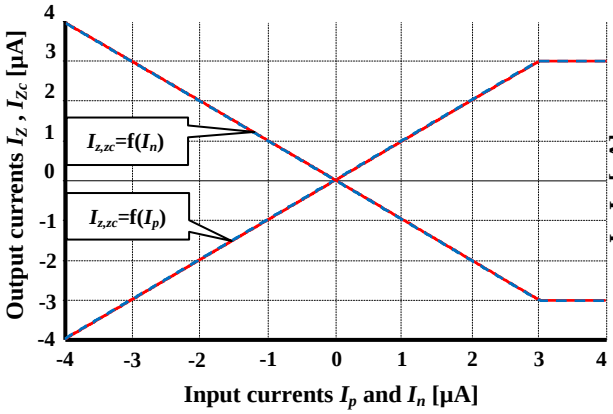


Fig. 3.60. DC curves I_z, I_{zc} versus I_p and I_n.

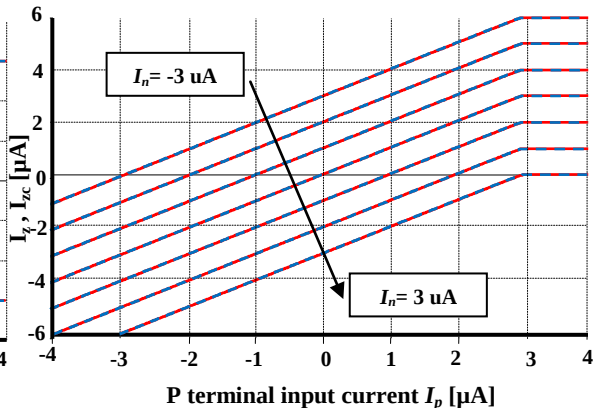


Fig. 3.61. DC curves I_z, I_{zc} versus I_p for various values of I_n.

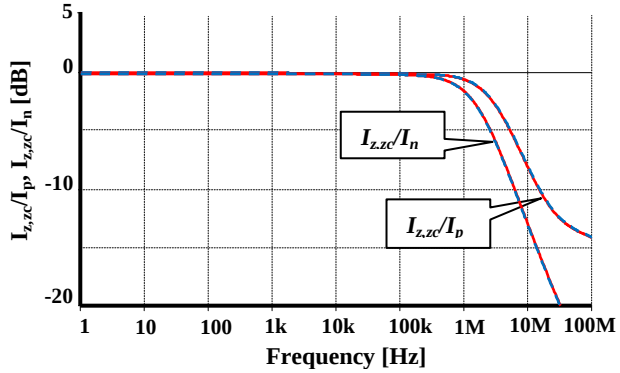


Fig. 3.62. Frequency responses of the current gains $I_{z,zc}/I_p$, $I_{z,zc}/I_n$.

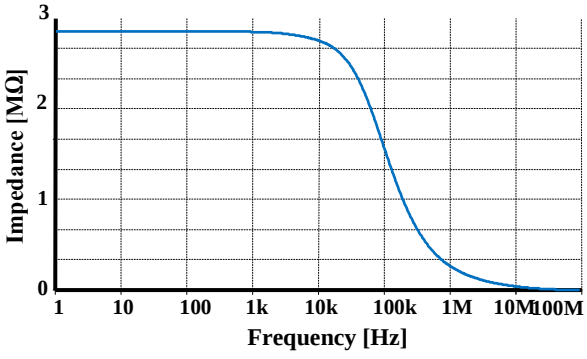


Fig. 3.63. Frequency response of the parasitic impedances of z and zc terminals.

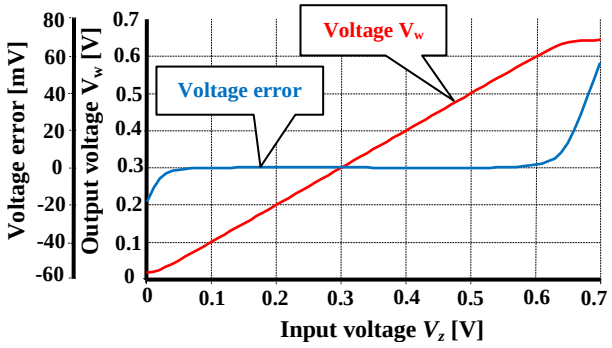


Fig. 3.64. DC curves V_w versus V_z and the voltage error.

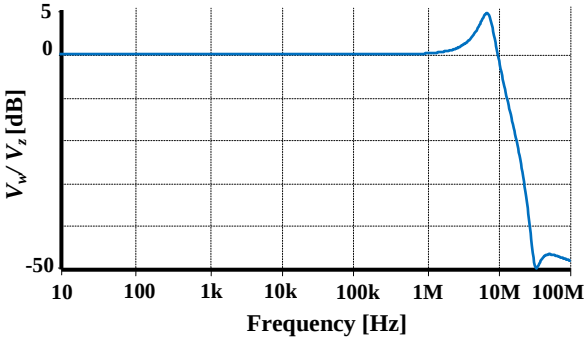


Fig. 3.65. AC curve of the voltage gain V_W/V_Z.

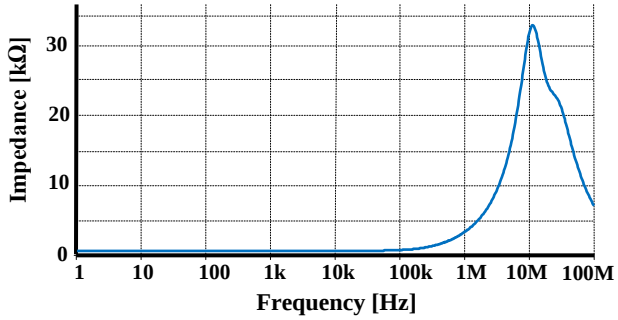


Fig. 3.66. Frequency dependence of the parasitic impedance of w terminal.

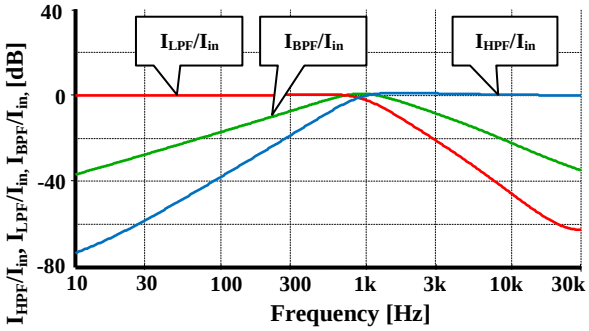


Fig. 3.67. Frequency response of the proposed filter.

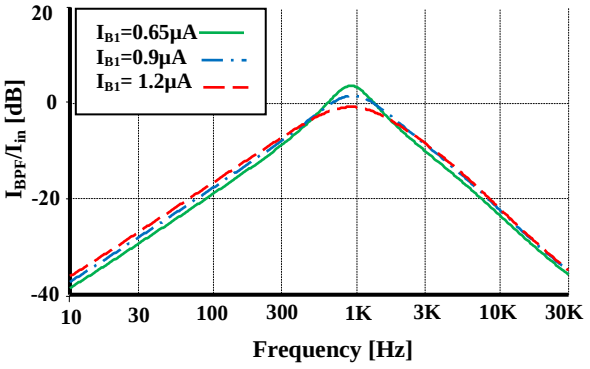


Fig. 3.68. The response of the band pass filter for different I_{B1} values.

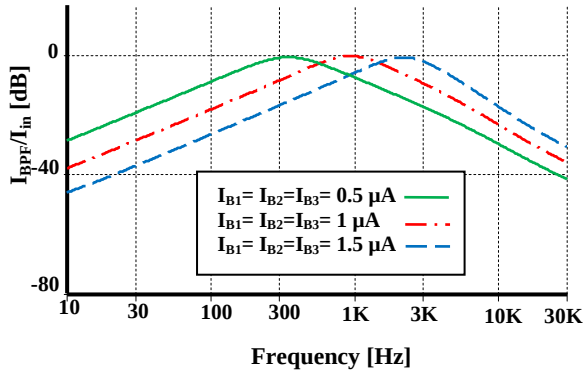


Fig. 3.69. The response of the band pass filter for different values of I_{B1}, I_{B2} and I_{B3}.

3.6. CURRENT FEEDBACK OPERATIONAL AMPLIFIER (CFOA)

The current feedback operational amplifier (CFOA) is a one of the most important and versatile active building blocks for realizing analog signal processing circuits. The CFOA has the second–generation current conveyor as an input stage and is followed by voltage follower as an output stage. This property makes it suitable for realizing both voltage–mode and current–mode analog signal processing circuits. Compared with voltage–mode operational amplifier, this device exhibits higher speed and better bandwidth. As a result, many CFOA–based circuits have been proposed such as filters, oscillators, gyrators and floating immittances; see, for example, [95–100].

The circuit symbol of conventional CFOA is shown in Fig. 3.70. The relationships of the terminals of ideal CFOA can be described as:

$$\begin{pmatrix} I_y \\ V_x \\ I_z \\ V_o \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \\ I_o \end{pmatrix}, \tag{3.57}$$

where y and x are the input terminals whereas z and o are the output terminals. For the ideal CFOA, the impedance level of the x and o are zero whereas the y and z terminals have infinite impedances. From (3.57), the relation of x, y and z terminals are properties of second generation current conveyor whereas the realization between z and o is the voltage follower.

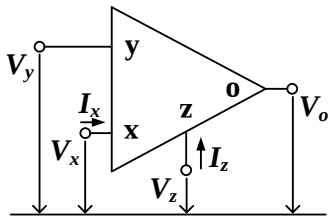


Fig. 3.70. Circuit symbol of CFOA.

3.6.1. Floating–gate differential difference current feedback operational amplifier (FG–DD–CFOA)

There are several CFOAs introduced in open literature [40], [47], [101–104]. Unfortunately, these CFOAs do not meet the needs of low voltage (LV) supply and low–power (LP) consumption applications.

A new LV supply and LP consumption CFOA using floating–gate technique is proposed here. The floating–gate (FG) technique is used to provide a low–voltage supply. By the use of floating–gate technique, differential difference voltage of CFOA can be easily obtained and hence the name floating–gate differential difference CFOA (FG–DDCFOA). Unlike the previous CFOA, the arithmetic operation capability of voltage signals of the proposed circuit can be obtained. The proposed building–block is designed using 0.18 µm CMOS technology. The supply voltage of a 0.8 V can be used. Simulation results show that the power consumption of the proposed CFOA is 20 µW. Thus, the circuit can be used in ultra–low–power applications such as bioelectronics, biosensor and biomedical system. The proposed CFOA is used to realize LV LP universal filter as an example application as will be shown shortly.

The proposed FG–DDCFOA is shown in Fig. 3.71. It consists of two pasts (differential difference current conveyor (DDCC) and voltage follower (VF)). The DDCC is consisted of M_1 to M_{14} whereas the voltage follower is consisted of M_{15} to M_{23}. Transistors M_1–M_2 and M_{15}–M_{16} perform two differential amplifiers for DDCC and VF, respectively. The differential input stages are the FG flipped voltage follower. Transistors M_4, M_7, M_8, M_{18}, M_{19} and M_{20} act as a multiple output current mirror for applying the constant current source

I_{bias} to each branch of the output stages. The power consumption of the proposed circuit can be controlled appropriately by setting I_{bias} and V_{DD}. Transistors M_3 and M_{17} act as tail current source for the first (M_1, M_2) and second (M_{15}, M_{16}) differential input stages, respectively. The output stage of differential input stage is created by cascoding transistors M_9 and M_7, M_{11} and M_{13}. These cascode transistors are used to support that the unity voltage transfer function between x and y terminal will be obtained. On the other hand, the cascode transistors M_{10} and M_8, M_{12} and M_{14} create the output stage for the DDCFOA at the output z. Also the use of cascode technique makes the proposed circuit provides a high resistance value for z terminal. The second part of the proposed circuit is a voltage follower that consists of M_{15} to M_{17} and M_{20} to M_{23} which is constructed from the input stage of differential difference current conveyor (DDCC) in order to realize the required voltage following between terminals z and o. Compared with previously CFOAs, the proposed circuit has the DDCC as an input stage and is followed by a voltage follower as an output stage. This device has all the good properties of the DDCC, such as high–input impedance, employs fewer active and passive components and easy implementation of arithmetic operation of voltage signals.

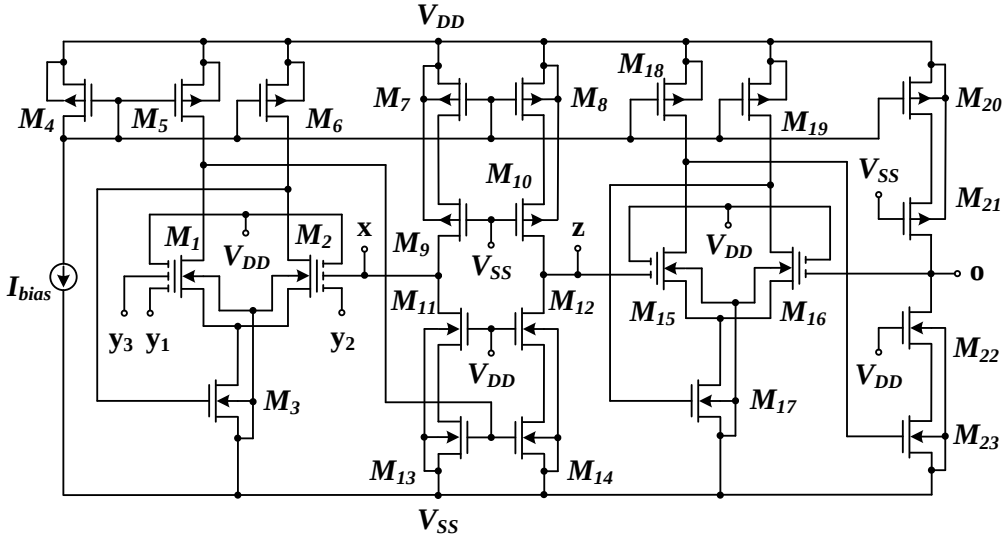


Fig. 3.71. Proposed FG–DDCFOA.

The circuit symbol of the conventional DDCFOA and the proposed FG–DDCFOA are shown in Fig. 3. 72 (a) and (b), respectively.

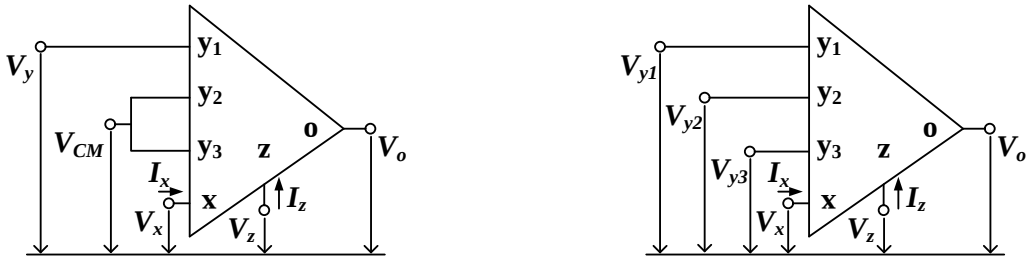


Fig. 3.72. Symbol of: conventional DDCFOA (a) DDCFOA and (b) proposed FG–DDCFOA.

3.6.1.1 FG–DDCFOA–based universal filter

The proposed FG–DDCFOA is used to realize voltage–mode universal filter as an example application. The circuit is shown in Fig. 3.73. This filter employs two FG–DDCFOAs, two grounded capacitors and two grounded resistors. Using (3.57), the output signals V_{o1}, V_{o2} and V_{o3} of Fig. 3.73 can be obtained as:

$$V_{o1} = \frac{s\left(\frac{1}{R_1C_1}\right)V_{in1} + \left(\frac{1}{R_1R_2C_1C_2}\right)V_{in2}}{D(s)}, \tag{3.58}$$

$$V_{o2} = \frac{\left(s\frac{1}{R_2C_2} + \frac{1}{R_1R_2C_1C_2}\right)V_{in2} - \left(\frac{1}{R_1R_2C_1C_2}\right)V_{in1}}{D(s)}, \tag{3.59}$$

$$V_{o3} = \frac{s^2V_{in1} + \left(s\frac{1}{R_1C_1}\right)V_{in2}}{D(s)}, \tag{3.60}$$

where $D(s) = s^2 + s\frac{1}{R_1C} + \frac{1}{R_1R_2C_1C_2}$. (3.61)

It is clear from (3.58)–(3.60), the filtering functions can be obtained by appropriately connecting the input and the output terminals. As an example, the BPF, LPF and HPF can be obtained, respectively, as:

- BPF: $V_{in1} = V_{in}$, $V_{in2} = V_{CM}$ and $V_{o1} = V_{out}$.
- LPF: $V_{in1} = V_{in}$, $V_{in2} = V_{CM}$ and $V_{o2} = V_{out}$.
- HPF: $V_{in1} = V_{in}$, $V_{in2} = V_{CM}$ and $V_{o3} = V_{out}$.

It should be noted that these filtering functions are obtained with high–input and some low–output impedances. For achieve five standard filtering functions, an additional FG–DDCFOA is needed. This is the advantage of this active building block that provides the arithmetic operation capability of voltage signals. The natural frequency (ω_o) and the quality factor (Q) can be given by

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}}. \tag{3.62}$$

$$Q = \sqrt{\frac{R_1C_1}{R_2C_2}}. \tag{3.63}$$

From (3.62) and (3.63), the parameter Q can be given by setting the ratio of C_1/C_2 and parameter ω_o can be controlled by setting resistors R_1 and R_2, simultaneously, while keeping the ratio of C_1/C_2 constant.

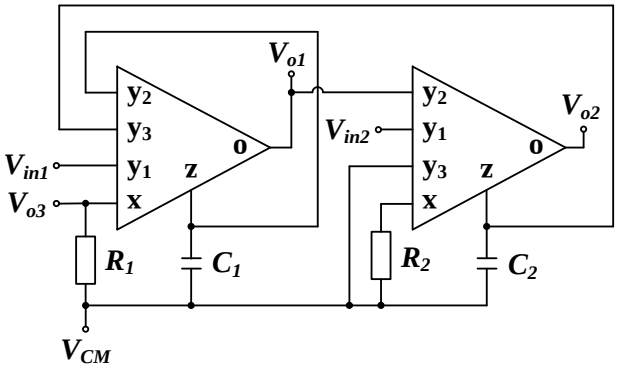


Fig. 3.73. FG–DDCFOA–based universal filter.

3.6.1.2 Simulation results

The proposed FG–DDCFOA was simulated using a 0.18 μm TSMC *N*–well CMOS process. The transistor aspect ratios of Fig. 3.71 were listed in Tab. 3.21. All resistances were 100 GΩ and all capacitances were 200 fF for floating–gate MOSTs M_1 M_2, M_{15} and M_{16}. The supply voltages were 0.8 V (V_{DD} = 0.8 V and V_{SS} = 0 V), the biasing current I_{bias} and the common–mode voltage V_{CM} were respectively taken as 0.2 μA and 0.4 V. The DC characteristic of the proposed circuit was investigated by connecting x and z terminals with 50 kΩ of resistance. Figs. 3.74, 3.75 and 3.76 show the V_x versus V_{y1}, I_z versus V_{y1} and V_o versus V_{y1}, respectively, when V_{y2} was changed in step (0.05 V) from –0.2 to 0.2 V. The other performances of the proposed circuit were summarized as Tab. 3.22.

Tab. 3.21. Transistor aspect ratios for Fig. 3.71.

MOS transistors	W/L(μm/μm)
M_1, M_2, M_{15}, M_{16}	1/0.5
M_3, M_{17}	0.4/1
M_4	6/1
M_5, M_6, M_{18}, M_{19}	3/1
M_7, M_8, M_{20}	150/0.3
M_9, M_{10}, M_{21}	100/2
M_{11}, M_{12}, M_{22}	50/2
M_{13}, M_{14}, M_{23}	8/0.3

Tab. 3.22. Summarized Performances of Proposed FG–DDCFOA.

Parameters	Value
Technology	0.18 μm
Supply voltage	0.8 V
Common–mode voltage (V_{CM})	0.4 V
DC voltage range	–390 mV to 390 mV
DC current range	–8 μA to 8 μA
–3dB bandwidth voltage follower V_x/V_y ($V_y=V_{y1}=V_{y2}=V_{y3}$) V_o/V_z	 ≤ 19 MHz ≤ 32 MHz
–3dB bandwidth current follower	≤ 19 MHz
R_{y1}, R_{y2}, R_{y3}, C_{y1}, C_{y2}, C_{y3}	99 GΩ, 200 fF
R_x, L_x	577 Ω, 1 mH
R_z, C_z	9.2 MΩ, 0.27 pF
R_o, L_o	1.28 kΩ, 0.91 mH
Power dissipation	20 μW

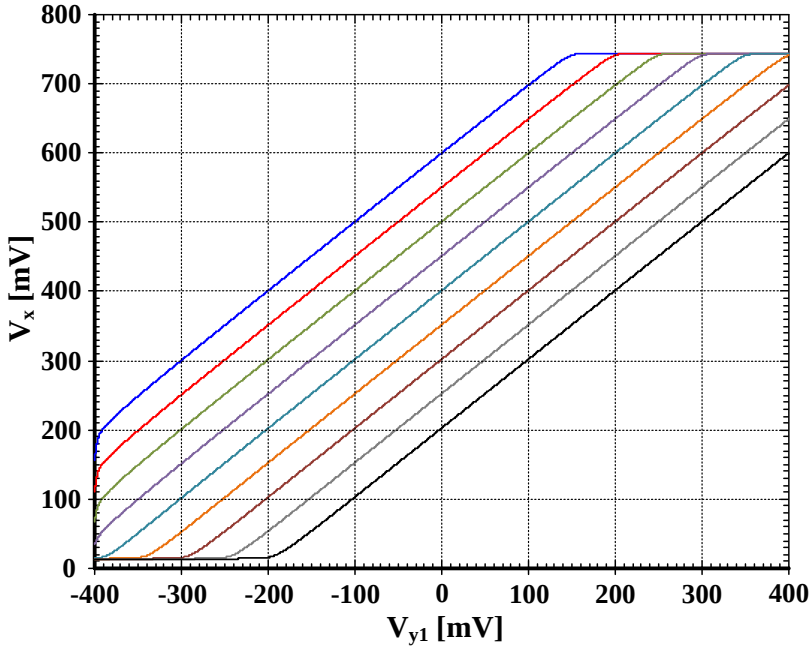


Fig. 3.74. Simulated V_x versus V_{y1} when V_{y2} is parameter.

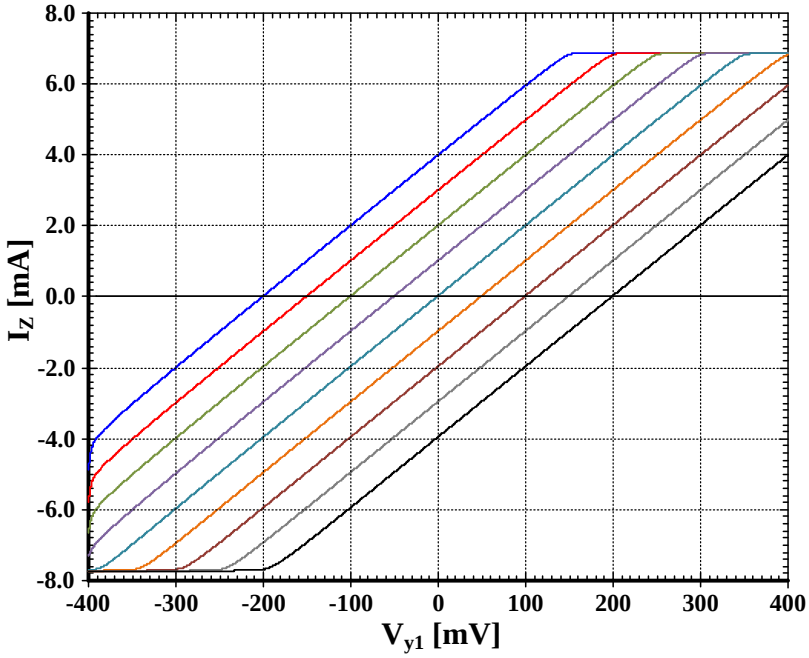


Fig. 3.75. Simulated I_z versus V_{y1} when V_{y2} is parameter.

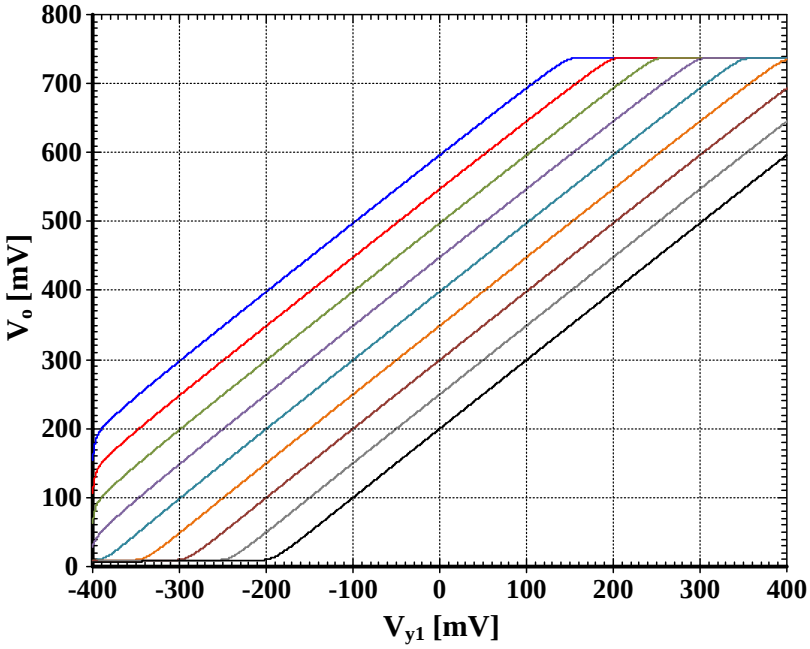


Fig. 3.76. Simulated V_o versus V_{y1} when V_{y2} is parameter.

The universal filter in Fig. 3.73 was also simulated. The proposed FG–DDCFOA in Fig. 3.71 was used. As an example design, $C_1 = C_2 = 50$ pF and $R_1 = R_2 = 330$ kΩ were given. This setting has been designed to obtain the BPF, LPF and HPF responses with $f_o = 10$ kHz and $Q = 1$. The simulation result for the BPF, LPF, and HPF characteristics is shown in Fig. 3.77. For these results the power consumption of only 40.6 μW was obtained. In order to test the input dynamic range of the filter, the simulation has been repeated for a sinusoidal input signal at $f_o \cong 10$ kHz. Fig. 3.78 shows that the input dynamic range of the BPF response extends up to amplitude of 130 mV (peak–to–peak) without signification distortion. The total harmonic distortion (THD) is about 1.1 % from this figure.

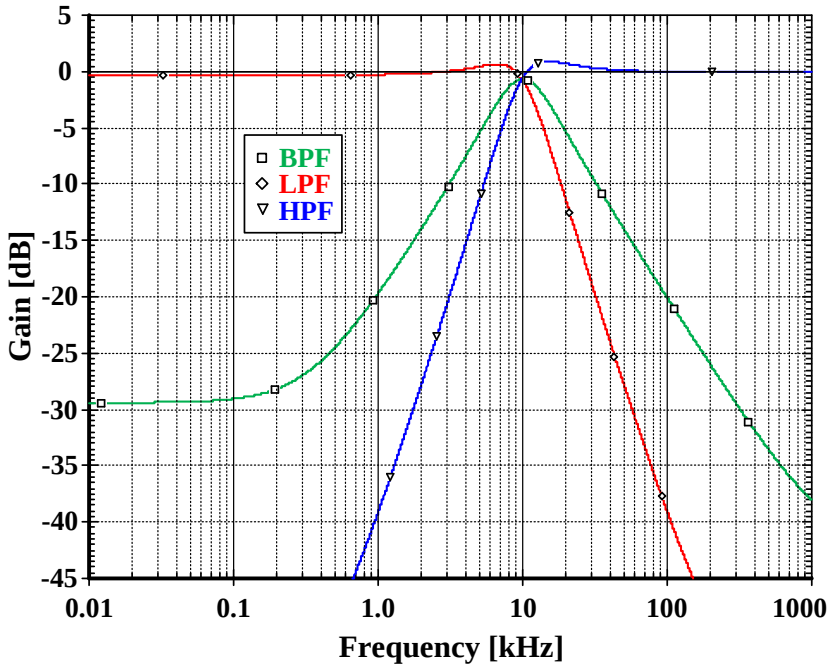


Fig. 3.77. Simulated magnitude response of BP, LP and HP filters.

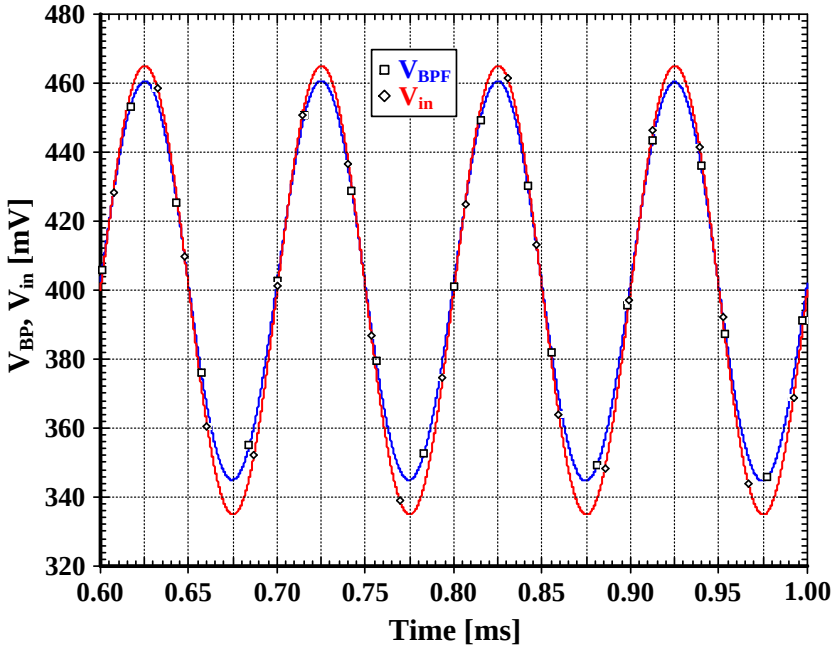


Fig. 3.78. The input and output waveforms of the BPF response for a 10 kHz sinusoidal input voltage of 130 mV (peak–to–peak).

3.7. SUB–CONCLUSION

In this chapter, new designs of active elements were designed by utilizing low–voltage low–power techniques. CMOS internal structure with simulation plots were proposed to verify the behavior of the presented LV LP circuits.

In paragraph 3.1, two operational transconductance amplifiers (OTAs) were presented. The first OTA was designed utilizing bulk–driven quasi–floating–gate (BD QFG) MOSTs and was verified by implementing a diode–less rectifier based on it. Whereas the second Ota was designed using floating–gate (FG) MOSTs and was verified by implementing an active element voltage differencing transconductance amplifier (VDTA), as well as low–pass and band–pass filters, based on it.

In paragraph 3.2, the well–known second generation current conveyor (CCII) was designed using bulk–driven (BD) MOSTs. The BD–CCII was confirmed by proposing conductance simulations based on it.

In paragraph 3.3, two fully–differential CCIIs (FD–CCIIs) were proposed. The first FD–CCII was proposed utilizing BD MOSTs. The proposed BD FD–CCII then was verified by realizing universal filter based on it. The second FD–CCII was designed using BD QFG MOSTs and was confirmed by applying a universal filter based on it.

In paragraph 3.4, a fully–balanced differential difference amplifier (FB–DDA) was proposed. BD QFG MOSTs were used to implement the circuit. Then a band–pass filter based on it was designed to confirm the functionality of the proposed BD–QFG FB–DDA.

In paragraph 3.5, a z–copy current–controlled current differencing buffered amplifier (ZC CC CDBA) was designed using BD MOSTs, then a universal filter was proposed based on it.

In paragraph 3.6, a differential difference current feedback operational amplifier (DD CFOA) was designed using FG MOSTs and a universal filter based on it was realized to confirm its functionality.

All active elements and application examples have been confirmed by PSpice simulator using the 0.18 μm TSMC CMOS parameters [41].

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4. CONCLUSION

The recent trend towards miniaturized circuits and portability of electronic equipment has given a strong and decisive boost towards the design of low–voltage low–power analog circuits. Without a doubt, operating at low voltage levels is one of the most critical issues challenging analog circuit designers. Consequently, nowadays, it has become a trend that catches eye of the designer. The difficulty of low voltage design consists of maintaining the most important characteristics of circuit's performance without altering it. Generally, characteristics such as the linearity, the gain, the input common mode range, the dynamic range, rail–to–rail operation, and other features have to be implemented to maximum in order for circuit to be applicable and in such way desirable.

This dissertation thesis consists of four sections:

Section 1 is the introduction of the thesis, it illustrates why and where we need LV LP analog circuits design.

Section 2 a state–of–the–art of developed technologies, conventional techniques and non–conventional techniques could be implemented to obtain LV LP circuits is done. Developed technologies used for LV LP IC design are: CMOS technology, BiCMOS technology, SOI (Silicon On Insulator) technology and multi–gate transistors. Conventional LV LP techniques include circuits with rail–to–rail operation range, MOSTs operating in weak inversion region, level shifter technique and MOSTs in self–cascode structure. Non–conventional LV LP techniques include bulk–driven, floating–gate, quasi–floating–gate, bulk–driven floating–gate and bulk–driven quasi–floating–gate approaches.

In section 3, circuits along with application examples are presented to demonstrate their functionality as designed using LV LP techniques. Circuits include well–known active elements such as Operational Transconductance Amplifier (OTA) and Second Generation Current Conveyor (CCII), and other active elements such as Voltage Differencing Transconductance Amplifier (VDTA), Fully Differential Current Conveyor (FD CCII), Fully Balanced Differential Difference Amplifier (FB DDA), Current Controlled Current Differencing Buffered Amplifier (CC CDBA) and Differential Difference Current Feedback Operational Amplifier (DD CFOA). Whereas application examples include diode–less precision rectifier, inductance simulation, as well as low–pass, band–pass and universal filters.

Finally in section 4 of the dissertation thesis, a conclusion is drawn.

However, as it turns out from the thesis, each low–voltage low–power technique has its advantages and disadvantages as concluded in 2.2. The thesis focused on designing LV LP circuits depending on both: LV LP techniques and LV LP building blocks. Utilizing LV LP configurations connected in a way that makes voltage biasing requirements lower, such as flipped voltage follower, is a suitable method in order to achieve LV LP capability. Thus, combination of LV building blocks and LV techniques simultaneously gives an excellent

solution to implement LV LP configurations and to overcome some of LV LP techniques' drawbacks. By following this strategy, the voltage supply was reduced down to approximately 0.5–0.6 V and the power consumption was reduced down to less than 20 μW almost in all circuits. Moreover, all circuits were stable, had rail–to–rail operation, and were very suitable for low–frequency applications such as biomedical applications.

The main goal of this thesis was to design and simulate novel CMOS structures of basic building blocks and active elements so they can operate at very low power supply voltage levels (average of 0.6 V) and consume very low power (average of 20 μW) for 0.18 μm CMOS technology, extending common–mode dynamic range while preserving other characteristics acceptable for many applications. With respect to above mentioned discussions, it is declared that aims of this thesis were fulfilled.

Finally, in my opinion, the trade–off between the perfect performances and the optimal biasing conditions is inevitable issue, but designers still have the opportunity to create LV LP configurations with the top performance to its maximum.

5. Curriculum Vitae

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Personal Details

Date of Birth	13 May 1984
Nationality	Syrian
Marital status	Single

Language skills

Arabic	Mother tongue
English	Excellent knowledge of speaking, reading and writing
Czech	Good knowledge of speaking and reading
German	Basic knowledge of speaking and reading

Objectives

To secure a challenging **position in the field of telecommunications or analog circuits design within** a **progressive reputable organization**, which facilitates professional growth and utilization of my qualification and experience, while embracing new methodologies & strategies to remain competitive in the market

Education

2011 - now	Brno University of Technology, Faculty of Electrical Engineering and Communication, Czech Republic, doctoral degree in Microelectronics
	Successfully passed the 2nd year doctoral state exam

2003–2010	Al-Baath University, Faculty of Electrical and Mechanical Engineering, Department of Electrical and Communication Engineering, Syria, diploma degree in Electronic & Communication Engineering *Nostrificated as an engineering degree by Brno University of Technology*

Professional Training Courses

- CBT Nuggets Cisco CCNA Training
- CBT Nuggets Cisco CCNP BSCI
- CBT Nuggets Microsoft MCSE
- MTN Syria special training course including Network Planning and Management, Maintenance and Configuring Devices
- Several courses in English language

Undergraduate and postgraduate projects

4th year project	Design and implementation of AM radio receiver
5th year project	High–range laser digital transmitter of audio signals with encryption and signalisation of interception
Ph.D. thesis	Low voltage low power analog circuits design

Technical skills

Mobile networks	Cellular communication systems (2G, 2.5G, 3G, 3.5G, 4G) and specially GSM & UMTS as well as MSS (Mobile Satellite Services)
Switches	Addressing, trunk, VLANs, VTP and subbnetting. Experience with Cisco Catalyst Series Switches 2950 and 1900
Security	IP access lists (standard and extended)
Routers	Experience with Cisco 1700 and 2600 Series Routers
Routing protocols	Static routing, RIP (v1, v2), IGRP, EIGRP, OSPF, ISIS, BGP and in WANs: frame relay, ISDN. Beside PPP & Chap, telnet, Nat and PAT
Circuit design	Excellent knowledge in analog circuits design, especially low-voltage low–power circuits

Software skills

Circuits design and simulation	PSpice, Eagle, Cadence Virtuoso, Cadence Spectre, Orcad, Workbench/Multisim, Micro-Cap, SNAP
Programming and scripting languages	Turbo Pascal, C/C++, Matlab/Simulink, Assembler

Research and teaching experience

Since 2011	Teaching assistant at Brno University of Technology, Department of Microelectronics. Taught courses: *Analogue electronic circuits* (practicals), *Modelling and Computer Simulation* (practicals)
Published papers in international journals	-ALSIBAI, Z. Floating- Gate Operational Transconductance Amplifier. *International Journal of Information and Electronics Engineering*, 2013, vol. 2013 (3), no. 4, p. 361-364. ISSN: 2010– 3719
	-ALSIBAI, Z. Floating- Gate MOSFET Based Tunable Voltage Differencing Transconductance Amplifier and Its Application to Biquad Filters. *International Journal of Engineering Sciences and Research Technology*, 2013, vol. 2013 (2), no. 4, p. 772–777. ISSN: 2277–9655
	-B. A. DABBOUS, S and ALSIBAI, Z. Ultra-Low Voltage Low Power Bulk Driven Z Copy-Current Controlled–Current Differencing Buffered Amplifier. *International Journal of Electronics and Electrical Engineering*, 2014, vol. 2014 (2), no. 3, p. 229-234. ISSN: 2301–380X

Hobbies

Playing piano, listening to music, watching and playing sports, writing poetry and reading