BRNO UNIVERSITY OF TECHNOLOGY
Faculty of Electrical Engineering and Communication
Department of Microelectronics

Ing. Mahmoud Shaktour

UNCONVENTIONAL CIRCUIT ELEMENTS FOR LADDER FILTER DESIGN

Nekonvenční obvodové prvky pro návrh příčkových filtrů

SHORT VERSION OF PH.D.THESIS

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KLÍČOVÁ SLOVA

Analogové zpracování signálů, proudový mód, napěťový mód, kmitočtový filtr, fázovací článek 1. řádu, univerzální filtr, KHN, simulátor plovoucího induktoru, OTA, CCII, CDTA, DVCC, VDTA, VDVTA.

The manuscript of this thesis is deposited and available:
at the Department of Microelectronics
Faculty of Electrical Engineering and Communication
Brno University of Technology
Technická 3058/10, 616 00 Brno, Czech Republic
Tel.: +420 541 146 340
Fax: +420 541 146 300
E-mail: info@feec.vutbr.cz

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INTRODUCTION

Filters are widely used in analog signal processing [1] to select the particular frequency. Voltage-mode and current-mode circuits such as current conveyors [2] and current feed back operational amplifiers [3] are getting much attention as compared to other active elements due to wider bandwidth, simple circuitry, low power consumptions and dynamic ranges.

In the last decade, a huge number of active building blocks were introduced for analogue signal processing. However, there is still the need to develop new active elements that offer new and better advantages. This thesis is, therefore, focused on definition of other novel analog building blocks (ABBs) and, furthermore, novel filter structure designs.

In the present days, a number of trends can be noticed in the area of analogue filter and oscillator design, namely reducing the supply voltage of integrated circuits and transition to the current-mode [4]. On the other hand, current-, voltage- and mixed-mode analog circuits design still receives considerable attention of many researches. Therefore, the proposed circuits in this work are working in current-, voltage-, or mixed-mode.

1. State of the art

In the last decade, a huge number of active building blocks (ABBs) were introduced for analogue signal processing.

Due to disadvantages of conventional inductors, active element-based inductor design is very desirable to designers today. During the last few decades, various floating inductors have been created using different high-performance active building blocks. That is why replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design.

The current conveyor (CC) is the basic building block of a number of contemporary applications both in the current and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [5]. Two years later, today's widely used second-generation CCII was described in [6], and in 1995 the third-generation CCIII [7]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (Op Amp) were not widely appreciated and any IC implementation of Current Conveyors was not available commercially as an off-the-shelf item.

Today, the current conveyor is considered a universal analog building block with wide spread applications in the current-, voltage-, and mixed-mode signal processing. Its features

find most applications in the current mode, when its so-called voltage input *y* is grounded and the current, flowing into the low-impedance input *x*, is copied by a simple current mirror into the *z* output.

The demand for a multiple-output current conveyor led to the DO-CCII (Dual-Output CCII), which provides currents Iz of both directions, thus combining both the positive and the negative CCII in a single device [8]. If both currents are of the same polarity, the conveyors are of the CFCCIIp or CFCCIIn types (Current Follower CCII), where the symbol p or n means positive or negative current conveyor [9]. Another generalization is represented by the so-called DVCCII (Differential Voltage Current Conveyor) [10], in which the original "voltage" input y is split into a pair of inputs y1 and y2. The voltage of the x terminal is then given by the voltage difference of the voltage inputs. This offers more freedom during the design of voltage- and mixed-mode applications.

OTA (Operational Transconductance Amplifier) [11] belongs to the most widespread active elements for on-chip implementation of fast frequency filters.

It acts as a voltage-controlled current source with the possibility of electronic adjustment of transconductance g_m.

Recently, the MO-OTA (Multiple Output OTA) has appeared as a generalization of BOTA (Bipolar OTA) and its applications in economical biquadratic filters [12], [13]. However, the drawbacks of such applications are not sufficiently emphasized. Some of them are referred to in [14]: the MO-OTA applications embody relatively high sensitivities to the attainable matching error of the current gains of the current mirrors that form the multiple output of the OTA.

Using the duality principle, the voltage conveyor (VC) has been presented in 1981 [15]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [15], [16], [17], [18]. The best known VC is the plus-type differential current voltage conveyor (DCVC+) [19] that is more often labeled as the current differencing buffered amplifier (CDBA) [20].

By the modification of the CDBA or replacement of the VF (Voltage Follower) by the operational transconductance amplifier (OTA) [21], the current differencing transconductance amplifier (CDTA) [22] has been presented.

The methodology described, which uses the CDU (Current Differencing Unit) or CF (Current Follower) or CI (Current Inverter) as the input unit, and the following simple blocks such as voltage buffer, OTA, and CCII, represents an open system.

Continuing with the variation that the input unit will now implement voltage and not current differences, the Voltage Differencing Transconductance Amplifier (VDTA) has been introduced [23].

Recently, many papers were published about the simulation of passive ladder filters via numerous types of active elements. Direct simulation via inductor replacement by a synthetic element, indirect simulation via Bruton transformation of passive RCL cell and subsequent FDNR implementation, or leap-frog techniques was used.

In such circuits, frequently used active elements are CDBAs [24-26], CAs (Current Amplifiers) [27], MCCCIIs (Multi-Output CCCIIs) [28], CDTAs [29-31], OTRAs (Operational Transresistance Amplifier) [32], VCCs (Differential Voltage Current Conveyor) [33], CCIIs and CFAs [34], [35], DO_OTAs (Differential-Output OTAs) [36], MO_OTAs (Multiple-Output OTAs) [37], and a combination of classical Operational Amplifiers and OTAs [38]. Common drawback of the above circuit topologies consists in the circuit complexity. For example, a floating inductor is modeled via several active devices, and the resulting filter structure contains large number of components, including floating resistors and capacitors. One exception from this rule is represented by recently introduced building block named CBTA (Current Backward Transconductance Amplifier) which enables simulating n-th order ladder filter via n CBTAs and n grounded capacitors [39], [40].

The above state-of-the-art clearly shows the topicality of the simulation of passive ladder filters via modern active elements as well as searching for such building blocks which would enable economical synthesis of artificial inductors. During the research activities towards finishing this work, it was shown that the VDTA element which was synthesized in the first stage of the research can be a good building block for designing economical ladder simulators.

2. Thesis objectives

The first aim of this thesis is to define various types of novel active building blocks for the effective synthesis of filter simulating RLC ladder structure. The second aim is to perform such a synthesis.

The first part of the thesis focuses on designing a high linearity, wideband bulk-driven OTA with tunable transconductance. This OTA is then used for designing active building blocks (CDTA, VDTA, VDVTA, and DVCC). As applications, several filters structures current-, voltage- and mixed-mode by using VDTA are presented, particularly the second-order filter structures that can provide all standard filter responses without changing the

circuit topology. Special attention is paid to Kerwin–Huelsman–Newcomb structure that enables independent control of the quality factor Q and characteristic frequency ω_0.

The second part of thesis deals with LC ladder simulation on the principle of inductor replacement by synthetic inductor.

The floating inductor is synthesized via:

1. MAX435, a commercial OTA [46], [53], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well-known circuitry for simulating the floating inductor. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.
2. „super-transistor“ (S-T), which is commercially available in several versions, e.g. OPA615, SHC615, OPA860, and OPA861 [53].
3. Newly introduced VDTA and VDVTA elements [45] designed in the first part of the thesis.

All the designs are verified in two steps:

In the first step, the theoretical analyses are done using SNAP software [41]. To verify the complex behavior of the proposed circuits, SPICE simulations are performed, utilizing transistor-level models of active elements.

3. Active building blocks and their properties

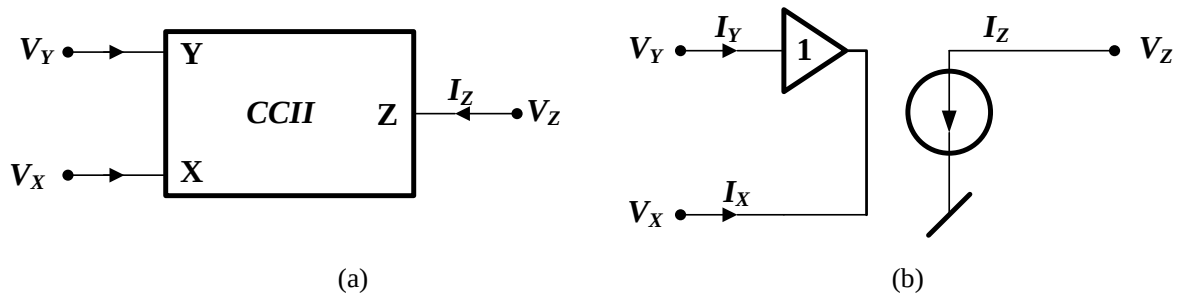
The following active elements are devices having multi ports with properties that make them useful in network synthesis [42]. Some active elements are more useful than others, depending of various design requirements.

3.1. Current Conveyor of Second Generation (CCII)

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC). The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [5]. CCI was then replaced by a more versatile second-generation device in 1970 [6], the CCII. Current conveyor designs have mainly been with BJTs due to their high transconductance values compared to their CMOS counterparts. They are used as current-feedback operational amplifiers like the MAX477 high-speed amplifier and the MAX4112 low-power amplifier, which both feature current feedback rather than the conventional voltage feedback used by standard operational amplifiers.

Current conveyors are used in high-frequency applications where the conventional operational amplifiers can not be used, because the conventional designs are limited by their gain-bandwidth product.

The second-generation current conveyor (CCII) is used as a basic building block in many current-mode analog circuits. It is a three-terminal (X, Y and Z) device as shown in Fig. 3-1 (a) and the equivalent circuit of the ideal CCII is shown in Fig. 3-1 (b).



(a) (b)

Fig. 3-1: (a) The CCII symbol, (b) ideal equivalent circuit.

The characteristics of ideal CCII are represented by the following hybrid matrix

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (3\text{-}1)$$

An ideal CCII has the following characteristics:

- Infinite input impedance at terminal Y ($R_Y = \infty$ and $I_Y = 0$)
- Zero input impedance at terminal X ($R_X = 0$)
- Accurate voltage copy from terminal Y to X ($V_X = V_Y$)
- Accurate current copy from terminal X to Z with infinite output impedance at Z ($I_Z = I_X$ and $R_Z = \infty$)

3.1.1. Bulk-driven CCII± based on Bulk-driven OTA

A new connection of Bulk-driven OTA is used to realize the CCII. In the OTA-based approach, presented in Fig.3-2, Bulk-driven OTA is used to implement the unity gain buffer between the Y and X inputs [44]. The X input current I_X is sensed by duplicating buffers' output transistors M_6 and M_7 using transistors M_8 and M_9, and extracting the X current from them as I_Z. Since transistors M_8 and M_9 have the same size and gate-source voltage as the output stage transistors M_6 and M_7, the current I_Z should be a copy of the current flowing through M_6 and M_7 which is I_X. Transistors M_{10}-M_{15} are used to generate I_Z. Since no

additional transistors need to be inserted between the OTA and rails, the approach will not increase the minimum operating voltage over that of the operational core. In addition the voltage follower is based on an OTA, thus it will maintain all the benefits and also the disadvantages of such a circuit i.e. a good voltage follower at the cost of lower bandwidth.

The simulated frequency responses of current gains I_{z+}/I_x, I_{z-}/I_x are given in Fig. 3-3. The cutoff frequencies for the gains are 20 MHz and 52 MHz, respectively.

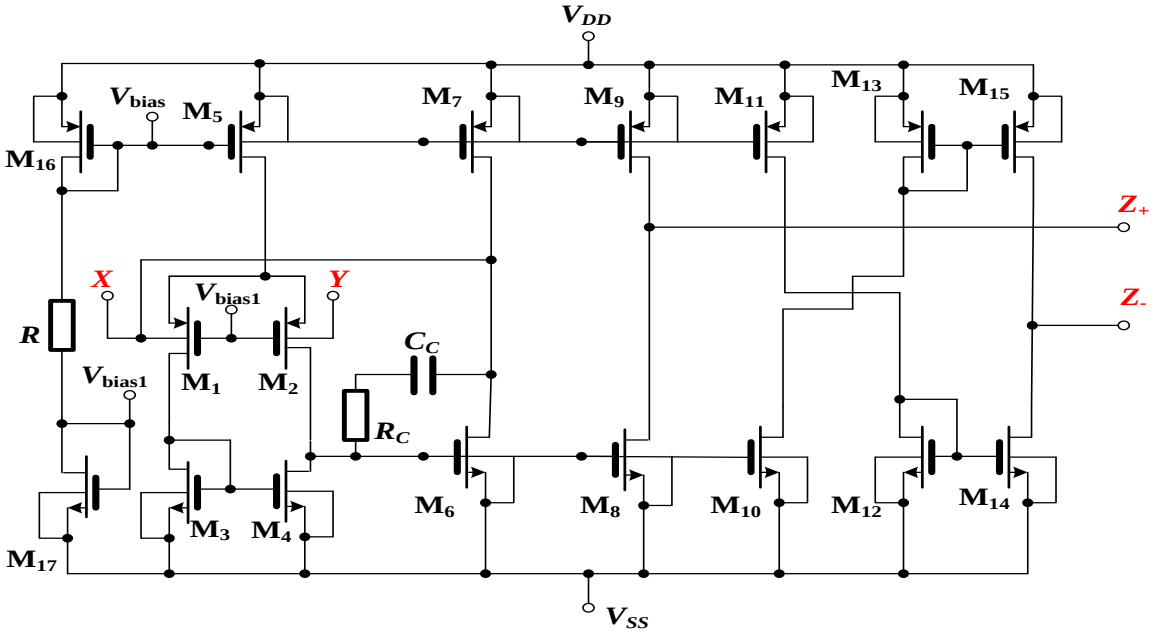


Fig. 3-2: Bulk-driven CCII± based on Bulk-driven OTA.

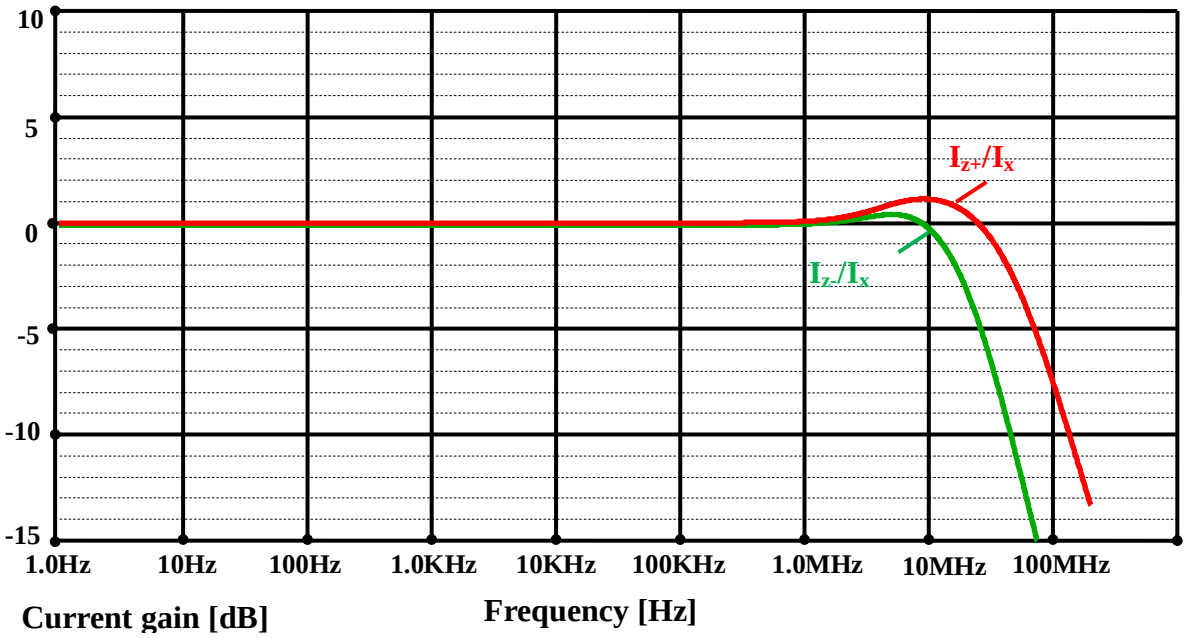


Fig. 3-3: Frequency variation of the current gains I_{Z+}/I_X, I_{Z-}/I_X in dB of the CCII in Fig. 3-2.

Simulation results of the CCII± are summarized in Table 3-1.

Characteristics	Simulation Result
Power consumption	119 μW
3-dB bandwidth I_{Z+}/I_X	20 MHz
3-dB bandwidth I_{Z-}/I_X	52 MHz
DC voltage range	-400, 600 mV
DC current range	±16 μA
Current gain I_Z/I_X	1
Voltage gain V_X/V_Y	0.97
Node X parasitic DC resistance	166 Ω
Node Y parasitic DC resistance	50 GΩ
Node Z+ parasitic DC resistance	560 kΩ
Node Z- parasitic DC resistance	554 kΩ
Measurement condition: V_{DD} = 0.6V, V_{SS} = - 0.6V	

Tab. 3-1: Simulation results of the Bulk-driven CCII.

3.1.2. Bulk-driven OTA with gm adjustable via external R

In this part, a new concept of high-linearity OTA with controllable transconductance is proposed. The OTA is simulated in a standard TSMC 0.18 mm CMOS process with a 0.6 V supply voltage.

The principle of g_m adjustable via a feedback resistor R_{adj} is show in Fig. 3-4.

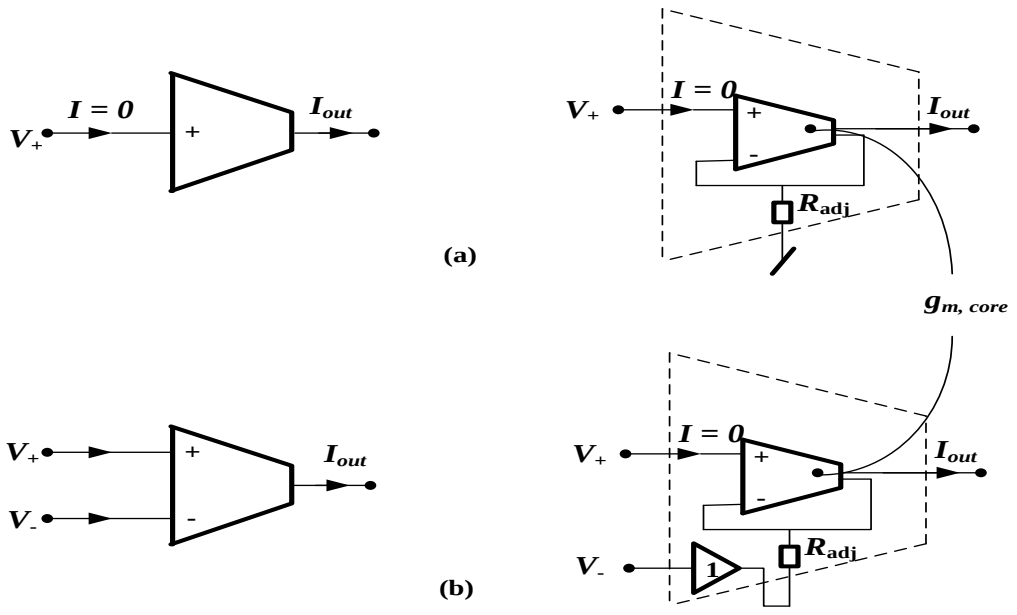


Fig. 3-4: (a) SISO OTA with gm adjustable, (b) DISO OTA with gm adjustable.

In this part, a high linearity, wideband OTA with tunable transconductance is presented according to Eq. (3-2). The adjustable transconductance $g_{m,\,adjust}$ depends on R_{adj} as follows:

$$g_{m,}adjust = \frac{g_{m,core}}{1 + g_{m,core}\ R_{adj}} \tag{3-2}$$

Figs. 3-5, and 3-6 show circuit implementations of Fig. 3.4, namely bulk-driven single input single output OTA (SISO) and a fully differential OTA (DIDO) based on voltage buffer and Current Conveyor of Second Generation CCII.

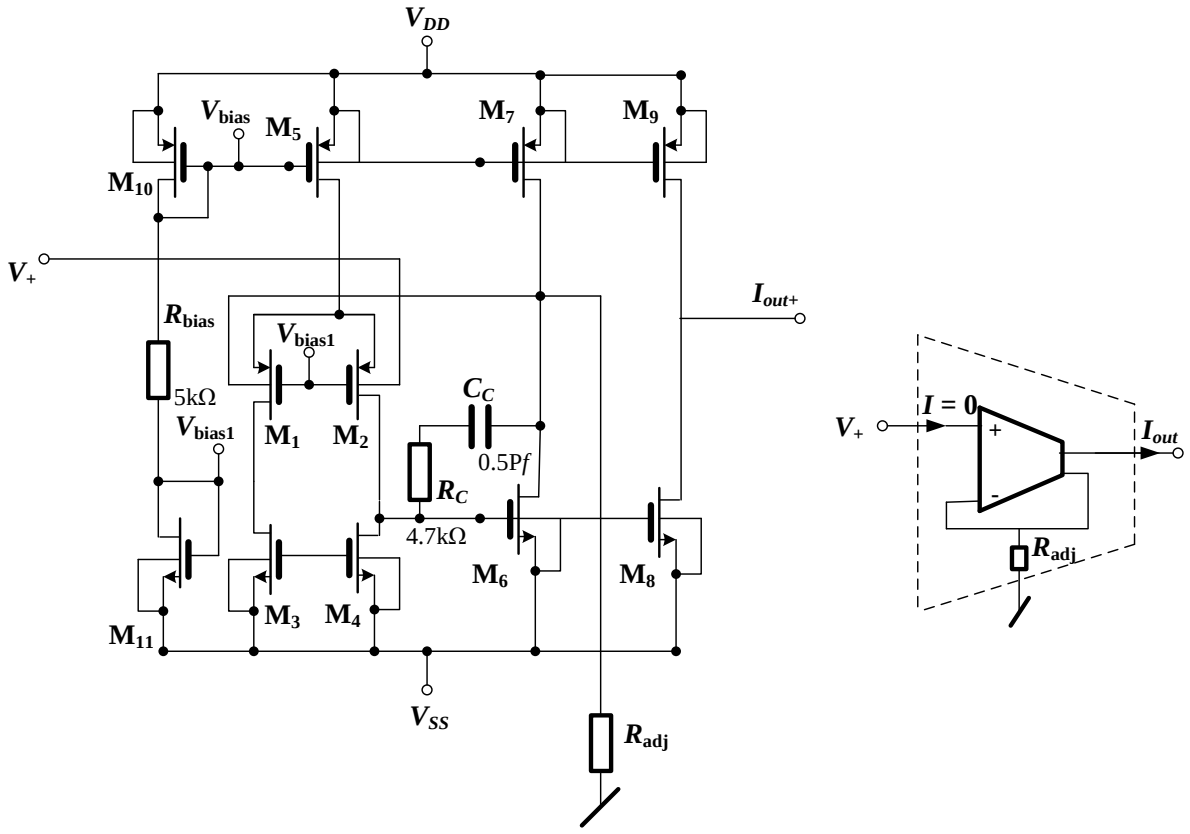


Fig. 3-5: Bulk-driven single input single output OTA (SISO) based on CCII.

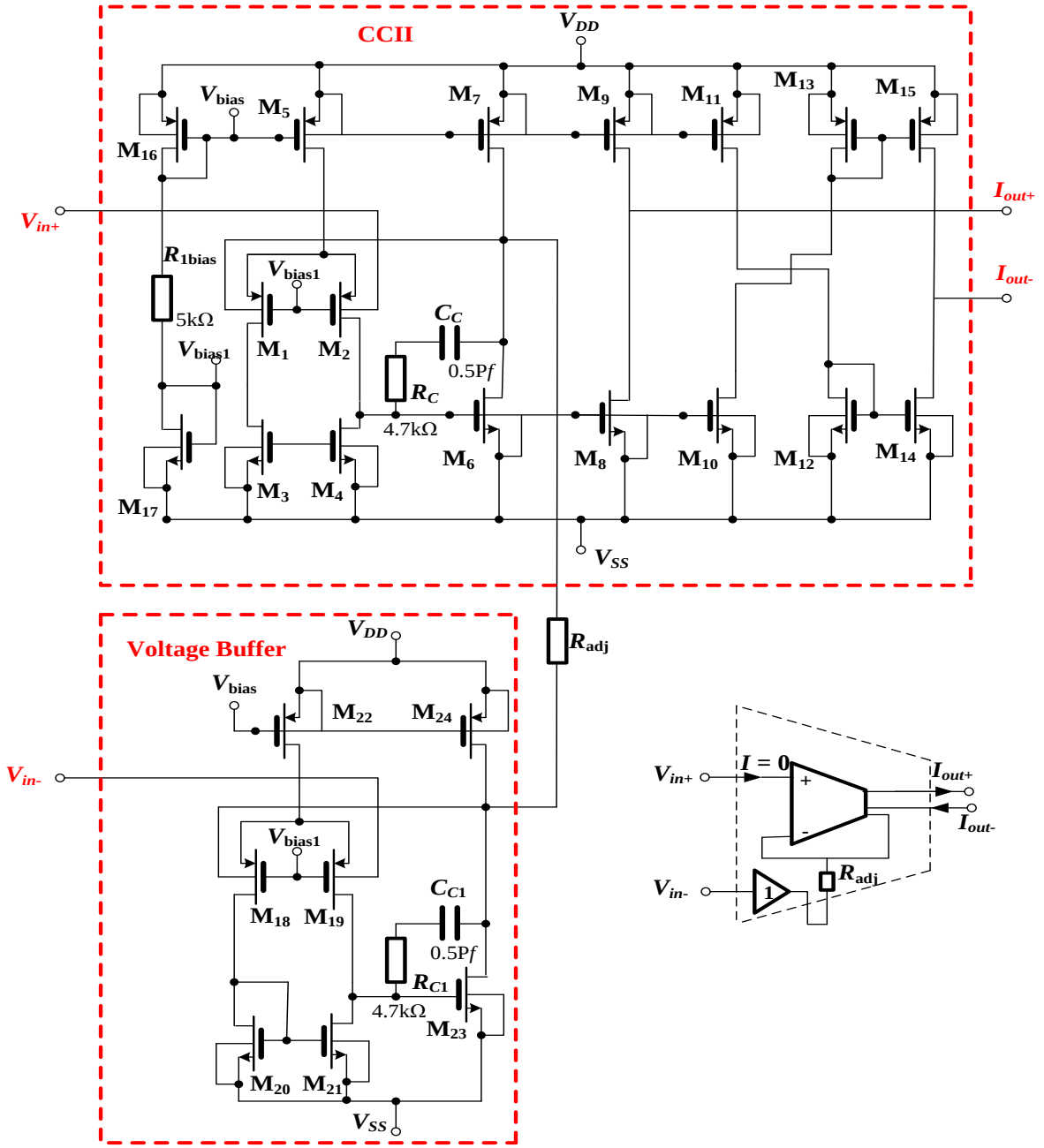


Fig. 3-6: Bulk-driven fully differential OTA (DIDO) based on CCII and voltage buffer.

The performance of the proposed OTA in Fig. 3-5 was verified via PSPICE simulation. All the balanced CMOS OTA was simulated by using CMOS structure and MIETEC 0.18µm.

Fig. 3-7 shows the simulated transfer characteristics of the OTA in Fig. 3-5. The plots of the output current I_{out} versus the input voltage V_{in} show that, for R_{adj} values of 1Ω, 10Ω, 100Ω, 1kΩ. 2kΩ, 5kΩ, 10kΩ, 20kΩ, 50kΩ, 100kΩ, 200kΩ, 500kΩ, and 1MΩ, the g_m is controlled accordingly.

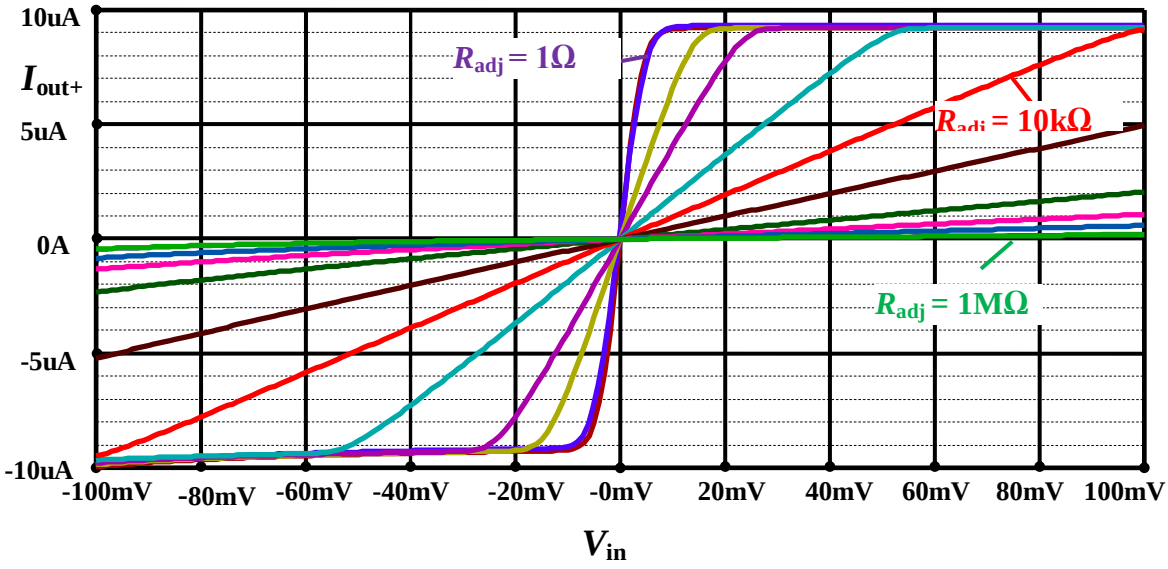


Fig. 3-7: DC transfer characteristics of bulk-driven fully differential OTA.

It is shown that the transconductance gain g_m can be linearly tuned when R_{adj} is increased. But for R_{adj} bigger than 50kΩ it causes distortion. The linear range is very good for R_{adj} of about 10kΩ.

The AC analysis of the bulk-driven OTA in Fig. 3.5 is shown in Fig. 3-8. The frequency dependence of I_{out} is measured by fixing AC value of V_{in} at 1V.

The responses are plotted for R_{adj} of 1Ω, 10Ω, 100Ω, 1kΩ, 2kΩ, 5kΩ, 10kΩ, 20kΩ, 50kΩ, 100kΩ, 200kΩ, 500kΩ, and 1MΩ. The corresponding values of g_m are shown in Table. 3-2

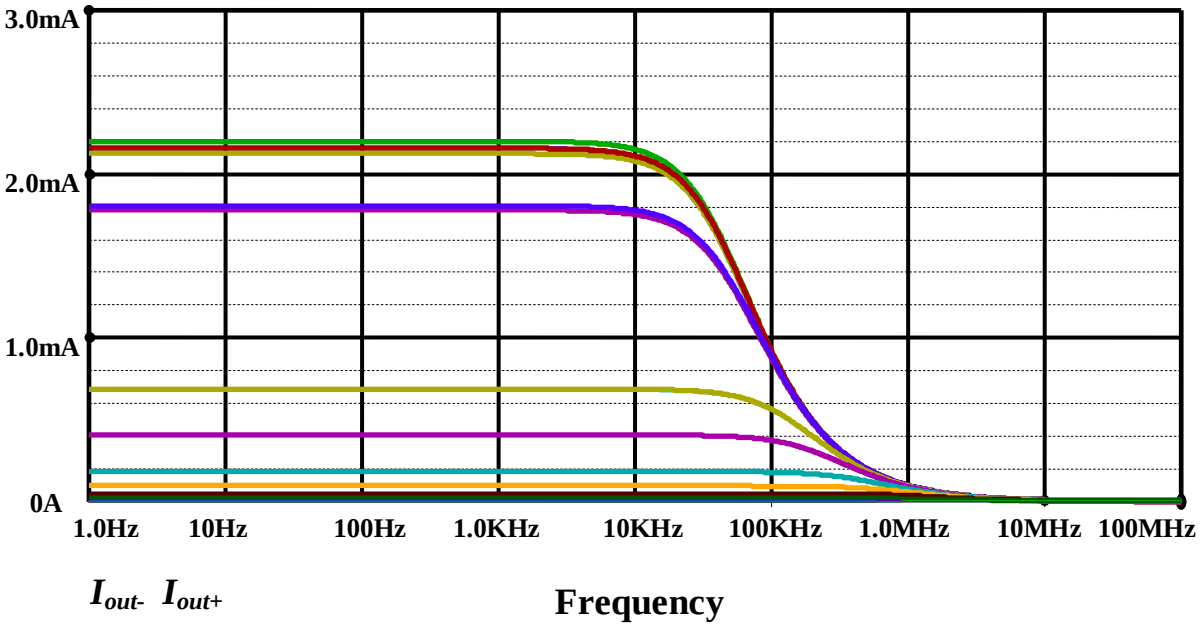


Fig. 3-8: AC transfer characteristics of bulk-driven fully differential OTA.

R_{adj}	g_m
1Ω	2.2 ms
10Ω	2.16 ms
100Ω	1.8 ms
1kΩ	688.7 µs
2kΩ	408.5 µs
50 kΩ	184.45 µs
100 kΩ	96.82 µs
200 kΩ	50.1 µs
500 kΩ	21.04 µs
1 MΩ	11.2 µs

Tab: 3-2: Variations of g_m by R_{adj}.

3.2. Voltage Differencing Transconductance Amplifier (VDTA)

The methodology described in the CDTA, which uses the CDU as the input unit, and the following simple block OTA represents an open system: Let us continue with the variation that the input unit will now implement voltage and not current differences. The differential-input OTA is a simple element for realizing the voltage difference. Simultaneously, it can provide the possibility of electronic control. The VDTA element [23] with its schematic symbol in Fig. 3-9 (a) has a pair of high-impedance current inputs p and n, and an auxiliary terminal z. A multiple copies of I_z current are indicated here in order to increase the universality of VDTA element. Thus, according to the proposed methodology, the VDTA element should have the "zc"(Z Copy) attribute. Also a possible implementation of VDTA using two OTA components is given in Fig. 3-9 (b). Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the *z* terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

$$I_P = I_n = 0, \qquad I_Z = \mathrm{g}_{mz}\left(V_p - V_n\right) \tag{3-3}$$

$$I_{zc} = \pm I_z \tag{3-4}$$

$$I_{x+} = \mathrm{g}_{mx} V_Z, \qquad I_{x-} = -\mathrm{g}_{mx} V_Z \tag{3-5}$$

VDTA has an interesting application potential: for example, the floating loss-less inductor can be simulated only by one VDTA and one grounded capacitor.

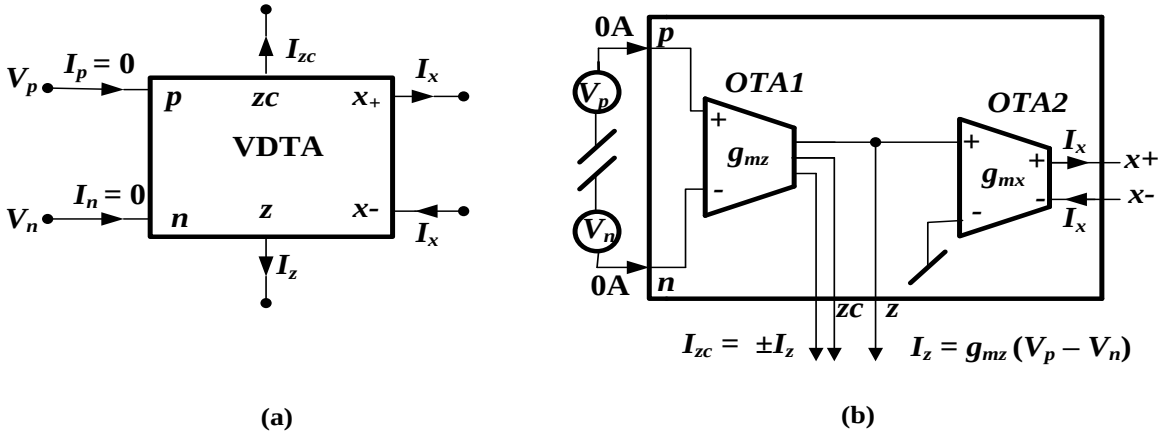


Fig. 3-9: (a) Symbol of the VDTA, (b) its implementation by OTAs.

3.2.1. Operations using the ideal VDTA

- **Integrator using VDTA**

The operation of integration can be achieved very conveniently using the VDTA as is shown in Fig. 3-10. Clearly,

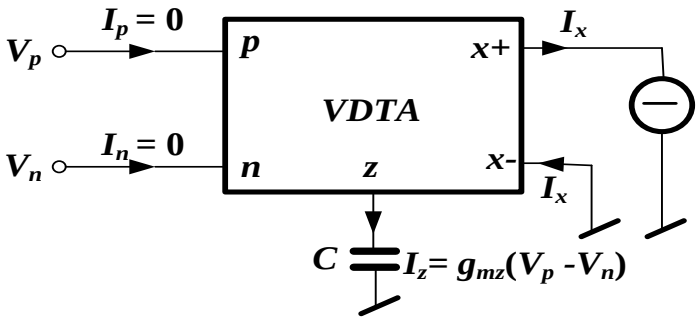


Fig. 3-10: Integrator using VDTA.

$$I_z = g_{mz}\left(V_p - V_n\right) \tag{3-6}$$

$$V_z = \frac{I_z}{sC} = \frac{g_{mz}\left(V_p - V_n\right)}{sC}$$

$$I_x = g_{mx} V_z = \frac{g_{mx}\, g_{mz}\left(V_p - V_n\right)}{sC}$$

$$\frac{I_x}{\left(V_p - V_n\right)} = \frac{g_{mx}\, g_{mz}}{sC} \tag{3-7}$$

- **Current Summation using VDTA**

Current summation can be obtained using VDTA as shown in Fig. 3-11.

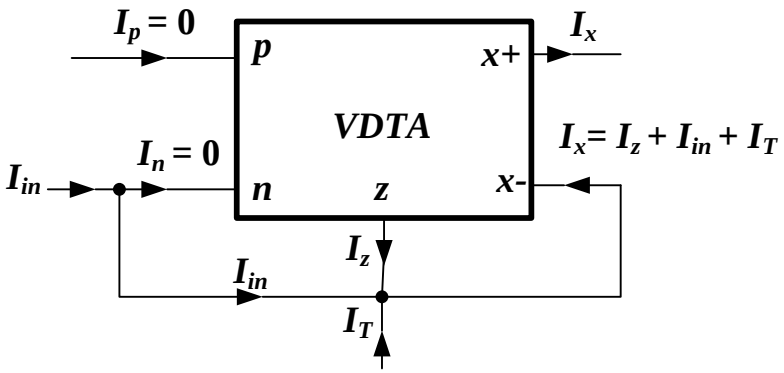


Fig. 3-11: Current summation using VDTA.

3.2.2. CMOS Implementation of VDTA

For low-voltage low-power applications, is can be advantageous to implement the VDTA element in Fig. 3-9 (b) with the utilization of bulk-driven [67] CMOS technique. One possibility is presented in Fig. 3-12.

VDTA is built here by means of two OTAs of DISO (Differential Input Single Output) and SIDO (Single Input Differential Output) types. This circuit uses low supply voltages, namely ± 0.6 V. The total power dissipation is less than 206μW.

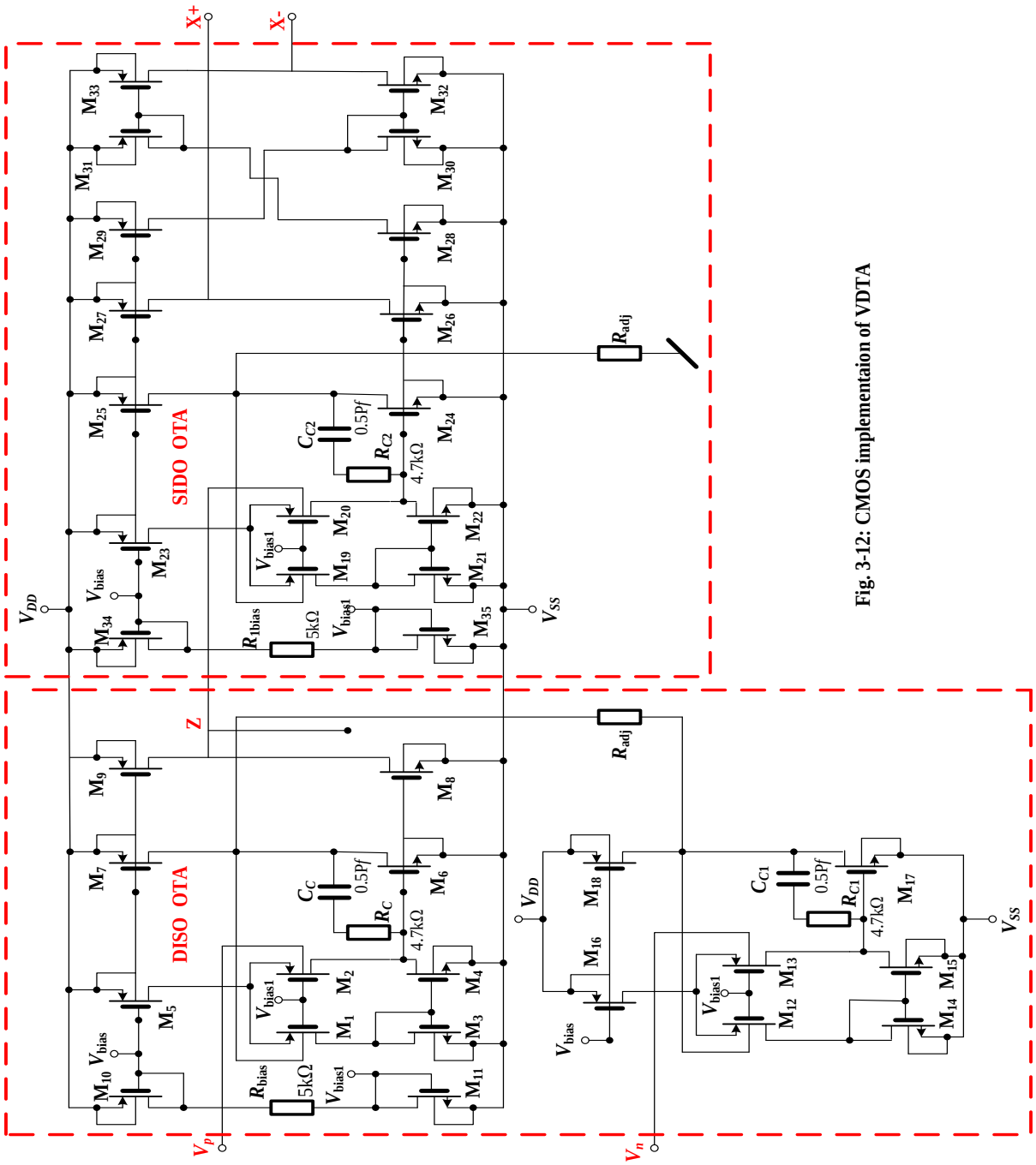


Fig. 3-12: CMOS implementaion of VDTA

4. LC ladder simulation and other applications of active elements

4.1. Optimization of ladder filters with GmC simulation of floating inductors

Replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design. An efficient way of simulating the floating inductor consists in replacing the inductor by three OTAs (Operational Transconductance Amplifier) and one grounded capacitor [43]. However, the common drawback of OTAs is the low-level input voltage providing the linear mode of the amplifier.

This can be in conflict with the requirements for a large dynamic range of signals being processed. When the filter is designed for the current-mode, the current limitations of the active elements should also be carefully monitored.

MAX435 is a commercial OTA [46], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well known circuitry for simulating the floating inductor [43]. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.

Using the concrete example of 5th-order video filter, a method for designing and optimizing such a circuit is described in this paper. The commercial MAX435 is used in the subcircuits of synthetic inductances. The procedure described can be applied to an arbitrary type of OTA.

4.1.1. MAX435 – a commercial OTA

MAX435 is an OTA with 275MHz bandwidth and 850V/us slew rate. Its recommended symmetrical power supply is +-5V. The transconductance g_m is set within a wide range by means of auxiliary R_t resistor [46]. The recommended maximum current through R_t as well as the output current are 10mA. A concrete saturation level I_{max} can be adjusted by R_{set} resistance approximately from 3mA up. R_{set} = 5.9kΩ corresponds to a current of 10mA. The maximum recommended differential voltage is 2.5V.

4.1.2. Synthetic inductor based on MAX435

Fig. 4-1 shows a synthetic floating inductor which employs a pair of differential-input differential-output OTAs. It is a generalization of the circuit from [43], where three single-output OTAs are used for inductor replacement. The signal flow graphs attached describe the process of transforming voltage V_1 into current I_1 of OTA No. 1, transforming current I_1 into voltage across the capacitor, and transforming capacitor voltage into current I_2.

It follows from the last graph that the circuit implements a lossless floating inductor with the inductance

$$L = \frac{C_L}{g_{m1} g_{m2}} \tag{4-1}$$

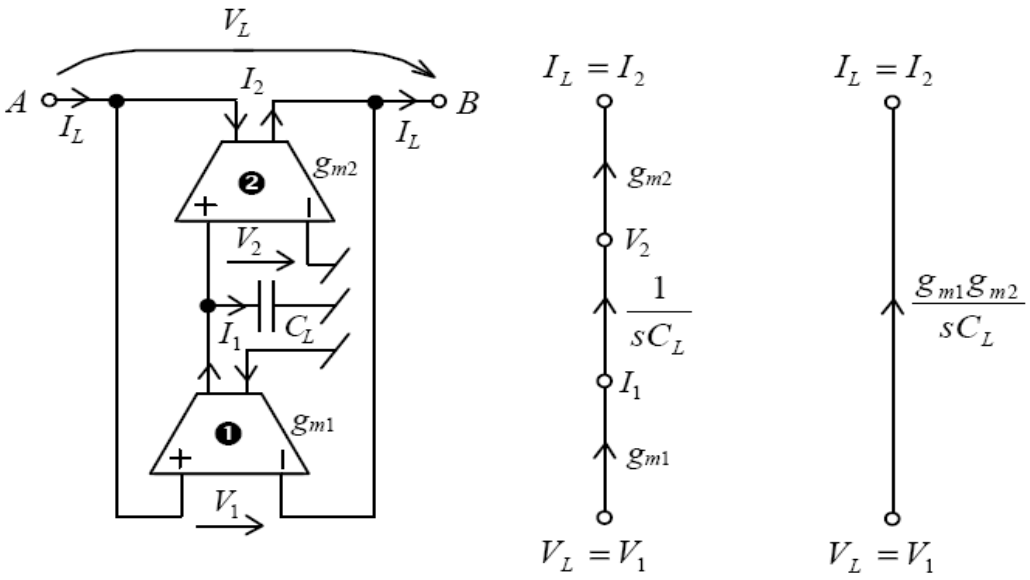


Fig. 4-1: Synthetic inductor and the corresponding signal flow graphs.

There are two degrees of freedom when designing the transconductance g_{m1} and g_{m2} and the capacitance C_L from the desired inductance value. They can be used for dynamic range optimization. The following rule results from 4-1:

The inductor is preliminarily designed with the parameters g_{m1}, g_{m2}, and C_L. These parameters will be modified according to the rule

$$C_L^{/} = a_0 C_L, \qquad \mathrm{g}_{m1}^{/} = a_1 \mathrm{g}_{m1}, \qquad \mathrm{g}_{m2}^{/} = a_2 \mathrm{g}_{m2} \tag{4-2}$$

Where a_0, a_1, and a_2 are real positive numbers, fulfilling the equality

$$a_0 = a_1 a_2 \tag{4-3}$$

Then the resulting inductance is not changed due to this modification. However, current I_1 will be a_1 times greater and voltage V_2 will be a_1/a_0 times greater than before the modification of the parameters.

This rule will be used for the dynamic range optimization of target application, i.e. the active filter which simulates the LC ladder.

The following equality also results from the graph in Fig. 4-1:

$$\frac{V_2}{V_1} = \frac{\mathrm{g}_{m1} I_2}{\mathrm{g}_{m2} I_1} \tag{4-4}$$

The purpose of optimizing the upper limit of the dynamic range is to equalize the voltage and current levels inside the synthetic inductors, thus $V_1 = V_2$ and $I_1 = I_2$. Eq. 5-1 shows that a complete equalization is enabled only when both transconductances are equal.

4.1.3. LC Ladder simulation

Fig. 4-2 shows the schematic of a lowpass LC ladder filter which has been designed according to Bessel approximation on the basis of the following specifications:

DC gain 0dB, 3-dB cutoff frequency 5MHz, attenuation at least 50dB for frequencies above 27MHz, maximally flat group delay. This specification is derived from the parameters of commercial video filter FMS6400-1 by Fairchild Semiconductor [47].

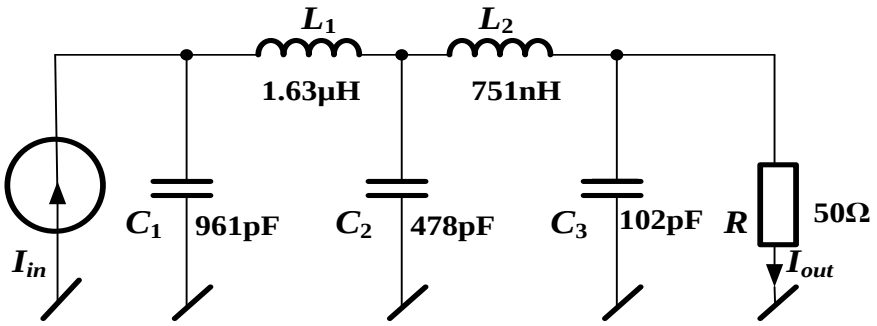


Fig. 4-2: 5MHz lowpass ladder filter.

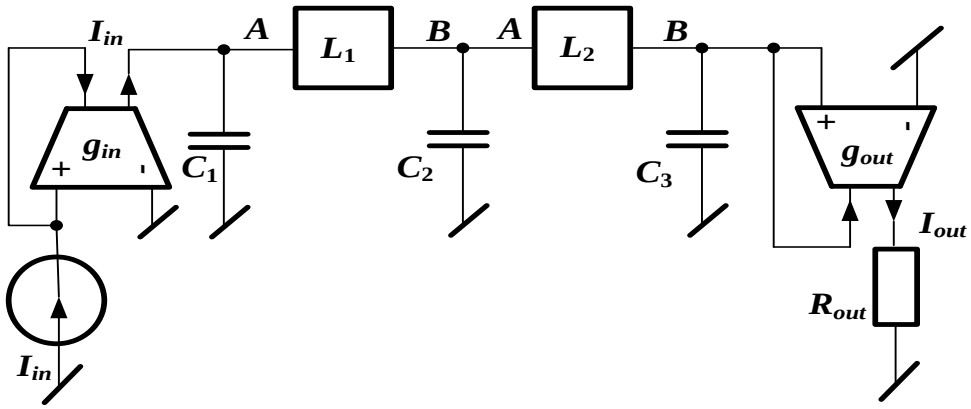


Fig. 4-3: Active ladder simulation by means of synthetic inductors and OTAs.

An active realization of the LC ladder is shown in Fig. 4-3. Blocks "L_1" and "L_2" are the synthetic inductors from Fig. 4-1. OTA with transconductance g_{in} serves as a current-controlled current source, providing low driving point impedance $R_{in} = 1/g_{in}$ for the input current source. OTA with transconductance $g_{out} = 1/R$ =20mS delivers current I_{out} into an independent load R_{out}. Let us design the active filter from Fig. 4-3 for a maximum driving current value of 10mA. The results of PSpice AC analysis of the passive LC ladder from Fig. 4-2 are shown in Fig. 4-4. The analysis was performed on the assumption of the attribute AC=10mA of the current source I_{in}. Those curves are depicted which are important for studying the filter dynamic range, i.e. the output voltage across R (i.e. the input voltage of the

terminating OTA), the output current through R (i.e. the output current of the terminating OTA), the voltages across L_1 and L_2 (i.e. the input voltages of OTA No. 1 in the synthetic inductors from Fig. 4-1), and the currents through L_1 and L_2 (i.e. the output currents of OTA No. 2 in the synthetic inductors from Fig. 4-1). The curves are determined by the parameters of filter elements and they can be influenced only via choosing another realization structure, another approximation of frequency response or another impedance level. The Bessel approximation used here guarantees a maximally flat group delay response.

Fig. 4-4 shows that both the synthetic inductors and the terminating OTAs should be designed for a maximum current of 10mA. It is fulfilled for MAX435 when adjusting R_{set} = 5.9kΩ. The input voltage of the end OTA is maximum (1V) for low frequencies. The required g_m value of this OTA is 1/R = 20mA/V and it can be set via R_t = 200Ω [46]. This amplifier will operate in the linear regime till its full current excitation.

The front-end OTA, excited by the current source I_{in}, will be designed with g_{in} = 100mA/V or R_t = 40Ω in order to provide low driving point impedance $R_{in} = 1/g_{in}$ = 10Ω. The maximum value of the input voltage will be 100mV for full current excitation of the filter input.

The curves $V(L_1)$, $V(L_2)$, $I(L_1)$, and $I(L_2)$ can be used for designing the synthetic inductors. The voltage across L_1 (L_2) takes its maximum value 408mV (173mV) at a frequency of 6.31MHz (5.75MHz). As stated before, the currents are maximum, i.e. 10mA at a frequency of 0 Hz.

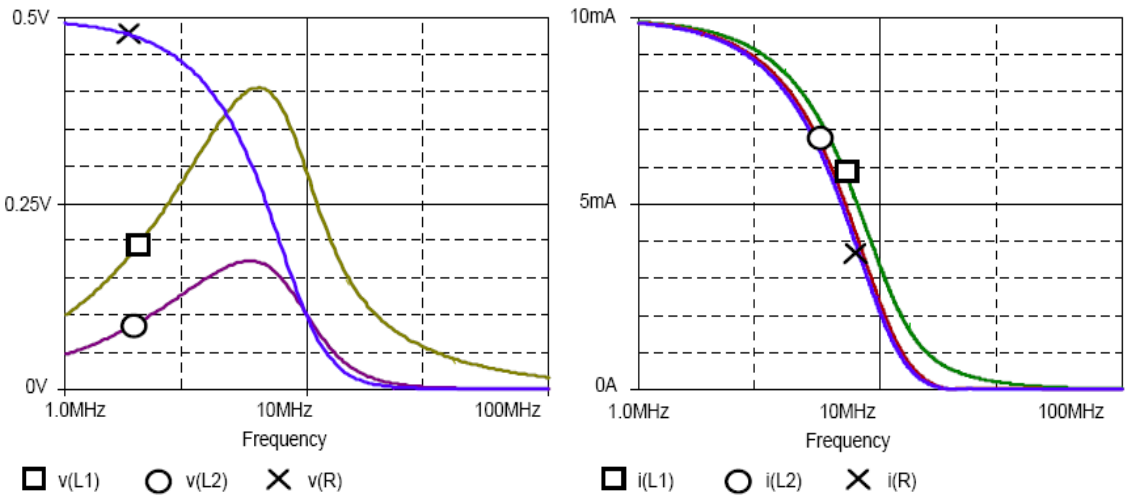


Fig. 4-4: Results of the AC analysis of LC ladder from Fig. 4-2 (a) for Iin = 10mA.

In the first step, a preliminary design of the synthetic inductors according to Eq. 4-1 will be performed. The initial capacitance in both inductors will be set to 100pF. For equal values of g_{m1} and g_{m2}, Eq. 4-1 leads to the results in Table 4-1.column (1).

		(1) Before optimization	(2) After optimization
L_1	g_{m1} [mA/V]	7.833	24.505
	g_{m2} [mA/V]	7.833	24.505
	R_{t1} [Ω]	511	163
	R_{t2} [Ω]	511	163
	C_L [pF]	100	979
L_2	g_{m1}[mA/V]	11.539	57.902
	g_{m2} [mA/V]	11.539	57.902
	R_{t1} [Ω]	347	69
	R_{t2} [Ω]	347	69
	C_L [pF]	100	2518

Tab. 4-1: Parameters of elements of the synthetic inductors before and after optimization.

The Signal-Flow-Graph from Fig. 4-1 describes relations among the internal variables of the synthetic inductor, particularly between the inductor terminal voltage, the output current of OTA No. 1, the input voltage of OTA No. 2, and the inductor terminal current. These relations can be pre-set in the Probe postprocessor of PSpice simulator [48]. The results are shown in Fig. 4-5(a). The left-side part contains the curves of OTA input voltages; the right-side shows the curves of OTA output currents.

The maximum values of voltages and currents from Fig. 4-5 are given in Table 4-2, column (1). Note that the input voltages of OTA No. 2 are too high whereas the output currents of OTA No. 1 do not reach their permitted maxima for either inductor. In addition, the following equality is true:

$$\frac{V_2}{V_1} = \frac{\mathrm{g}_{m1} I_2}{\mathrm{g}_{m2} I_1} \tag{4-5}$$

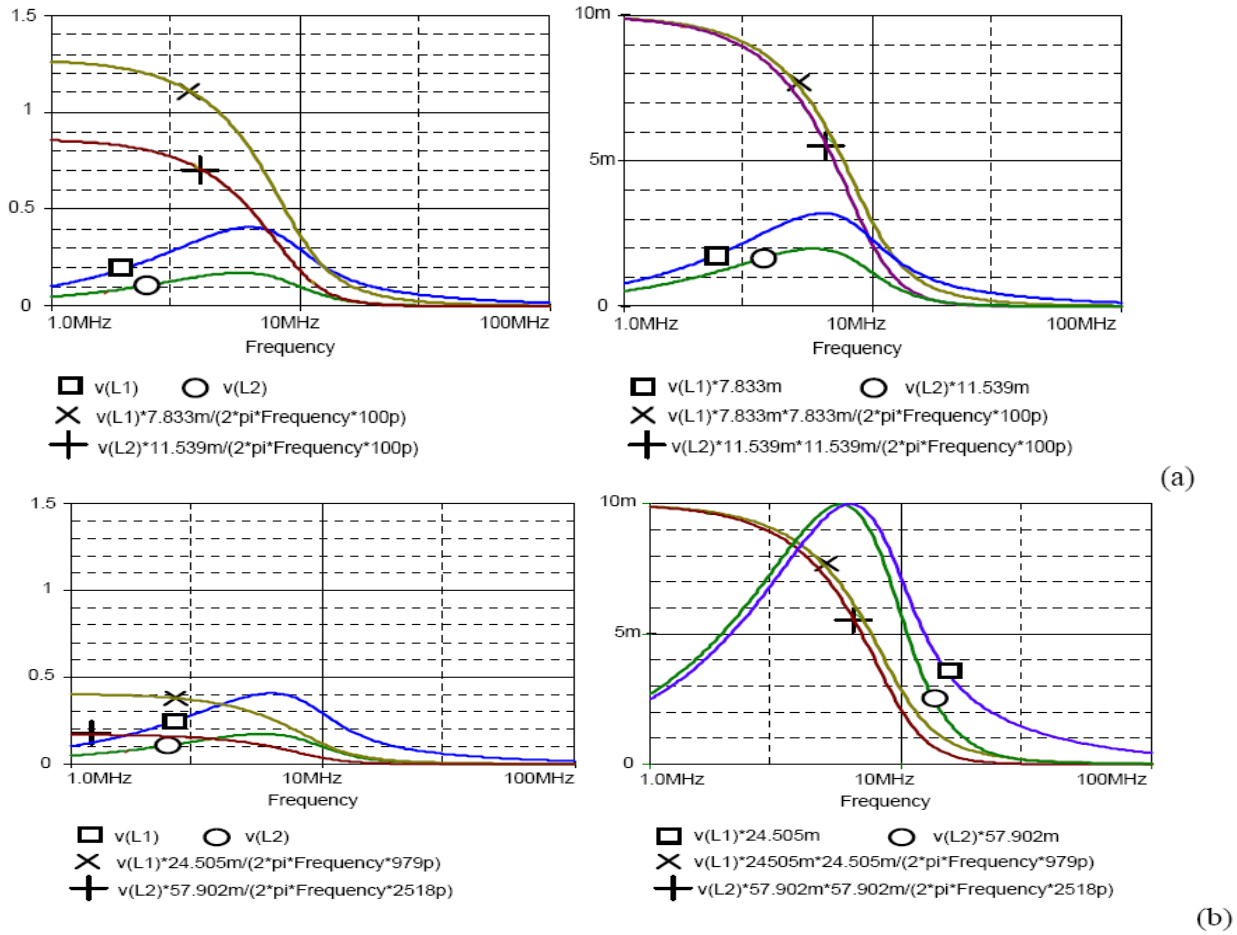


Fig. 4-5: PSpice analysis of synthetic inductors by means of dependences described by Signal- Flow-Graphs from Fig. 4-1, (a) before, (b) after optimizing the dynamic range.

		(1) Before optimization	(2) After optimization
L_1	V_{1max} [V]	0.4082	0.4082
	V_{2max} [V]	1.277	0.4082
	I_{1max} [mA]	3.197	10.003
	I_{2max} [mA]	10	10
L_2	V_{1max} [V]	0.1727	0.1727
	V_{2max} [V]	0.8666	0.1727
	I_{1max} [mA]	1.992	9.998
	I_{2max} [mA]	10	10

Tab. 4-2: Maximum values of inductor voltages and currents before and after optimization.

It is in conformity with Eq. (4-2). These ratios are 3.128 for inductor No. 1 and 5.018 for inductor No. 2.

Applying the rule from Section 4.1.2 and the corresponding equations (4-2) and (4-3), we conclude that the upper limits of the dynamic ranges of voltages and currents in the inductors can be equalized if both transconductance are multiplied by ratio 4/5 and the capacitance is simultaneously multiplied by the square of this ratio. After this optimization, the parameters of the elements are as shown in Table 4-1, column (2). The corresponding frequency responses are given in Fig. 4-5 (b) and the maximum values of voltages and currents can be found in column (2) of Table 4-2.

Frequency responses of the optimized active filter, simulated in PSpice simultaneously with the frequency responses of ideal LC ladder, are shown in Fig. 4-6. Note that the group delay is more sensitive to real properties of the amplifiers than the gain response. The analysis found that low output impedance of MAX435, namely 3.5kΩ, is a dominant factor which imports losses to the ladder structure. Nevertheless, the group delay ripple is less than is specified for similar commercial video filter FMS6400-1 [47].

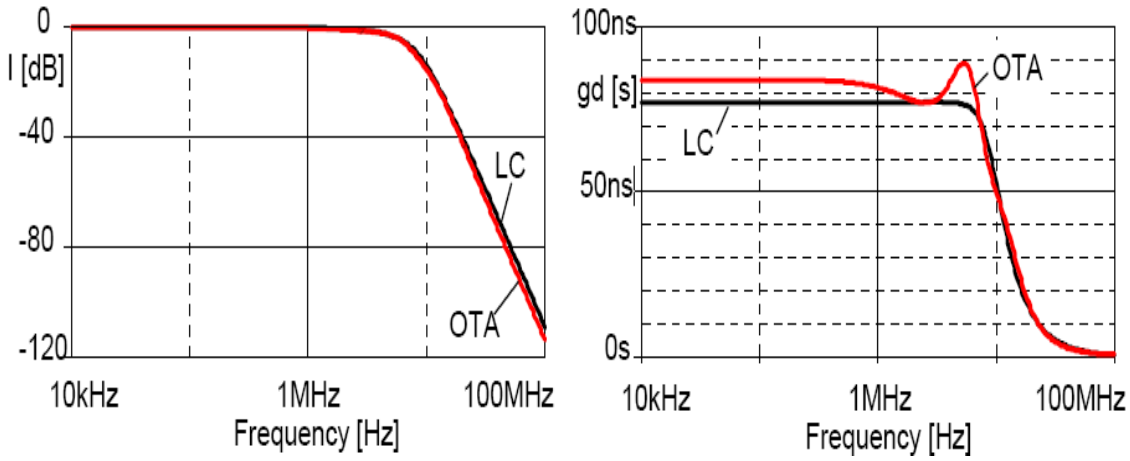


Fig. 4-6: Frequency responses of ideal LC ladder (LC) and optimized active filter.

4.2. Voltage Differencing Transconductance Amplifier for Filter Implementation

Presently, there is the interest of the availability of building active filters and other signal processing circuits without the use of physical coils. Although, a spiral inductor can be realized in an integrated circuit, it still has some drawbacks in the usage of space, weight, cost and tunability.

The inductance simulators can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element. The attention is subsequently focused on the inductance simulation using different high-performance active building blocks such as, Operational Transconductance Amplifiers (OTAs) [47], current

feedback op-amps [27], and four-terminal floating nullors (FTFNs) [49], current conveyors [50-53], current differencing buffered amplifier (CDBAs) [54], etc. The literature surveys shows that a large number of circuit realizations for floating and grounded inductance simulators have been reported [47], [54].

In this section, we present novel floating simulators employing Differencing Transconductance Amplifier (VDTA), which is proven to be quite useful in either current or voltage-mode signal processing circuits.

4.2.1. Synthetic inductor based on VDTA

Fig. 4-7 shows a synthetic floating inductor which employ one of Voltage Differencing Transconductance Amplifier (VDTA) which contains Differential Input Single Output OTA (DISO) and Single Input Differential Output OTA (SIDO), and one grounded capacitor C_L**.**

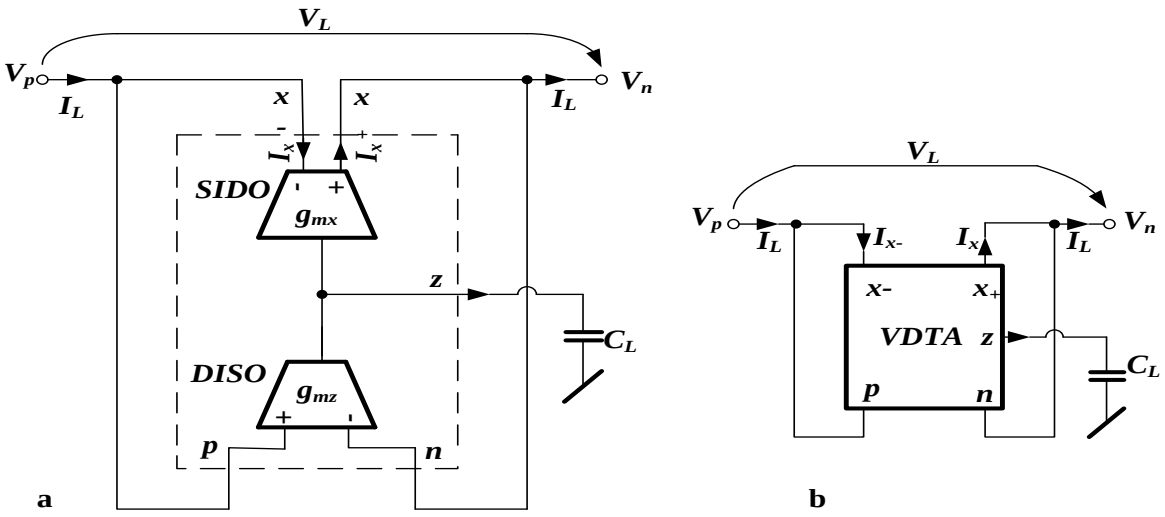


Fig. 4-7: (a) Synthetic inductor circuit employing DISO OTA and SIDO OTA, (b) simplified representation of the synthetic inductor by VDTA.

The process of transforming voltage difference ($V_P - V_n$) into current I_z of DISO OTA is described by the equation:

$$I_Z = \mathrm{g}_{mz}\left(V_p - V_n\right) \tag{4-6}$$

Current I_z causes voltage across the capacitor, and this voltage is transformed into current I_x.

$$V_C = \frac{I_Z}{sC_L} = \frac{\mathrm{g}_{mz}\left(V_p - V_n\right)}{sC_L} \tag{4-7}$$

$$I_X = g_{mx} V_C \tag{4-8}$$

$$I_X = g_{mx} g_{mz} \frac{(V_p - V_n)}{sC_L} \tag{4-9}$$

$$Z_{in} = \frac{I_X}{(V_p - V_n)} = \frac{g_{mx} g_{mz}}{sC_L} \tag{4-10}$$

The circuit, thus, simulates a floating inductor with the resulting inductance given by

$$L = \frac{g_{mx} g_{mz}}{C_L} \tag{4-11}$$

4.2.2. Low-pass LC Ladder simulation

Fig. 4-8 shows the schematic of a lowpass LC ladder filter which has been designed according to Cauer approximation on the basis of the following specifications:
DC gain 0dB, 3-dB cutoff frequency 25kHz, ripple 2dB, 40dB for frequency above 55kHz, third-order.

The active simulation of the passive LC ladder filter from Fig. 4-8 by means of Voltage Differencing Transconductance Amplifier (VDTA) is given in Fig. 4-9.

The proposed floating inductor circuit in Fig. 4-7 is realized with the following values: g_{mz} $=g_{mx}$ = 96.8 µS with R_{adj} equal to 10kΩ according to Table 3-2.

From equation (4-11)

$$C_L = L\, g_{mz}\, g_{mx} = 441\text{pF}$$

The VDTA is simulated by using the schematic implementation shown in Fig. 3-12 with DC power supply voltages equal to V_{DD} = V_{SS} =±0.6 V. The simulations are performed by using CMOS structure and MIETEC 0.18µm CMOS process model technology parameters.

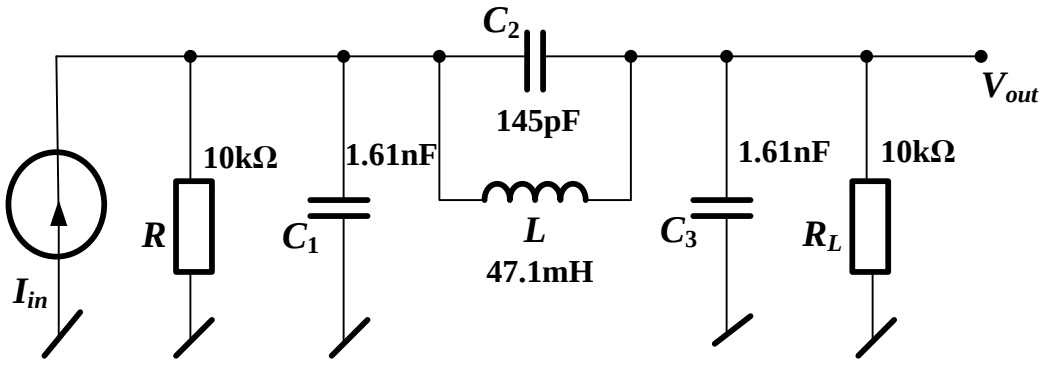


Fig. 4-8: 25kHz LC ladder filter.

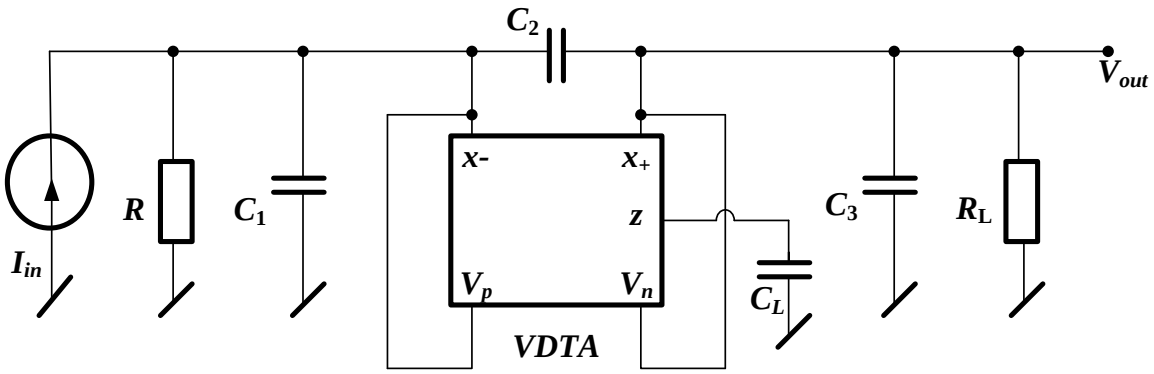


Fig. 4-9: Active implementation of the filter from Fig. 4-8.

The frequency responses and the group delay of the filter are shown in Figs. 4-10, and 4-11, respectively. It can be seen that the simulation using the true inductor and its VDTA simulators are in good agreement.

Fig. 4-12 shows that the magnitudes of the impedances of an ideal inductor with value equal to 47.1mH which we used in LC ladder filter in Fig. 4-8, and its simulator circuit by Voltage Differencing Transconductance Amplifier (VDTA) as shown in Fig. 4-9 with C_L equal to 441pF can be made very close for a set of selected values over many decades.

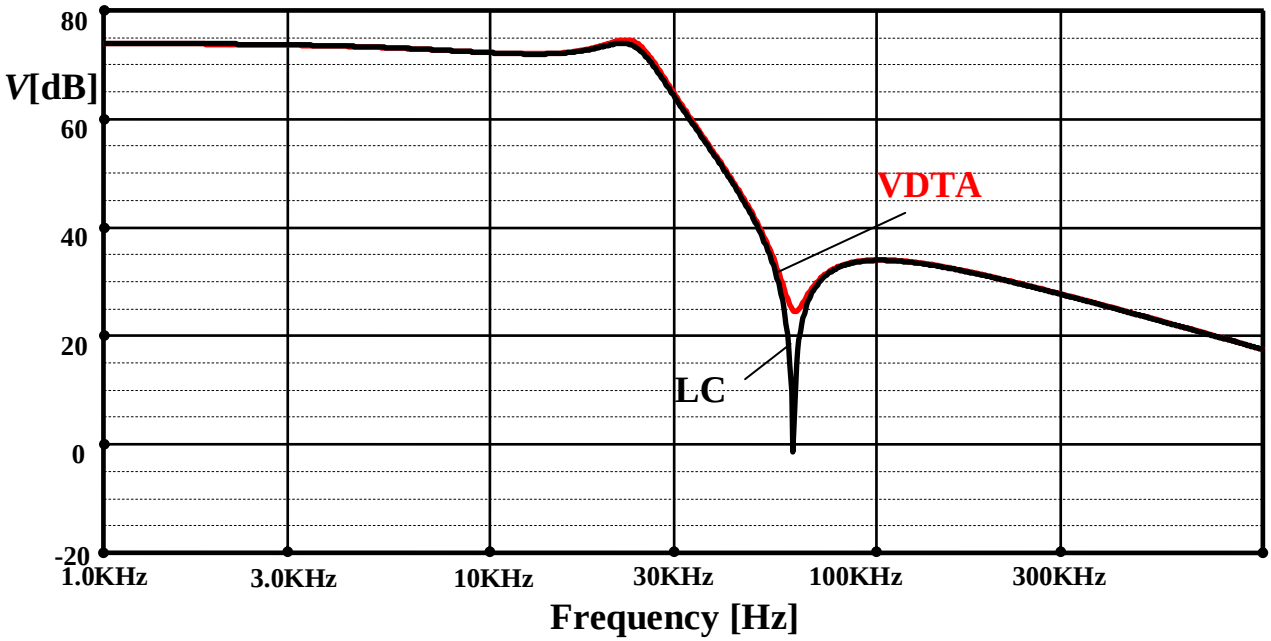


Fig. 4-10: The frequency responses of ideal LC ladder and VDTA-based active filter.

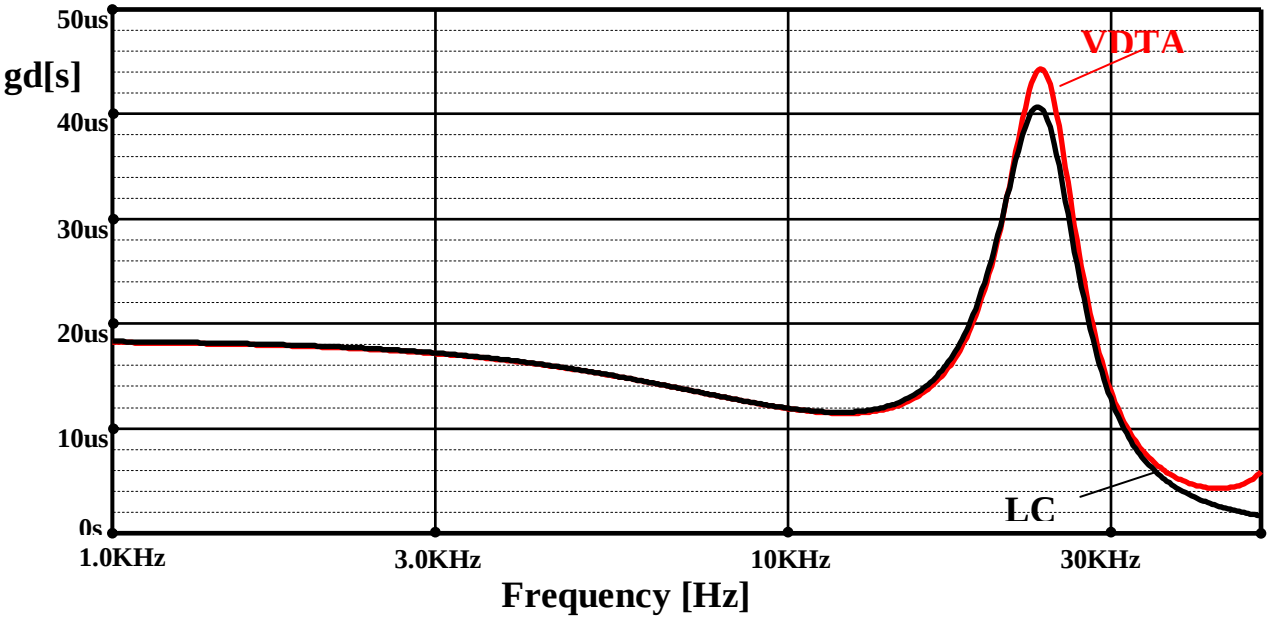


Fig. 4-11: The group delay response of ideal LC ladder and VDTA-based active filter.

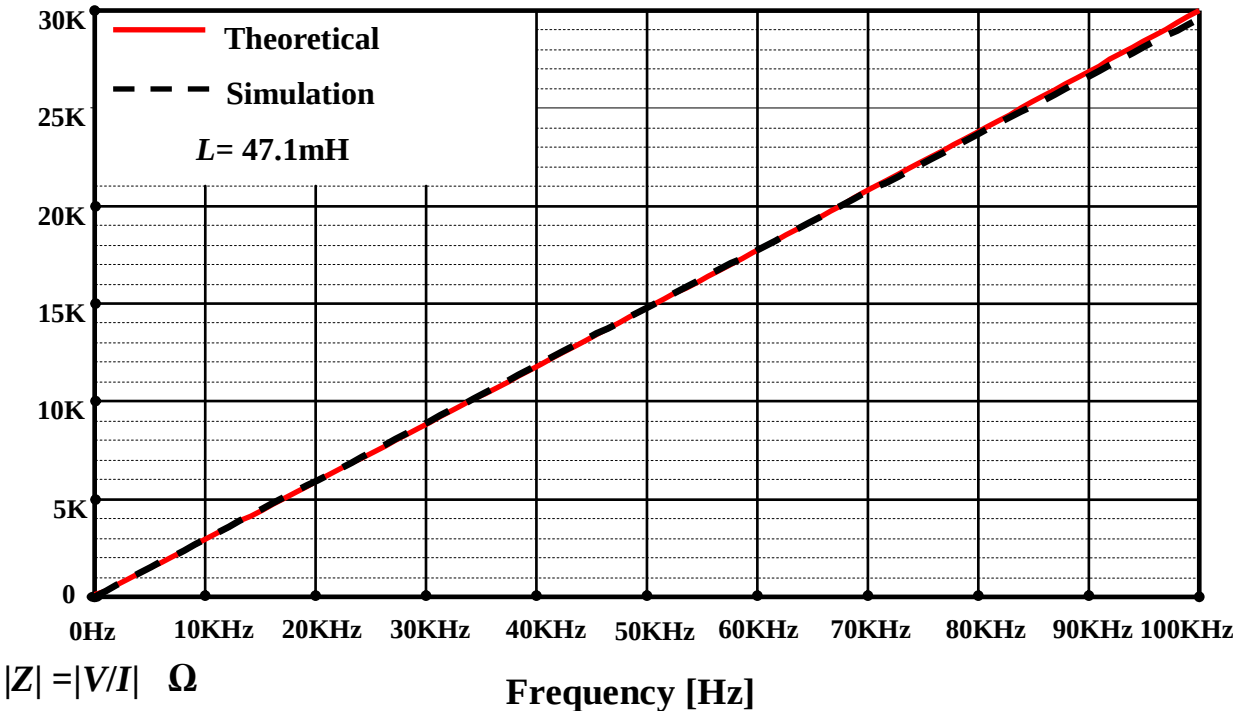


Fig. 4-12: The impedance values relative to frequency of the ideal and simulated inductors.

4.2.3. Design of resistor-less first-order all-pass filter using single VDVTA

All-pass filters (APFs) find applications where frequency dependence of phase, or phase linearity or group delay flatness can be major design consideration. They have been

exhaustively investigated over the last decade or so. As far as first-order APFs are concerned, most of these circuits use several passive components [55–58]. On the other hand, recently proposed resistor less first-order AP filters [56] use two capacitors (one of them is floating) and suffer from the need of passive component ratio-matching conditions, as well as product performance variability problems because of their dependence on op-amp internal compensation capacitors.

In analog signal processing, first-order all-pass filters are widely used to shift the phase of the input signal from 0 to 180° or from 180° to 0 while keeping its amplitude constant over the desired range of frequency.

Fig. 4-13 and Fig. 4-14 illustrate proposed transimpedance -mode all-pass filters using two OTAs with high input and low output impedances and its implementation by single VDVTA and one grounded capacitor, respectively.

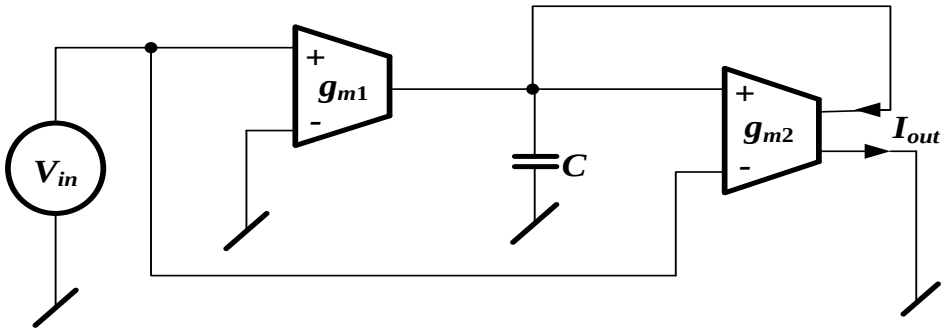


Fig. 4-13: The all-pass filter by OTAs.

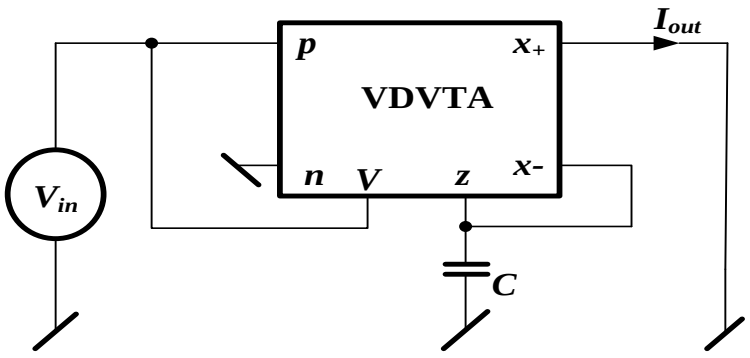


Fig. 4-14: Implementation of all-pass filter in Fig. 4-25 by using VDVTA.

The proposed circuits shown in Figs. 4-13 and 4-14 yield the following transimpedance transfer function:

$$\frac{I_{out}}{V_{in}} = \frac{g_{m1} - sC}{g_{m2} + sC} g_{m2} \tag{4-12}$$

The proposed APFs shown in Figs. 4-13 and 4-14 have been simulated using PSPICE. During these simulations, the CMOS-based structure of Fig. 3-12 has been used. The device model parameters are taken from TMSC 0.18μm CMOS process. The ±0.6V supply voltages all g_m equal to 96.8μs were used.

Figs. 4-15 and 4-16 show the magnitude and phase responses respectively for the all-pass filtering signal. The simulated results of all-pass filter by OTA obtained agree well with the VDVTA-based all-pass filter.

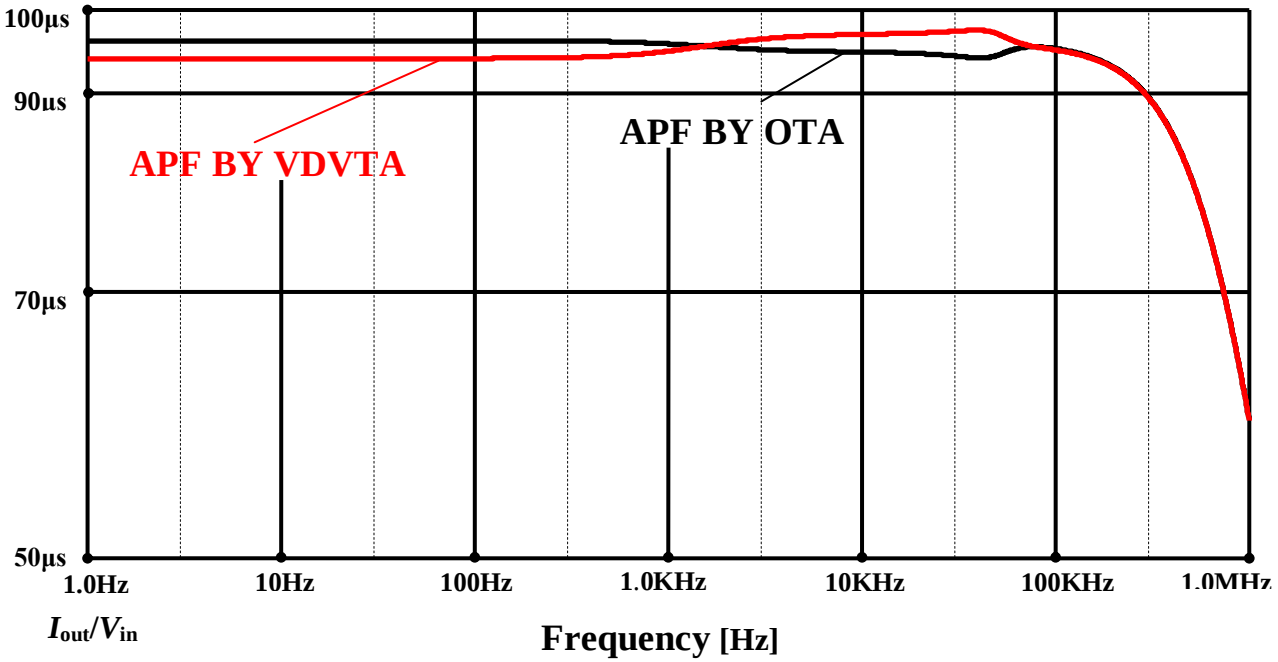


Fig. 4-15: Amplitude frequency responses of all-pass filters.

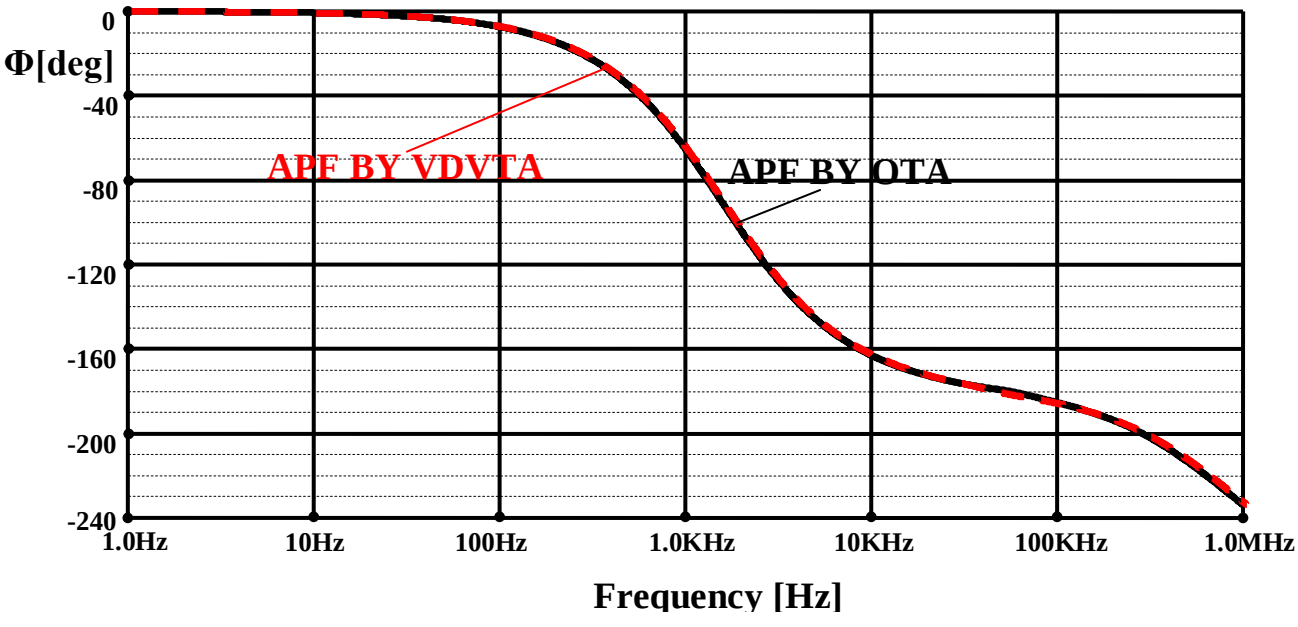


Fig. 4-16: Phase frequency responses of all-pass filters.

4.2.4. Design of KHN filter using VDTA

The Kerwin–Huelsman–Newcomb (KHN) biquad filter [59], [60] belongs to popular filter structures of the type of "two integrators in the feedback loop". An important feature of this structure is the generation of all three basic filter transfer functions, i.e., low-pass (LP), band-pass (BP), and high-pass (HP) simultaneously.

The well-known voltage-mode 2nd-order KHN filter [59], [60] in Fig. 4-17 is preferred building block for cascade filter design. This circuitry can be understood as a single-input three-output device, generating three basic 2nd-order transfer functions (low-pass, band-pass, and high-pass).

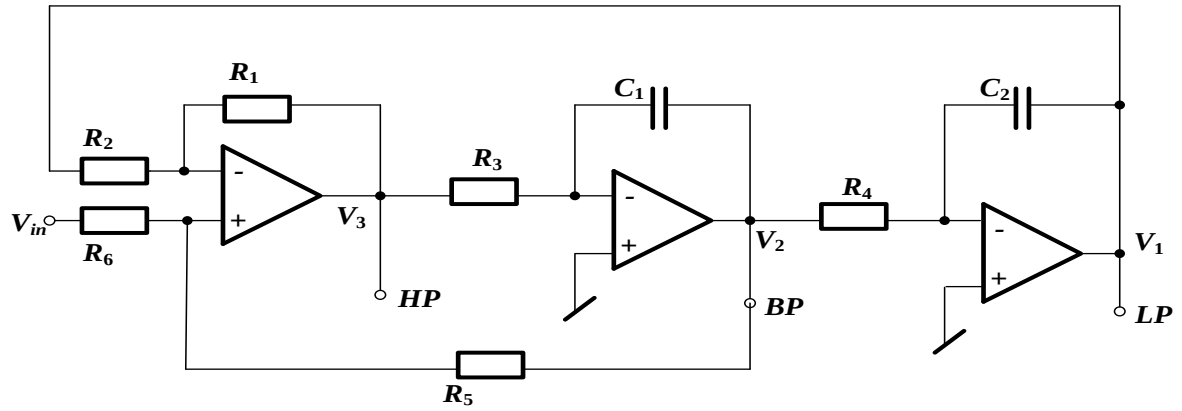


Fig. 4-17: Classical structure of the KHN filter.

In addition, as obvious from the flow-graph in Fig. 4-18, filter tuning without modifying the quality factor can be done by simultaneous modification of R_3=R_4. For identical values of R_1, R_2, R_5 and R_6 the DC gain of LP, high frequency gain of HP, and maximum gain of BP filters are fixed to their unity-values while tuning, and thus the upper bound of the filter dynamic range remains unchanged.

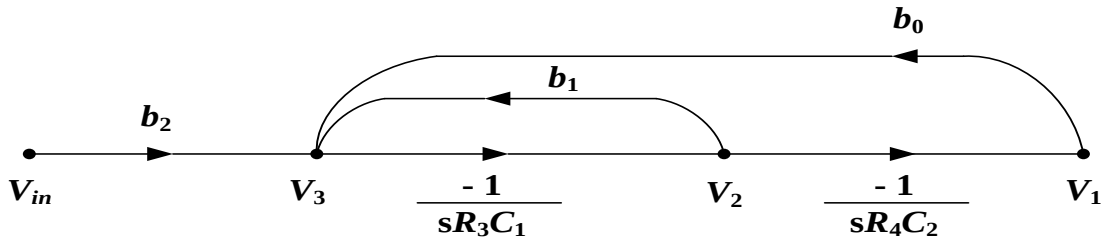


Fig. 4-18: The corresponding flow-graph of KHN in Fig. 4-29. For $R_1 = R_2 = R_5 = R_6$, $b_2 = b_1 = - b_0 = 1$.

Recently, many methods were published how to implement the KHN structure by means of active elements other than voltage Op Amps, in particular by current conveyors [61-63], but

also by CDBA (Current-Differencing Buffered Amplifier) [64], [65] or DO-DDCC (Differential-Output Differential Difference Current Conveyor) elements [45].

In this part, the classical KHN structure is transformed into the current mode by utilizing the VDTA (Voltage Differencing Transconductance Amplifier) circuit elements [66], whose input and output signals are currents. The final filter consists of only two VDTAs and two grounded capacitors, and thus it can be classified as so-called VDTA-C filter, an analogy with the well-known gm-C filters.

A possible CMOS-based VDTA circuit realization suitable for the monolithic IC fabrication is displayed in Fig. 3-12. The proposed VDTA-based CM KHN biquad is given in Fig. 4-19.

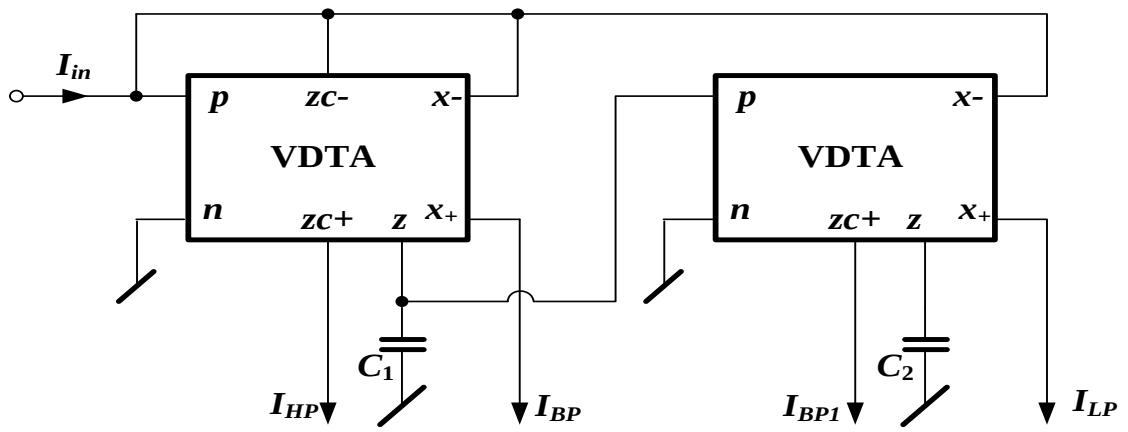


Fig. 4-19: VDTA-based CM KHN circuit.

The signal-flow graph in Fig. 4-18 can be redrawn for currents as shown in Fig. 4-20, together with the corresponding VDTA-based biquad. In contrast to conventional Op Amp, the VDTA enables an easy implementation of the non-inverting integrator. The non inverting integrators in the feedback loops require the signs of gains of the feedback branches to be modified, as follows from a comparison of the graphs in Figs. 4-20 and 4-18.

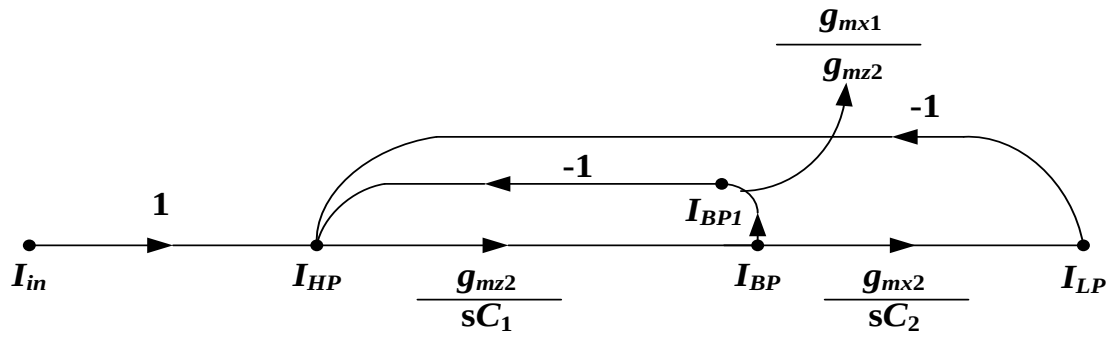


Fig. 4-20: The corresponding flow-graph of KHN in Fig. 4-31.

Evaluating the flow-graph in Fig. 4-32 yields the following transfer functions:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + s\,{g_{mx1}}/{C_1} + {g_{mz2}g_{mx2}}/{C_1C_2}} \tag{4-13}$$

$$\frac{I_{BP}}{I_{in}} = \frac{s\left({g_{mz2}}/{C_1}\right)}{s^2 + s\,{g_{mx1}}/{C_1} + {g_{mz2}g_{mx2}}/{C_1C_2}} \tag{4-14}$$

$$\frac{I_{BP1}}{I_{in}} = \frac{s\left({g_{mx1}}/{C_1}\right)}{s^2 + s\,{g_{mx1}}/{C_1} + {g_{mz2}g_{mx2}}/{C_1C_2}} \tag{4-15}$$

$$\frac{I_{LP}}{I_{in}} = \frac{{g_{mz2}g_{mx2}}/{C_1C_2}}{s^2 + s\,{g_{mx1}}/{C_1} + {g_{mz2}g_{mx2}}/{C_1C_2}} \tag{4-16}$$

Where

$$\omega_0 = \sqrt{\frac{g_{mz2}g_{mx2}}{C_1C_2}}, \qquad B = \frac{\omega_0}{Q} = \frac{g_{mx1}}{C_1} \tag{4-17}$$

$$Q = \sqrt{\frac{C_1}{C_2}}\,\frac{\sqrt{g_{mz2}g_{mx2}}}{g_{mx1}} \tag{4-18}$$

It follows from Eqs (4-13), (4-14), (4-15), and (4-16) that the above filter structure in Fig. 4-19 provides basic highpass, lowpass, and bandpass operations. Due to current output signals, a simple implementation of other types of the transfer functions can be accomplished via a proper combination of these currents.

It follows from Eqs (4-17) and (4-18) that

(a) the natural frequency ω_0 can be tuned via the transconductances g_{mz2} and/*or* g_{mx2} and/or via capacitance C_2 without disturbing the filter bandwidth B,

(b) the filter bandwidth B can be controlled independently of ω_0 via g_{mx1},

(c) the quality factor Q can be controlled independently of ω_0 via g_{mx1}.

To verify the theoretical analysis, the CM KHN filter configuration presented in this study is simulated in SPICE circuit simulation program using the CMOS-based VDTA circuit given in Fig. 3-12. Here, 0.18 μm MIETEC real transistor model parameters are implemented for all

transistors in the circuit. The symmetrical supply voltages of ±0.6V were used. Fig. 4-21 demonstrates the results of CM KHN biquad circuit simulations when $C = C_1 = C_2 = 10$ nF, $g_{mx1} = g_{mz1} = g_{mx2} = g_{mz2} = 96.82$ μS, which corresponds to the theoretical natural frequency of 1.57 kHz. The simulated value is 1.54 kHz. Therefore, the CMOS-level simulation confirms well the theoretical assumptions.

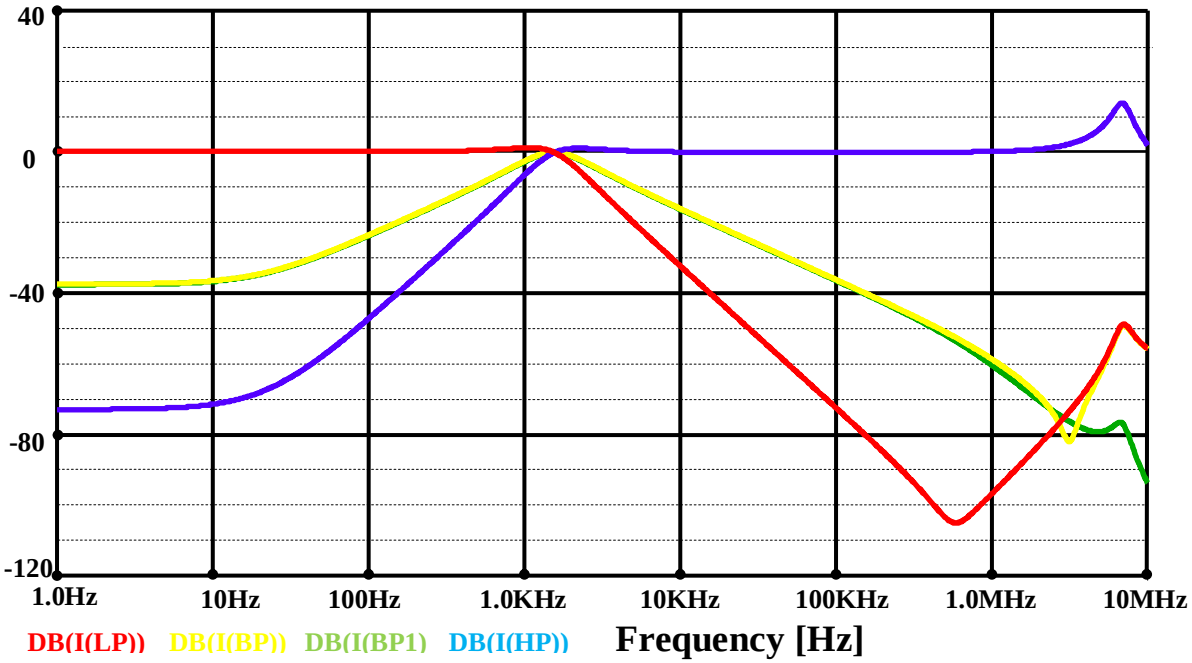


Fig. 4-21: Results of circuit simulations for CM KHN circuit using CMOS-based VDTAs.

5. Conclusion

In the last decade, for analogue signal processing huge number of active building blocks was introduced, however, there is still the need to develop new active elements that offer new and better advantages. Therefore, the main contribution of this thesis was the definition of such novel ABBs, and their application possibilities.

The theoretical and practical results of the work were presented in two main chapters, which introduced the novel introduced blocks and moreover proved the possibility of the implementation of these blocks. The new high linearity, wideband bulk-driven OTA with tunable transconductance was designed. This OTA is then used for designing active building blocks (CDTA, VDTA, VDVTA, and DVCC). In this thesis I presented some new active building blocks as (VDTA, and VDTVA). As applications, several filters structures current-, voltage- and mixed-mode by using VDTA, and VDVTA was presented.

Novel structures of first-order all-pass filters based on VDVTA and novel structures of second-order universal filters, KHN-equivalent circuits by novel active element (VDTA) proposed in this thesis. Thesis also was focused on LC ladder simulation on the principle of inductor replacement by synthetic inductor.

The floating inductor was synthesized via:

1. MAX435, a commercial OTA [46], [53], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well-known circuitry for simulating the floating inductor. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.
2. „super-transistor“ (S-T), which is commercially available in several versions, e.g. OPA615, SHC615, OPA860, and OPA861 [53].
3. Newly introduced VDTA and VDVTA elements [45] designed in the first part of the thesis.

The presented work represents the investigation on building blocks for modern current-mode and mixed mode based integrated circuits. A number of novel introduced building blocks together with their implementation are the results. The functionality of the proposed blocks was proved by simulations in the SPICE programme.

With respect to the above discussion it can be declared that aims of this thesis were fulfilled.

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Curriculum Vitae

Personal Details:

Name:	Mahmoud Ahmed Shaktour
Date of birth:	29. 09. 1973, Tripoli–Libya
Phone:	+420 774 101 074
Nationality:	Libyan
Contact:	xshakt00@stud.feec.vutbr.cz, ztoever2002@yahoo.co.uk

Address: University of Nasser, Faculty of Science
Department of Physics, Alkhoms-Libya, North Africa

Education

1999-2003: University of Nasser – teacher

2004-2007: Brno University of Technology (M.Sc in Microelectronics)

2007-2010: Technical University of Brno (Ph.D. study)

Experience

From 1999 Lecturer at University of Nasser, Faculty of Science,

Department of Physics.

Languages:

Arabic, English

ABSTRACT

Frequency filters are linear electric circuits that are used in wide area of electronics. They are also the basic building blocks in analogue signal processing.

In the last decade, a huge number of active building blocks for analogue signal processing were introduced. However, there is still the need to develop new active elements that offer new possibilities and better parameters. The current-, voltage-, or mixed-mode analog circuits and their various aspects are discussed in the thesis. This work reflects the trend of low-power (LP) low-voltage (LV) circuits for portable electronic and mobile communication systems and the problems of their design. The need for high-performance LV circuits encourages the analog designers to look for new circuit architectures and new LV techniques.

This thesis presents various active elements such as Operational Transconductance Amplifier (OTA), Current Conveyor of Second Generation (CCII), and Current Differencing Transconductance Amplifier (CDTA), and introduces novel ones, such as Voltage Differencing Transconductance Amplifier (VDTA) and Voltage Differencing Voltage Transconductance Amplifier (VDVTA). All the above active elements were also designed in CMOS bulk-driven technology for LP LV applications.

This thesis is also focused on replacement of conventional inductors by synthetic ones in passive LC ladder filters. These replacements can lead to the synthesis of active filters with interesting parameters.

ANOTACE

Kmitočtové filtry jsou lineární elektrické obvody, které jsou využívány v různých oblastech elektroniky. Současně tvoří základní stavební bloky pro analogové zpracování signálů.

V poslední dekádě bylo zavedeno množství aktivních stavebních bloků pro analogové zpracování signálů. Stále však existuje potřeba vývoje nových aktivních součástek, které by poskytovaly nové možnosti a lepší parametry. V práci jsou diskutovány různé aspekty obvodů pracujících v napěťovém, proudovém a smíšném módu. Práce reaguje na dnešní potřebu nízkovýkonových aplikací pro přenosné přístroje a mobilní komunikační systémy a na problémy jejich návrhu. Potřeba těchto výkonných nízkonapěťových zařízení je výzvou návrhářů k hledání nových obvodových topologií a nových nízkonapěťových technik.

V práci je popsána řada aktivních prvků, jako například operační transkonduktanční zesilovač (OTA), proudový konvejor II. generace (CCII) a CDTA (Current Differencing Transconductance Amplifier). Dále jsou navrženy nové prvky, jako jsou VDTA (Voltage Differencing Transconductance Amplifier) a VDVTA (Voltage Differencing Voltage Transconductance Amplifier). Všechny tyto prvky byly rovněž implementovány pomocí "bulk-driven" techniky CMOS s cílem realizace nízkonapěťových aplikací.

Tato práce je rovněž zaměřena na náhrady klasických induktorů syntetickými induktory v pasivních LC příčkových filtrech. Tyto náhrady pak mohou vést k syntéze aktivních filtrů se zajímavými vlastnostmi.