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PROGRESS TOWARD THE DEVELOPMENT OF SINGLE NANOWIRE-BASED ARRAYS FOR GAS SENSING APPLICATIONS

POKROK VE VÝVOJI SNÍMACÍCH POLÍ ZALOŽENÝCH NA JEDNOM NANODRÁTU A JEJICH VYUŽITÍ
V OBLASTI DETEKCE PLYNŮ

DOCTORAL THESIS

DIZERTAČNÍ PRÁCE

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Abstract

This thesis presents the development of silicon-based platforms for selective integration of semiconducting metal oxide (MOX) nanostructures and their use as highly sensitive and selective elements for the detection of gas analytes in prospective mobile devices. Semiconducting MOX nanostructures, for instance nanowires, have proved better gas sensing properties including sensitivity, stability and to a certain extent also selectivity as compared to their bulk counterparts. The use of single (or few) nanowire structures connected in parallel has also shown to be the ideal architecture to achieve well-defined conduction channel easy to modulate by the gas-solid interactions. However, yet current methods for the integration of single nanowire structures in functional devices represent a technological challenge, with most of the methods needing the assistance of techniques, such as focused-ion beam (FIB), which restricts the scalability of the process and increases the cost and time of fabrication. In this context, this work is focused on the search and optimization of technological processes to fabricate gas sensing systems based on arrays of single semiconducting nanowires.

In this thesis, three versions of electrode platforms were developed for the selective integration of single gas-sensitive metal oxide nanowires. State-of-the-art multistep throughput fabrication techniques, as well as electron-beam lithography (nanofabrication), were used as crucial fabrication technologies allowing the development of arrays with faced nanoelectrodes and other functional nanostructures. Results show the fabrication of electrode platform with faced nanoelectrodes (100 – 300 nm width) framed in narrow dielectric windows close to the nanowire diameter (100 – 200 nm approx.). These nanoelectrodes were used as both mechanical support to align the single nanowire, and electrical contacts to measure the electrical change along the nanowire during gas detection. Results also include the optimization of techniques for removal and redeposition of nanowires to achieve single nanowire interconnections in the array of parallel electrodes using an alternating electric field as a simple and effective technique for nanowires alignment (dielectrophoresis).

The validation of these systems toward various gaseous species (oxidizing and reducing gases) was performed using non-functionalized and Pt-functionalized WO_3 nanowires synthesized by aerosol-assisted chemical vapor deposition (AACVD) and backside ceramic heaters (with the operating temperature at 250 °C) assembled on TO-8 package. The sensing parameters of such systems showed better sensing responses in resistive regime to nitrogen dioxide (NO_2) and ethanol (EtOH) than their counterparts based on multiple nanowire-based films. The last version of gas sensing systems developed in this thesis (described as third chip generation) includes a third insulated electrode buried under the gas sensitive nanowire for enhanced gas sensing regime. Gas sensing tests of this system to hydrogen (H_2) and nitrogen dioxide (NO_2) corroborated the enhanced functionality of these systems and the modulation of sensor response by applying external electrical stimuli on the buried electrode.

Keywords

Electrode platform, nanoelectrodes, array of single nanowires, nanowire alignment, sensing system, gas detection.

Abstrakt

Tato práce se zabývá vývojem platforem na bázi křemíkového substrátu pro selektivní integraci polovodivých nanostruktur oxidu kovu (MOX) a jejich použití v perspektivních mobilních zařízeních jako vysoce citlivé a selektivní prvky pro detekci analytů plynů. Polovodičové nanostruktury MOX, například nanodráty, prokázaly lepší schopnosti pro snímání plynů včetně citlivosti, stability a do jisté míry také selektivity, ve srovnání s jejich protějšky na bázi vrstev. Rovněž použití jednoho (nebo několika) nanodrátů zapojených paralelně se ukázalo jako ideální architektura pro dosažení dobře definovaného vodivého kanálu snadno modulovatelného interakcemi na přechodu plynná-pevná látka. Dosavadní způsoby integrace struktur na bázi jednoho nanodrátu do funkčních zařízení však stále představují technologickou výzvu, protože většina metod vyžaduje asistenci technik, jako je soustředěný iontový paprsek (FIB), který omezuje škálovatelnost a zvyšuje náklady a čas výroby. V této souvislosti je práce zaměřena na optimalizaci technologických procesů pro výrobu systémů založených na elektrodových polích s jedním polovodivým nanodrátem.

V této práci byly vyvinuty tři verze elektrodových platforem pro selektivní integraci jednoho nanodrátu z MOX materiálu citlivého na plyn. Jako klíčové technologie výroby byly použity nejmodernější vícestupňové výrobní postupy a litografie s využitím elektronového paprsku (nanofabrikace), které umožňují vývoj elektrodových polí s přímými nanoelektrodami, ale i dalších funkčních nanostruktur. Výsledky demonstrují výrobu elektrodové platformy s přímými nanoelektrodami (šířky 100–300 nm), na kterých se nachází úzká dielektrická okna s šířkou blízké průměru nanodrátu (přibližně 100–200 nm). Tyto nanoelektrody byly použity jako mechanická podpora pro zarovnání jednoho nanodrátu a rovněž jako elektrické kontakty pro měření elektrické změny nanodrátu během detekování plynu. Výsledky také zahrnují optimalizaci technik pro odstraňování a opětovné nanášení nanodrátů pro dosažení jedno nanodrátových propojení v poli paralelních elektrod pomocí střídavého elektrického pole jako jednoduché a účinné metody pro zarovnávání nanodrátů (dielektroforéza).

Ověření těchto systémů vůči různým plynným látkám (oxidačním a redukčním plynům) bylo provedeno za použití nefunkcionalizovaných a Pt-funkcionalizovaných WO_3 nanodrátů syntetizovaných pomocí aerosolové chemické depozice par (AACVD) a topného prvku na bázi tlusté vrstvy na korundové keramice (s provozní teplotou 250 °C), sestaveného spolu s elektrodovou platformou na pouzdru TO-8. Snímací vlastnosti takových systémů vykazovaly lepší citlivost v odporovém režimu na oxid dusičitý (NO_2) a ethanol (EtOH) než jejich protějšky využívající nanodrátových filmů. Poslední verze systému pro snímání plynu vyvinutého v této práci (popsaná jako třetí generace čipů) obsahuje třetí izolovanou elektrodu zabudovanou (utopenou) pod citlivým nanodrátem pro zvýšení detekční schopnosti snímání plynu. Testy odezvy na vodík (H_2) a oxid dusičitý (NO_2) potvrdily zvýšenou funkčnost tohoto systému modulující odezvu senzoru pomocí externího elektrického napětí na utopené elektrodě.

Klíčová slova

Platforma s elektrodovým polem, nanoelektrody, pole založené na jednom nanodrátu, zarovnávání nanodrátů, sensitivní systém, detekce plynů.

Bibliographic citation

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Declaration

I declare that I am the author of the doctoral thesis "Progress in the development of single nanowire-based for gas sensing applications" under the supervision of Assoc. Prof. Jaromír Hubálek, and Dr. Stella Vallejos Vargas, using specialized literature and other information sources, all of which are cited in this work and listed in the bibliography at the end of the work.

As the author of this dissertation, I further declare that in connection with the creation of this dissertation I have not infringed the copyrights of third parties, in particular, I have not infringed illegally on foreign personal rights, and I am fully aware of the consequences of violating Section § 11 and subsequent Copyright Act No. 121/2000 Coll., including possible criminal consequences arising from the provisions of Section § 152 the Criminal Code No. 140/1961 Coll.

Brno, 12th September 2019

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Ing. Ondřej Chmela, author

Acknowledgments

„Člověk přišel na svět proto, aby tady byl, pracoval a žil. Jen moudrý se snaží náš svět postrčit dál, posunout výš. A jen vůl mu v tom brání.“

"Human came into the world to be here, work and live. Only the wise seek to push our world further, to move higher. And only the ox stands in his way."

Jan Werich

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Introduction, motivation, and aims of the thesis

Environmental surveillance is still an important topic in the agenda of government enforces agencies, which in the last years have increased their interest in monitoring emissions continuously at the source, with cross-stack instruments designed to detect particular measurands in reasonable well-known background matrix. The efficiently of this approach relies on the availability of gas sensing systems with increased measurement capabilities and decreased overall capital cost for multiple gas detection so that they can cover wider geographical area with a larger network of monitoring stations. Current gas sensing systems, however, do not fulfill all these requirements, and therefore the interest in further technological improvements of these systems. Generally, the deployment of advanced gas sensing elements could contribute to better control of air pollution and thus have an impact in the following areas.

Human health

Air pollution is one of the most significant environmental health risks in Europe and worldwide causing a wide range of diseases (e.g., lung cancer, cardiovascular and respiratory diseases). Also, air pollution has been associated with adverse influences on fertility, pregnancy, newborns, and children. In particular, it has a negative effect on neural development and cognitive abilities, which can lead to low performance at school and later to a lower quality of life [1]. Another diseases (except hearth and lung diseases), which are responsible for cases of premature death attributed to air pollution, are stroke and new-onset type two diabetes in adults [2].

Ecosystem and climate changes

Air pollution also has several environmental impacts on the ecosystems (e.g., vegetation, quality of water). Here are a few pollutants which causing biodiversity loss. For instance, high levels of nitrogen oxides (the sum of nitrogen dioxide (NO_2) and nitrogen monoxide (NO)), ammonia (NH_3), Volatile Organic Compounds (VOC) and sulfur dioxide (SO_2), burden aquagenic and terrestrial ecosystems by excessive quantities of nitrogen and sulfur. This contributes to the acidification of soil, rivers, and lakes.

Also, it is a well-known fact that several air pollutants have an impact on global weather changes. For instance, ground-level ozone (O_3) formation, formed in the lower part of the atmosphere, methane (CH_4) or carbon dioxide (CO_2). All of these pollutants and their increasing tendency of occurrence are a serious worldwide problem. As an example can be used increasing of the methane production(CH_4), which is characterized as a greenhouse gas (GHG). GHG emissions are presupposed to rise by 50 % in 2050 compared to 2011, and from a global perspective, up to 18% of global GHG emission is accounted to the livestock sector, the dairy cow production, respectively. [3,4]

Economic and cultural impacts

In light of the actual conditions of air pollution, which have the evidential influence on human health, the global climate, and ecosystems, it should also emphasize the potential economic consequences of the deteriorating air conditions in the future. The European Commission estimated that total health-related external costs in 2010 were in the range of EUR 330–940 billion, including direct economic damages of EUR 15 billion from lost workdays, EUR 4 billion from healthcare costs, EUR 3 billion from crop yield loss and EUR 1 billion from damage to buildings. [5]

The Organisation for Economic Co-operation and Development (OECD) projects market costs (e.g., additional health expenditure, forest yield losses) reach about 2% of European gross domestic product (GDP) in 2060, leading to a reduction in capital accumulation and a slowdown in economic growth. Non-market costs (also referred to as welfare costs) are those associated with increased mortality and morbidity (illness-causing, for example, pain and suffering), degradation of air and water quality and consequently ecosystems health, as well as climate change. Globally, air pollution could cause 6 to 9 million of premature deaths a year by 2060 and cost 1% of global GDP (around 2.6 trillion USD annually), as a result of sick days, medical bills and reduced agricultural output. [6]

Indeed, new technologies brought many benefits to our new modern lives. However, they also brought many inconveniences, such as the increase of unwanted global release of air pollutants that will result in enormous costs to cover those environmental and health losses in the next few decades. The consequences are very significant, and there is a need to call for strong policy actions, which need to be supported by the implementation of advanced monitoring technologies for environmental surveillance, restoration, and remediation.

Motivation

Gas sensing systems are expected to play a notable role in environmental control and monitoring, to secure a better quality of life for the next generations [7,8]. The necessity of gas sensing in different fields (industrial safety, security, environmental surveillance, biomedical, to cite few) has been analyzed previously by the global gas sensor market, which predicts a gas sensor market size of USD 1.82 billion in 2016 and an estimated growth at a CAGR (Compound Annual Growth Rate) of 7.5 % from 2017 to 2025 [9]. Therefore, the fabrication of the new generation of gas sensing systems requires the deployment of advanced techniques and concepts that allow not only for high performance elements, but also for low power consumption miniaturized systems so that they can be integrated in portable or wearable components, as opposed to the current gas sensing technologies in the market [10].

These new characteristics could facilitate the approach of these systems into a human's ordinary life, for example, by means of sensing platform integrated into mobile (portable) devices, such as smartphones. Thus, everybody could have the chance to monitor the actual air

conditions (toxicity of the pollution) and control the areas that could possibly represent a risk. This could also have other effects, as these smart sensors become part of the equipment of our mobile phones so that the data recorded can be potentially used for real-time detection and shared with other users to inform the current air situation in their vicinity. Online health monitoring from exhaled breath is another possible application, which could also bring positive benefits for preventive medicine [11]. All this would allow to ordinary people to have clear records based on evidence from millions of mobile sensors in their hands that the environment in their city, village, or region, is dangerous to their health. Thus, it can increase the pressure on politicians to do fundamental changes in the policies.

In this context, during the last decades, many researchers have focussed on different aspects that involve gas sensing technologies. Thus, a variety of sensors, systems, and technologies have been developed for sensing and monitoring gases or vapors. Pellistors, electrochemical, optical, and thick film metal oxides (MOX) are the most famous gas sensing devices; however, these technologies do not accomplish the above-mentioned conditions of size, cost, and performances at low concentration levels. As an alternative, gas sensor based on nanomaterials (particularly semiconducting oxides) and micro/nanotechnologies are good candidates for this application as they can allow for miniaturized gas detectors. The miniaturization of devices reduces material consumption in device manufacture and reduces power consumption in device operation. Sensors miniaturization also offers faster response times and lower detection limits than traditional commercial ceramic-based devices, enabling sensors to be deployed on-site and making real-time detection possible.

One-dimensional (1D) semiconducting metal-oxide (MOX) nanostructures in the form of nanowires, nanorods or nanobelts have demonstrated to play a significant role in the functional properties of gas sensing systems, typically improving their performance, as opposed to bulk MOX. For instance, 1D MOX have demonstrated to improve parameters, such as the sensitivity and stability of the sensing element, and also, to a certain extent, the selectivity [12] [13]. It has also been demonstrated that gas sensors based on a single (or few) nanowire structures connected in parallel are the ideal architecture to achieve well-defined conduction channel easy to modulate by external stimuli (e.g., gaseous molecules) [12,14-17]. However, yet current methods for the integration of single nanowire structures in functional devices represent a technological challenge, with most of the methods needing the assistance of techniques, such as focus ion beam (FIB), which restricts the scalability of the process and increases the cost and time of fabrication [18,19]. **In this context, this work is focussed on the search and optimization of technological processes to fabricate gas sensing systems based on arrays of single semiconducting nanowires.**

Aims of the dissertation

To address the fabrication of single nanowire-based system **this thesis is centered in two general aims (1) the development of platforms provided of nanoelectrode arrays for the selective integration of single gas-sensitive metal oxide nanowires and (2) the validation of these platforms toward various gaseous species.** To achieve these general aims, it was necessary to face several scientific and technological issues; therefore, the specific aims were set to provide systematic feedback at each step and thus improve the whole system fabrication process. The specific aims and the most relevant tasks carry out to reach these aims are summarized below.

1. **Determination and optimization of nanowires processing techniques** – this aim was focused on finding the appropriate techniques for the removal (from a basic substrate) of the as-deposited AACVD nanowires. The transfer, positioning, and integration of nanowires into the prefabricated electrode arrays using approaches that provide large-scale and easier processability have also been selected and optimized. The optimization of this process includes the setup of techniques suitable to obtain nanowires without significant disturbance of their length, ready to be transported (redeposited) onto the electrode array and integrated between the electrodes as single structures interconnected in parallel by dielectrophoresis technique.

2. **Setting of the protocol for the fabrication of electrode arrays to provide mechanical support and electrical connectivity to single nanowires** – the tasks within this aim dealt with the design and implementation of key processing technologies (particularly lithography and etching processes) for the fabrication of arrays of electrodes on silicon platforms. The designs were adjusted based on the features (length and diameter) of the gas-sensitive nanowires (previously developed via aerosol-assisted chemical vapor deposition - AACVD). Three generations of structures were fabricated within this aim, and each one was redesigned and improved based on the feedback obtained from a previous generation in order to achieve the interconnection of several single nanowires in parallel. The last improved modification includes the introduction of an additional electrode system for gas sensing enhancement. It is worth to mention that the processing fabrication techniques for this aim were adjusted to produce structures in the nanoscale order.

3. **Assembling of the gas sensing system** – due to the need for a heating element to activate the gas-sensitive structures, an assembly process was required before the application of the fabricated systems. Therefore, this aim was centered in assembling the electrode arrays platform together with a heater element into a package. This step also included the electrical connection of the elements for their characterization and control (to measure the gas responses and control the heater for the set of temperature).

4. **Development and implementation of the gas characterization system** – a system for the validation of the assembled sensing device functionality under exposure to various gases has been developed. The design of the gas testing chamber was addressed to allow the measurement of highly sensitive materials (nanowire), so the design includes (1) maximal electromagnetic interference shielding for low current measurement (high resistance of nanowires), (2) high gas exchange rate, and also (3) minimal adsorption of the chamber.

5. **Gas sensing characterization in resistive mode** – the electrode array platform with integrated nanowires have been tested under the exposure to various gases (reducing, oxidizing) and their concentrations. The characterization of the sensing system revealed the parameters for maximum performance, for instance, the appropriate sensing current with good S/N ratio, or the operational temperatures with the highest gas response. Effect of the nanowires (pristine metal oxide) with their surface functionalized by catalytic nanoparticles and its influence on the selectivity and sensitivity of sensing elements have also been examined.

6. **Gas sensing characterization in enhanced mode** – the planar arrangement with the nanowires across the electrodes offers the possibility to control the conductivity of the nanowire channel using an additional (third) electrodes system. The effect of the additional (third) electrode on the gas response, related to the sensitivity and selectivity, has been evaluated in the presence of various gases. This third electrode proved to enhance the sensing properties of the sensing elements due to the applied electric field forces provided to the gas sensitive nanowire.

Scientific contribution

This dissertation presents a summary of the author's doctoral thesis. The efforts of this work were focussed on developing single-nanowire based gas sensing element. The most relevant aspects developed in this thesis include the methodology for fabricating miniaturized electrode platform systems provided of several arrays with parallel faced electrodes. To this end, several advanced fabrication processes were adjusted and optimized, including the e-beam lithography process for nanoscale fabrication.

The novelty of the developed platforms consists in achieving the parallel connection of various single nanowires in parallel by using electric forces (method) and by modifying the width of the electrode close to the dimensions of the nanowire diameter (structure). This breakthrough opened the door to assemble different types of nanowires in one sensing platform, and thus improve the selectivity of the sensor. This, also contribute to developing other novel structures, described along with the thesis as the third chip generation, which proved the functionality enhancement of planar aligned single NWs interconnected in parallel by external electrical stimuli applied on a third electrode buried under the NWs.

Dissertation structure

Chapter 1 was dedicated to the theoretical knowledge dealing with solid-state gas sensors based on MOX semiconductors, their working principle with special emphasis on sensing element and the ongoing processes between the sensitive material and adsorbed gas molecules during gas-solid interactions (receptor function), or the mechanism that give rise to the response of gas sensors (transducer function). Thus, influencing effects of the grain size, shape, crystalline quality, or surface functionalization, on the sensor sensitivity and selectivity with the emphasis on single-crystalline materials, were also presented. The last **section (1.3)** of this chapter was addressed to introduce sensing system based on multiple NWs, or single NWs, and their possible electrodes arrangements with particular focus on single NW based platforms and its feasible solution.

The fabrication and development techniques employed during the experimental part of this work were briefly described in **Chapter 2**. Some techniques are compared to each other, for example, to determine the suitability of each technique related to the chosen fabrication approach, as it was the case for the deposition techniques. The e-beam lithography is among the most important techniques used in this work. Without the tune of this process in the current work the required dimensions of the proposed electrode platform solution could not be achieved. The results of the experimental part were presented in **Chapter 3**, **Chapter 4**, and **Chapter 5**, which reflect the degree of maturation both of the designs and processing techniques adjustment. Therefore, these chapters are entitled as first, second and third chip generation. To close the dissertation, the conclusions associated with each objective were summarized (presented) in **Chapter 6**.

1 State of the art

1.1 *Classification and characteristic parameters of gas sensors*

A gas sensor is an essential component of an analyzer. In addition to the sensor, the analyzer may contain devices that perform the following functions as sampling, sample transport, signal processing, and data processing. An analyzer may be an essential part of an automated system. The analyzer working according to a sampling plan as a function of time acts as a monitor. [20] Generally, some specific parameters are used in order to evaluate the monitored signal produced by the sensor, which will be explained below.

- **Sensitivity and sensor response** - the sensitivity is defined as the ratio between the change in the sensor resistance and the change in the gas concentration represented by calibration curve, the slope of the calibration curve, respectively. A more general definition of sensitivity is the ability of a certain method to distinguish between two very close concentration. From this, it can be said that it is related also with sensor response. The maximum relative response of the chemiresistor to the analyte can be expressed as [21]:

$$SR = \frac{\Delta R(\infty)}{R_0} \cdot 100\% = \frac{R_{max} - R_0}{R_0} \cdot 100\% \qquad (1.1)$$

where R_0 is the resistance of the sensor in the absence of the analyte and R_{max} is the resistance of the sensor in the presence of the analyte. Another frequently used an alternative definition of the sensor response for n-type oxides is:

$$SR = \frac{R_{air}}{R_{gas}} \ (reducing\ gas), \qquad SR = \frac{R_{gas}}{R_{air}} \ (oxidizing\ gas) \qquad (1.2)$$

where R_{air} is the resistance of the sensor in the absence of the analyte and R_{gas} is the resistance after the subjection to the gas. For oxidizing and reducing gas, in the case of p-type oxides, are these equations reverse. Figure 1 depicts a typical response curve of the gas sensor during gas exposure, where ON determines the time when the flow solution is switched from the buffer, mostly synthetic air, to buffer containing the analyte of interest, OFF is the time when the flow is switched back to the buffer solution without target analyte.
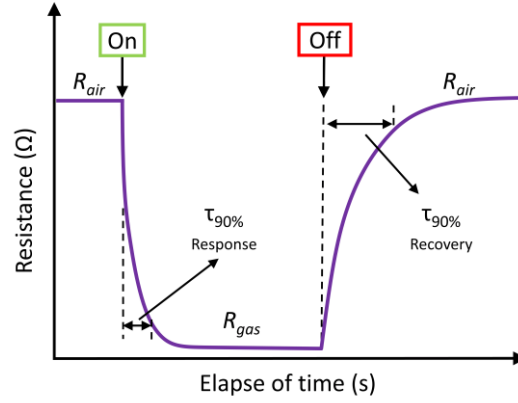
Figure 1. Typical response curve during gas exposure. Adapted from [22].

- **The response time and recovery time -** in gas detection, response time is usually defined as the time taken to achieve 90 % of the final change in resistance following a step change in gas concentration at the sensor and reverse for the recovery time. Often this time is quoted to 50 % or 70 % of the final change. This derives from the response often being very fast initially but having a long-drawn-out tail before the constant value is reached. The shape of the curves can vary from one gas to another. The response time is an important parameter since its value can determine the applicability of the sensor.

- **Selectivity -** the data about the different gases makes it possible to determine the selectivity of one gas relative to that of the other gases at any point in the temperature range. The selectivity is usually defined as:

$$Selectivity = \frac{Sensitivity\ to\ gas\ 1}{Sensitivity\ to\ gas\ 2} \qquad (1.3)$$

for equivalent concentrations of both gases, or, sometimes for the concentration of the gases known to be involved in the application of interest. Thus, from the study of sensitivities, an optimum temperature or range of temperatures over which the selectivity is acceptable can be determined.

- **Stability -** a gas sensor should be stable in a variable ambient atmosphere. It must also be reversibly unstable in the presence of the gases to be detected. These requirements are difficult to meet simultaneously. Slow changes in the properties of the bulk material or the near-surface region are almost inevitable. Such slow changes, which are the result of changes in the ambient atmosphere or temperature, are called drift.

- **Lower Detection Limit -** is the lowest quantity of an analyte that can be recognized from the absence of the analyte (a blank value) with a stated confidence level which is generally 99%. The detection limit is determined by the sensitivity and noise levels in sensor response. It is often assumed in gas sensor characterization that the limit of detection is reached when the response signal is three times higher than the noise level.

1.2   *Solid-state chemical sensors – metal oxide based gas sensors*

As stated above, the demand for using real-time detection and monitoring is going to be more common in domestic and industrial activities. Generally speaking, a chemical sensor is a device that transforms chemical information into an analytically useful signal (e.g., electrical, optical) for chemical information that can be connected with the concentration of the specific analyte and/or its composition. Traditional analytical instruments, such as mass spectroscopy or chromatography are expensive, complex, bulky and require sample preparation, restricting real-time analyses. In contrast, solid-state chemical sensors have a relatively simple architecture, they are small and can be miniaturized further by using micro/nano technologies for their operation in low-cost portable devices. [23,24]

Nowadays, a large number of different solid-state based gas sensors have been reported due to the productive interdisciplinary science related to solid-state chemistry, physics, biology and so forth. Solid-state gas sensors can be based on a variety of materials, structures, and detection principles. For example, in term of materials, either organic or inorganic materials such as semiconducting metal-oxides or polymers are used as active sensing layers in solid-state gas sensors. Those materials, usually, are in the form of thick/thin films or nanostructures. Also, solid-state gas sensors can work based on various approaches to obtain the desired read-out from the sensitive material. These approaches are generally connected with the physical change used as a detection principle. Thus, typically the electrical conductivity is used as read-out information in chemoresistive gas sensors, mass in piezoelectric sensors (surface acoustic wave, microcantilevers, etc.), optical parameters as reflection, fluorescence or interferometry in optical sensors (fibre optic or thin films), heat or temperature in catalytic gas sensors (Seebeck effect, pellistors) or electromotive force in electrochemical gas sensors. [25]

Solid-state gas sensors have numerous advantages including the possibility to miniaturize the final sensing device using the optimization of silicon micro/nano fabrication techniques, which helps the mass sensor production at low cost. Miniaturization also represents the possibility to get a device with low power consumption, easy integration with electronics and portability. A variety of inorganic materials, typically based on semiconducting metal oxides have proved to detect a wide range of gaseous chemical compounds, but also different reaction capability to them. Actually first gas sensors based on semiconductors were used for detection of explosive gas leakages in residential premises and pollutants inside cars in the 1950s, after the initial publication of gas-sensitive effects on germanium by Brattain and Bardeen [26], then metal oxides were recognized as possible sensitive materials by Heiland et al. [27] and Bielanski et al. [28]. Seiyama et al. published the first report of MOX semiconductor gas sensor in the early 1960s [29]. They manage to develop a new gas detector based on ZnO thin film utilizing the semiconductor catalysis mechanism, where the adsorption and desorption of gaseous compounds cause oxidation and reduction of the surface which evoke a change in the electrical conductivity of the sensing layer. This was a breakthrough advancement which has triggered a new pathway toward the development of new gas sensors based on various MOX

materials. Later, Taguchi has patented a gas sensor based on SnO_2 and commercialized it as household gas alarms in 1969. [30]

A search in the literature (see pie chart in Figure 2) shows that metal oxides such as SnO_2 or ZnO are the most common materials. Commonly metal oxide based gas sensors work in resistive mode, i.e., sensing the changes produced in the electrical resistance of the material due to the gas-solid interactions characterized by the exchange of electrons. [31,32]

However, the gas sensor based on metal-oxides also have some disadvantages, particularly regarding long-term stability and reproducibility. These undesired problems are related to the sensor functionality during an extended working period. In literature, this is a phenomenon known as "aging effect." There are two types; the first is defined as a drift of the baseline values, which can be conductance or resistivity in air or reference gas. The second is linked to the drift in the sensor response with respect to the calibrated response values. The lack of stability is mainly caused by morphological changes in grains and intergranular boundaries of sensing elements, irreversible reactions with chemical species in the ambient or changes in parameters of the heating element or the electrodes due to aging. [33,34]
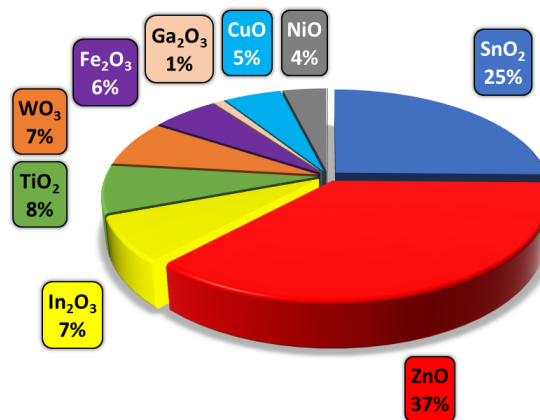
Figure 2. Published research on metal-oxide material for gas sensors performed by using the Web of Science database from 1998 to 2018.

Figure 2 also reveals other metal oxides with potential in gas sensings, such as In_2O_3, TiO_2, and WO_3. In the last few years, these materials have attracted much attention due to strong demand for new sensitive materials seeking, which have been insufficiently studied before and show promising properties that could allow to develop more selective and sensitive gas sensors. [32,35-37]

Therefore, current efforts in metal oxides gas sensors are devoted to finding novel sensitive materials at the nanoscale and miniaturized transducers of the chemical stimulus in the air into an electrical signal. Miniaturization brings an increasing number of sensor density on a single chip which is taken positively from the energy consumption point of view and more efficient use of materials.

MOX represent a specific class of materials whose are referred to as functional oxides. Their properties are covering the almost entire aspects of material science and physics including metals, semiconductors, isolators, and many others. Moreover, the structures of metal oxides (MOX) are very diverse that there is an infinite quantity of possible new application and phenomena. Such unique characteristics make MOX one of the most used fundamentals of smart devices because the morphology and structure might be controlled precisely. Therefore, deposition and synthesis of the functional, sensitive material is an important step and crucial part due to the fabrication process. Otherwise, the desired material with the required oxide composition is not achieved. [38-40]

Therefore, metal oxides size down to the nanometer scale demonstrate enhanced sensing properties, and in particular novel classes of nanostructures with high-crystallinity structure provide the opportunity to increase gas sensor performance and functionality dramatically. In this context, the literature shows that structured materials as nanotubes and nanoparticles have been studied intensively. Figure 3 displays the pie chart distribution of 1-D metal oxide nanostructures forms used as sensitive material in gas sensors from 1998 until 2018 in the Web of Science database.
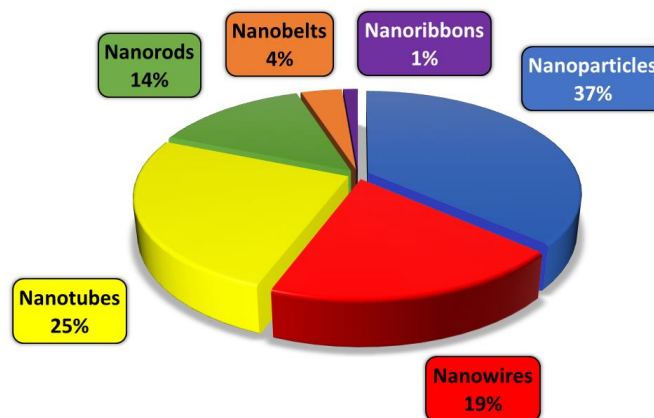
Figure 3. Published research related to 1-D nanostructured forms, performed by using the Web of Science database from 1998 to 2018.

This thesis focusses on the use of semiconducting metal oxides (specifically WO_3 nanowires) in sensor applications with the aim to find the best technological solution to enhance and optimize the functionality of these sensitive materials. Generally speaking, research within this cross-connection of technologies based on new nanostructured surfaces such as composite like nanowires decorated with nanoparticles are the subject of our future intention. Modified materials, especially nanowires combined with nanoparticles (NPs) have shown promising properties which can be useful to ensure improved sensitivity or cross selectivity in gas sensing applications. The thesis goes further by joining classical micro and nanotechnological approaches to integrate this material into a miniaturized sensor device with improved performance.

1.2.1 Working principle summary of metal oxide gas receptor

In terms of principal components of the sensor, MOX gas receptor (sensor) is effectively a gas-sensitive resistor compose of several functional layers, including the active sensing material (i.e., semiconducting material with a high surface-to-bulk ratio), a heating element (metallic heater track, electrically isolated from the active sensing material, to reach optimal operating temperature) and incorporated electrodes in direct contact with the sensing layer (metallic track in contact with the sensing material to measure the actual ongoing electrical changes).

As stated by Brattain and Bardeen more than five decades ago [26], the electrical conductivity of semiconductor depends on the composition of the gas surrounding a relatively shallow area near to the surface where the reaction is taking place. In this region, the gas-solid interactions lead to charge carrier's density changes by physical adsorption and chemical adsorption. Later, Yamazoe and Shimanoe [41] pointed out that there are many other factors which influence the sensing properties of MOX to measured readout information, respectively. These factors depend not only on the proper selection of a MOX and related method and conditions for fabrication but also crystallite size, contacting geometry between crystals, packing thickness or porosity. Furthermore, the sensing properties of MOX might be largely modified with the loading of foreign substances such as sensitizers, which can enhance the efficiency of catalytic reactions.

In principle, the readout values of gas sensor depend on key features such as the ***receptor*** function of the oxide surface that interact with the gas species and the ***transducer*** ability to transfer the chemical information into an analytically useful signal without attenuation of the response recognized by changes in the electrical conductivity (resistivity). An additional feature includes the penetration depth of target gas into the pores of assembled crystals, this feature is known as a ***utility*** factor which predicts how the gas response depends on the physical and chemical properties of the microporous structure and target gas.

Accordingly, to the utility factor mentioned above, this feature depends generally on the nature of the structure of the sensitive material. Utility factor can be taken into account in microporous structures or sensitive layers with micro-grains organization, where the diffusion process into the layer is a part of the gas-solid interaction. However, the utility factor may be neglected, for example, when as sensitive material for the gas sensor is used the nanostructured surface, as it is in the case of nanowires, which have the finest crystallography facets and the major gas sensing processes take place on the surface of MOX material. The exact meaning of each function will be specified into details during the following sections.
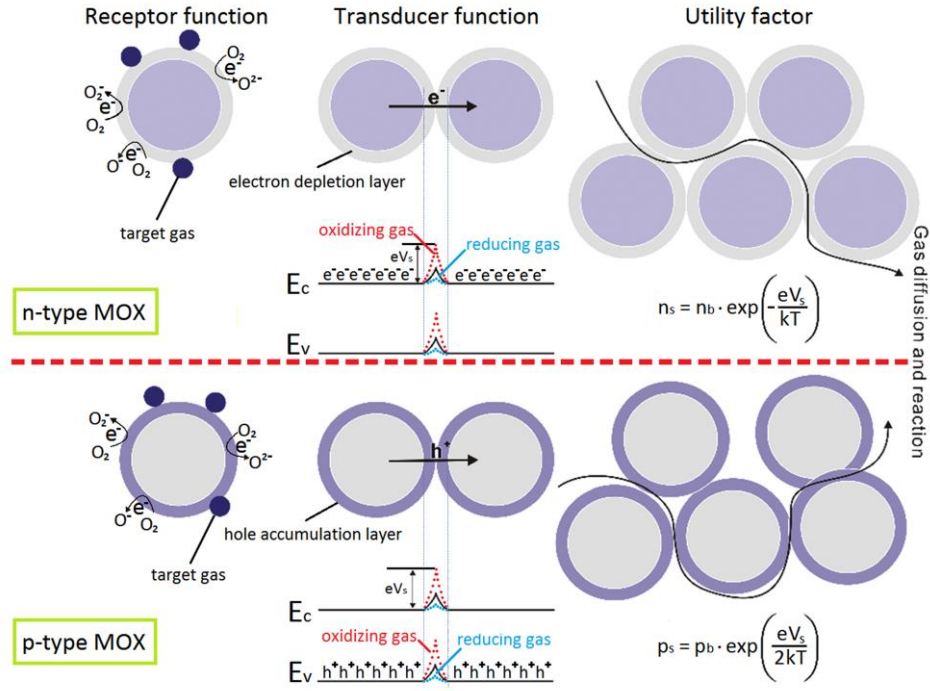
Figure 4. Diagram description of the gas-sensing mechanism and conduction model based on n-type and p-type MOX. Adapted from [42].

Despite facilitating imagining of undergoing processes presented in Figure 4, complex understandings of these phenomena indeed require interdisciplinary knowledge among surface chemistry, semiconductor physics, quantum mechanics and so on. Therefore, in the following section, we will devote our attention to describe the basics of the physical and chemical processes and the mechanism that takes place in metal oxides gas sensors, in order to justify our interest of nanowire-based gas sensors, which will be fabricated and experimentally studied in the subsequent chapters.

1.2.2   Receptor function – gas-solid interactions

As stated previously, the receptor function is the recognition of the target gas species through a physical-chemical reaction taking place at the surface of the sensitive layer and/or inside the layer of the semiconductor. The surface reaction is attributed to the exchange of free electrons between the sensitive material (adsorbent) and adsorbed gas molecules (absorbate), and the reaction in bulk is induced by the exchange between the oxygen ions of the gas and oxygen vacancies in the material. Generally, most of MOXs comprising of unstoichiometric structures as a result of oxygen deficiency causing a large number of oxygen vacancies in the volume, which is a typical property of polycrystalline materials.

When the sensitive layer is exposed to air, the number of the molecules passing from the gaseous phase begin to cover the surface by the species of the gaseous medium. The presence of the molecules raises gas-solid interactions to occur at the grain boundaries of MOX grains. Those interactions may cause several reaction processes, which can take place at the surface, in bulk or both at the same time. It highly depends on actual conditions, as for examples, temperature, binding energy or relative pressure but also on the sensitive material form (e.g.,

compact layer, polycrystalline structure, nanostructure). The reactions induced by gas-solid interaction generally include reduction/oxidation processes of the semiconductor, adsorption of the chemical species directly on the semiconductor and/or adsorption by reaction with surface states associated with preadsorbed ambient oxygen, the electronic transfer of delocalized conduction-band electrons to localized surface states or vice versa. Consequences of these processes for physical-chemical properties of MOXs are shown in Figure 5. [38]
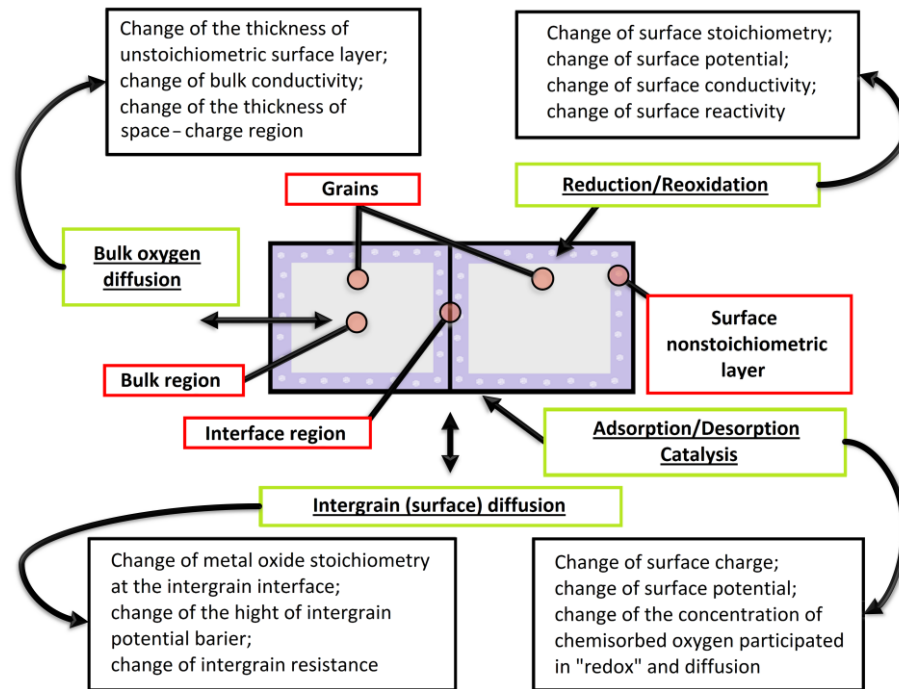
Figure 5. Gas-solid interaction diagram of processes and consequences taking place in polycrystalline MOXs. Adapted from [38].

As it is shown in Figure 5, the gas sensing mechanism can go along together with several types of processes which are fundamentally different from the place of their origin. Taking into account mentioned above, before we start with a description of these processes and their mechanism, the point of our objection has to be set. This thesis devotes to the kind of MOX gas receptors, which could be easily adapted into microelectronic devices compatible with standard silicon technology. Accordingly, there are two types of MOX-based gas sensors, which differ in the region of operating temperatures, and the related detection principle in the given area.

The first, most of the commercial gas sensors (i.e., for detection hydrogen, methane or carbon oxide) operate at relatively higher temperatures about $300 - 500$ °C are based on surface conduction materials considered as "surface sensors" because of the gas-solid interactions modify electron/hole density close to the surface forming chemisorbed oxygen species such as O_2^-, O^- and O^{2-}. Here, the adsorption of oxygen at the surface and the grain boundaries leads to formations of surface oxygen ions and Schottky barriers between the grains. Those oxygen ions extract free electrons from semiconducting material and decrease its conductivity. The oxidation processes evoking different types of adsorption as a function of temperature are expressed as follows:

$$O_{2\,(g)} \rightarrow O_{2\,(ads)} \tag{1.1}$$

$$O_{2\,(ads)} + e^- \rightarrow O_{2\,(ads)}^- \qquad < 100°C \tag{1.2}$$

$$O_{2\,(ads)}^- + e^- \rightarrow 2O_{(ads)}^- \qquad 100 < T < 300°C \tag{1.3}$$

$$O_{(ads)}^- + e^- \rightarrow O_{(lattice)}^{2-} \qquad > 300°C \tag{1.4}$$
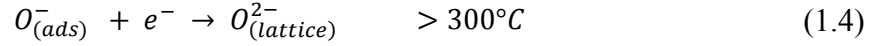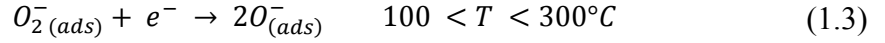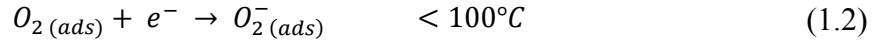
The second category of gas sensors are based on bulk conduction materials so-called "bulk defect sensors," for example, Ga_2O_3 and $SrTiO_3$. They are operating at higher temperatures about $700 - 1100\,°C$, taking advantage of natural nonstoichiometry of semiconducting oxide, where oxygen vacancies diffuse quickly from the interior of the grains to the surface, or from the surface to the interior of the grains. Here, as an example can be a lambda sensor used in an internal combustion engine that controls the air-to-fuel A/F ratio. [43,44]
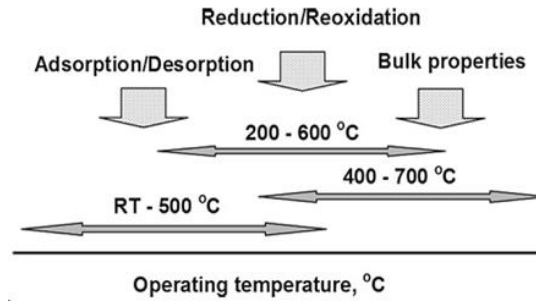
Figure 6. Processes controlling response of high temperature and low-temperature MOX gas sensors [45].

In principle, in the case of surface sensors due to a small constant of bulk oxygen diffusion the chemical composition of the material does not reach an equilibrium state during the time of gas detection. It is a so-called redox mechanism, reduction/reoxidation respectively. At still lower temperatures, the adsorption/desorption processes (chemisorption) can dominate in surface reactions as it is shown in Figure 6 [45,46]. On the contrary, the sensing mechanism of high temperature operating bulk defect sensors is based on bulk oxygen diffusion, when the absorption/desorption mechanism is suppressed. Both sensors have its advantages and disadvantages, but it is necessary to note that bulk defect sensors require, very often, high demands on the robust heating system, which is not in line with semiconductor technologies [38]. Therefore, we will only focus on the mechanisms that apply to the surface sensors, concerning catalytic reactions such as adsorption/desorption.

Adsorption and desorption mechanism

Iwamoto [47] investigated the adsorption mechanism of oxygen on MOXs by using a TPD (Temperature Programmed Desorption) technique about 40 years ago. Adsorption can be described as an increase in the concentration of a dissolved substance at the interface of a condensed and a gaseous phase due to the effect of surface forces. Focusing on the sticking of gas molecules (adsorbate) at a solid surface (adsorbent), we can describe the flux of molecules impinging a surface (ϕ_i), by the Hertz-Knudsen equation [48]:

$$\phi_i = \frac{p}{(2 \cdot \pi \cdot m \cdot k_B \cdot T)^{\frac{1}{2}}} \tag{1.5}$$

where p is the pressure, m the mass of the molecule, k_B the Boltzmann constant and T the temperature. When molecules are in contact with the surface, they can be adsorbed and later desorbed. This sorption process depends on several factors as the actual operational temperature, the binding energy with the surface or pressure. There are two types of adsorption, which differ in the diverse forces that retain the adsorbed molecules on the surface. In other words, the forces that arise between a solid and a foreign molecule can be of different nature. Thus, if the forces of action have a physical nature, there is *physical adsorption* (physisorption) that extends over the entire surface, where the interaction takes place without involving charge transfer between the adsorbent and adsorbate. In principle, it is assumed that the surface of the solid follows an unspecific interaction with the adsorbate, i.e., the interaction takes places on all surface sites with the molecule independently of the gas species, attracting the molecule due to Van der Waals's interactive forces or electrostatic polarization forces as long as the proper pressure and temperature conditions are kept [49]. Van der Waals interactive forces induce a long-range interaction, which attracts the gas molecule for a purpose to minimize its energy. The interaction involves small adsorption energy, up to $0.01 - 0.1$ eV [50]. Due to the low binding energy, the physisorbed particles are highly mobile on the surface and are easily desorbed. This process is reversible, non-activated and non-dissociative, i.e., the gas species remains unmodified, and takes place usually at temperatures close to their boiling point. At higher temperatures, the physisorption can be neglected.

The second type of adsorption deals with the forces adsorption processes that involve a chemical nature. This type of interactions takes place for higher adsorption energies, where electrons are shared between the gas adsorbate and solid adsorbent, which gives rise to *chemical adsorption*. The interaction energy during the chemisorption of adsorbates may reach several eV, approximately one order of magnitude above the characteristic values for physisorption. Although the effectiveness of the chemisorption may be limited to a specific temperature range, chemisorption has no restrictions on temperature, unlike physisorption. For instance, physisorption phenomena prevail due to slow chemisorption mechanism, which barely takes place at low temperatures (e.g., at room temperature). It is known as non-activated chemisorption process. The activated chemisorption requires additional energy (activation energy) in order to pass from physisorbed stated to the chemisorbed state. The additional energy is mostly achieved by raising the temperature. Figure 7 depicts a typical adsorption curve, representing the potential energy of the system as a function of the distance z between the absorbent solid surface and the gas molecule being adsorbed.
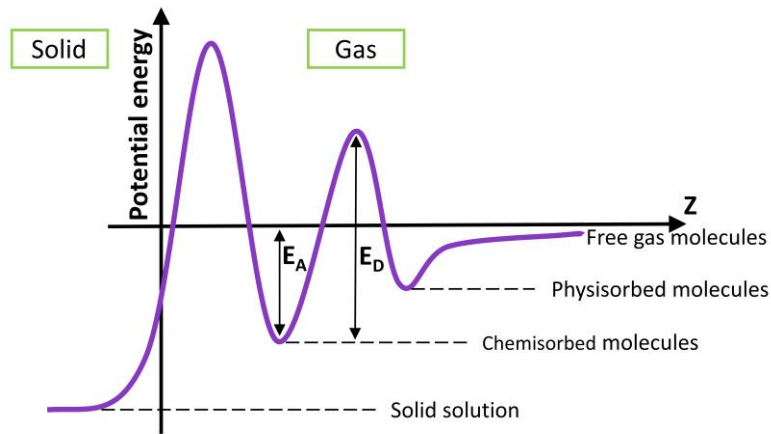
Figure 7. The energy of a gas molecule at a solid-gas interface. E_A: adsorption energy, E_D: desorption energy. Adapted from [51].

If the intersection between physisorption and chemisorption energy get negative values, the process calls as non-activated, when the intersection occurs at positive values it is activated chemisorption, respectively. Usually, chemisorption is activated adsorption, but the presence of activation energy is not necessarily a criterion of chemisorption in some cases, e.g., the adsorption of common gases such as H_2, CO or N_2, where there is no activation energy or the difference E_A-E_D is negligibly small. [49]

In summary, the adsorption of gas molecules on solid surfaces can lead to the following events [52]:

    a. the molecule loses some energy transferring it to the solid and reaching the physical adsorbed state (i.e., translational energy),

    b. the gas molecule is scattered by the surface in an elastic process, without any loss of energy,

    c. the molecule passes, if the energy is high enough, directly to a chemisorbed state if this can be formed near the incidence site, without being trapped in the physically adsorbed state,

    d. within the formation of the chemically adsorbed species, the molecule or its dissociated parts can lose chemical energy (released to the solid, and become localized at the original site) or lose energy and hop diffusively until the excess of energy is dissipated,

    e. the molecule can be physisorbed at the site of the incidence, then it may be chemisorbed, be inelastically scattered back to the gas phase or hop to a neighboring site, where can take place cases a) and b).

Generally speaking, the adsorption and desorption mechanism during gas-solid interactions may be qualitatively described by adsorption isotherm or isobar. The dependence of the adsorbed amount of the gas on its partial pressure at a constant temperature is called as adsorption isotherm. On the contrary, the dependence of the adsorbed amount of the gas on a

certain temperature at constant pressure is adsorption isobar. In the case of adsorption isotherm, at a constant temperature, the adsorbed amount of the gas increases with the pressure or vice versa, the adsorbed amount increases with temperature at constant pressure when we are talking about adsorption isobar, respectively.

While the qualitative description gives us only a general idea of ongoing events, the mechanism of gas-solid interaction is quantitatively better described with several conventional models. For instance, the energy potential of chemisorption can be represented as a Lennard-Jones potential, Buckingham potential or Morse potential [53]. These models allow for the analysis of the gas interactions at the surface of the sensitive layer at constant pressure and different temperature (adsorption isobars). The Lennard-Jones model of activation barriers is most commonly applied between the physisorbed and chemisorbed states.

Figure 8a shows the dependence of the desorption activation energy barrier ΔE_A of neutral molecules on the distance z, which is the distance that needs to be overcome for a physisorbed molecule to reach the chemisorption well. Typical adsorption isobars are depicted in Figure 8b, where the solid lines represent the equilibrium physisorption and a chemisorption isobar, the dashed line represents irreversible chemisorption. Maximum coverage of chemisorbed molecules is obtainable at the temperature T_{max}; below this temperature, the chemisorption is irreversible because the rate of desorption becomes negligible. [54]
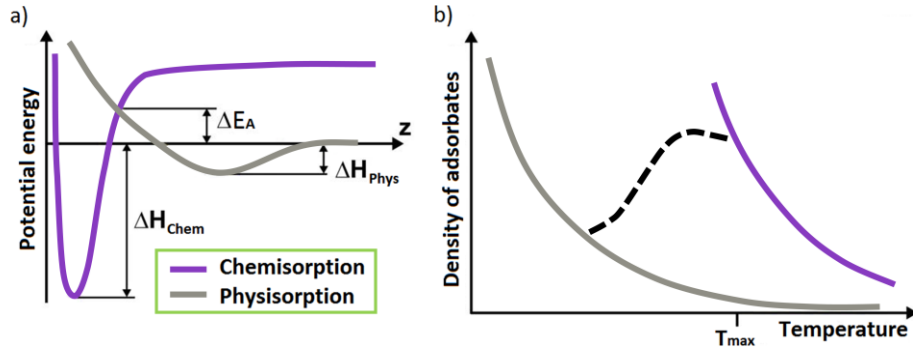
Figure 8. Lennard-Jones model for physisorption and chemisorption of a molecule. Adapted from [54].

Adsorption is always an exothermic reaction; it means that the level of adsorbed quantity at constant pressure will decrease with increasing temperature. At low temperatures, the molecules are captured in a physical state because they cannot overcome the activation barrier ΔE_A, which also corresponds to the maximum coverage at T_{max}.

Accordingly, to the Lennard-Jones activation energy model, the rate of chemisorption $d\Theta/dt$ is given by the difference between the adsorption and desorption rate:

$$\frac{d\Theta}{dt} = k_{ads} \cdot exp\left[-\frac{\Delta E_A}{k_B \cdot T}\right] - k_{des} \cdot \Theta \cdot exp\left\{-\frac{(\Delta E_A + \Delta H_{Chem})}{k_B \cdot T}\right\} \qquad (1.6)$$

where Θ is the proportion of unoccupied surface with chemisorbed particles, k_{ads} and k_{des} are rate constants for adsorption and desorption, ΔE_A is the activation barrier for desorption, and ΔH_{Chem} is the reaction heat of chemisorption [55]. Considering the equilibrium conditions

dH/dt = 0, then the rate of adsorption will be equal to desorption rate, and the coverage density Θ depends on the reaction heat of chemisorption ΔH_{Chem} and can be expressed as:

$$\Theta = \frac{k_{ads}}{k_{des}} \cdot exp\left(-\frac{\Delta H_{Chem}}{k_B \cdot T}\right) \qquad (1.7)$$

Even though Lennard-Jones potential is a simple mathematical model which approximate the interaction between a pair of neutral atoms or molecules, it has to be mentioned that it is largely simplifying and omit some of the phenomena that may occur. Among them the site availability and repulsive forces between the adsorbed molecules, and the dependence of ΔH_{Chem} on the level of surface coverage. Also, the charging heat required for adsorption is not included in the model. In the case of ionosorption, the adsorption heat is related to the acceptor level in the molecule and the electrochemical potential of the electrons (Fermi level) of the solid material. Due to the negative surface charge of a higher energy level in the solid, the energy distance between the acceptor level and Fermi energy is also reduced that leads to the reduction of adsorption heat. Thus, with a subsequent increase of surface coverage, the adsorption heat further decrease. Apart from the adsorption heat, the activation barrier for chemisorption also changes with the concentration of molecules on the surface. [56]

The situation, when the solid surface is covered by more than one pair of a gas molecule is taken into account in other conventional model based on the adsorption of one layer "monolayer" on a solid surface at a constant temperature, for instance in the Langmuir model. In this case, it is assumed that one species of adsorbate, and at most one adsorbate, may be bound at each adsorption site. Accordingly, when the full coverage occurs, one monolayer of particles may be adsorbed. This interaction is also assuming that the binding energy between the adsorbate and adsorbent is constant. Additionally, it is considered that one adsorbate does not interact with the others, i.e., the binding energy is independent of the coverage. Langmuir's isotherm can be expressed as follow [57]:

$$\Theta = \Theta_{Max} \cdot \frac{k_L \cdot p}{1 + k_L \cdot p} \qquad (1.8)$$

where Θ is the amount of adsorbed gas at equilibrium pressure *p*, which is also the ratio of occupied sites related to the total available sites, $k_L = k_{Ads} / k_{Des}$ it is so-called adsorption coefficient of the temperature-dependent adsorption and desorption, Θ_{Max} is the maximum adsorbed amount required to fully occupied surface with monolayer under conditions $p \rightarrow \infty$. Figure 9 depicts the typical dependence of Langmuir isotherm as a function of the density of adsorbates and the gas pressure *p*.
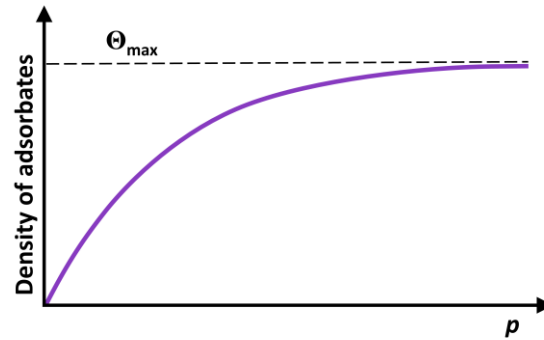
Figure 9. Langmuir isotherm as a function of the gas pressure. Adapted from [57].

As stated, the Langmuir model is not expected to be valid in all cases. For instance, during increasing surface coverage the binding energy or adsorption heat decrease. Hence, the treatment is reasonable only for poor surface coverage, and no surface diffusion is assumed.

Additionally, there are also other models, which take into account other cases, in which more than one layer is attaching the surface of the solid. Brunauer, Emmett, and Teller (BET) isotherm is an extended theory of the Langmuir model describing the physical adsorption of several monolayers. This model is considering other layers upon yet adsorbed layer generated through the action of intermolecular forces between adsorbed molecules and molecules from the gaseous phase.

Further extension of the theory of chemisorption on a semiconductor is included in Wolkenstein's model, which takes into account the strong electronic interactions between the adsorbate and adsorbent. This model is widely accepted in the theory of heterogeneous catalysis and semiconductor surface physics, and it is generally applicable to different kinds of semiconductor gas sensors [50,58]. Accordingly to the Wolkenstein, two forms of chemisorption may be distinguished:

- *Weak chemisorption*, where the chemisorbed particle (considered together with its adsorption center) remains electrically neutral, and the bond between the particle and crystal lattice is established without the participation of a free electron or hole from the crystal lattice.

- *Strong chemisorption*, in which the chemisorbed particle keep in its neighborhood a free electron or hole from the crystal lattice (thus, it is an electrically charged compound) and the free electron or hole plays a leading part in the chemisorption bond. In this sense, it can be defined two types of strong bonds: acceptor bond (n-bond) is one in which a free electron captured by the adsorbed particle participates, donor bond (p-bond) is one in which a hole captured by adsorbed particle participates.

1.2.3 Transducer function – charge transfer and electrical conductivity via grains of MOX

The gas adsorption mechanisms on solid surfaces have been presented briefly in the previous subsection, and the parameters that influence the coverage of a solid surface with gaseous molecules have been described. The mechanisms that give rise to the response to MOX gas sensors will be presented subsequently.

As stated in 1.2.2, the exact definition of the phenomena that evoke the response to gas species impinging the sensitive layer is complex mechanism of chemical and physical interactions. Essentially, trapping of electrons at adsorbed molecules and band bending, which is induced by charged molecules are responsible for a change in conductivity. When a molecule adsorbs at the surface, electrons may be donated to the solid if the highest occupied orbitals lie above the Fermi-level of the solid (donor level) or vice versa, electrons may be donated to the molecule if the lowest-lying unoccupied molecular orbitals of the adsorbate lie below Fermi-level (acceptor level). Then molecular adsorption may result in a net charge at the surface of the sensitive layer and give rise to an electric field that causes a bending of the energy bands in the solid. [59]
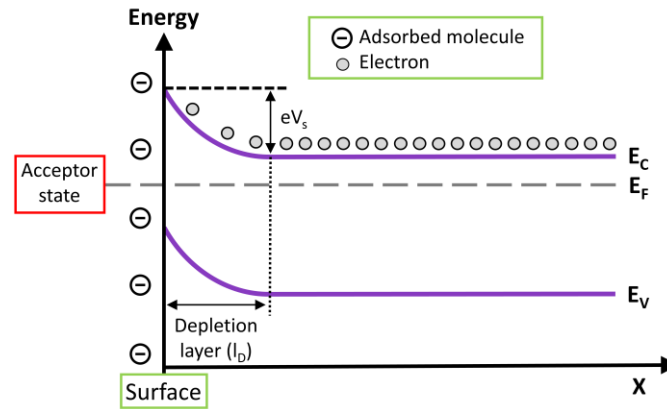
Figure 10. Energy band bending diagram in the near-surface of an n-type MOX. Adapted from [56].

Figure 10 illustrates this event on the example of negatively charges adsorbate. In detail, a negative surface charge caused by adsorbate bends the energy bands upwards, i.e., pushes the Fermi-level into the bandgap of the solid and effectively reducing the charge carrier concentration and resulting in an electron depletion zone [56]. Thus, the depleting electrons causes a positive space charge region that compensates for the negative surface charge. The charge density distribution in the depletion layer can be determined by solving one-dimensional Poisson equation [56]:

$$\rho(z) = e \cdot [p(z) - n(z) + D^+(z) - A^-(z)] = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{d^2 V}{dz^2} \qquad (1.9)$$

where e is the elementary charge, p and n represent the charge carrier density (number of holes and electrons), and D^+ and A^- are the density of singly charged donors and acceptors, ε_r and ε_0 are the dielectric constants of the material and vacuum, V the electrical potential barrier and z is depth from the surface, respectively. Therefore, the charge carrier depletion layer in the

presence of surface charges gives rise to changes in the conductivity of the semiconductor. This change in conductivity $\Delta\sigma$ is frequently used as the signal (response) in gas sensing devices. Thus, the conductivity change considering the band bending eV_s is given by:

$$\Delta\sigma = e \cdot \left[\mu_n \cdot \int n(z) - n_{bulk} dz + \mu_p \int p(z) - p_{bulk} dz \right] \qquad (1.10)$$

where μ_n and μ_p denote the electron and hole mobility.

The height of eV_s and depth of space charge region (known as the charge transport barrier or depth of depletion layer, L_D) of the band bending depend on the surface charge which is determined by the amount and type of adsorbed oxygen (see Figure 10). The depletion layer depth can be expressed as:

$$L_D = \lambda_D \cdot \left(\frac{e \cdot \Delta V}{k_B \cdot T} \right) \qquad (1.11)$$

where λ_D is Debye length, e is the elementary charge, ΔV is the electrical potential barrier, k_B is Boltzmann's constant, and T is absolute temperature. At the same time, the space charge region depends on the Debye length (λ_D), which is a characteristic of the semiconductor material for a particular donor concentration and is described as:

$$\lambda_D = \sqrt{ \frac{\varepsilon_0 \cdot \varepsilon_r \cdot k_B \cdot T}{e^2 \cdot n_d} } \qquad (1.12)$$

where ε_r and ε_0 are the dielectric constants of the material in a vacuum, T the operating temperature, and n_d the carrier concentration which corresponds to the donor concentration assuming full ionization.

Therefore, the height of the potential barrier is given by:

$$\Delta V = \frac{Q_S^2}{2 \cdot \varepsilon_0 \cdot \varepsilon_r \cdot n_d} \qquad (1.13)$$

where Q_S is a surface charge.

Even though the surface conductivity as a product of gas-solid interactions, is one of the crucial parameters of transducer function, it is not only the surface conductivity, which must be taken into account, as the electrical resistance of the material also includes the bulk conductivity. Therefore, the surface-to-volume ratio and the crystalline quality of the adsorbent are also important parameters to take into the account. In the following paragraphs, we will focus our attention on various features of the sensing element such as the morphology and the correlation with the mechanisms taking place during gas-solid interactions, since this relationship influences the sensor response (i.e., changes in the sensor conductivity).

1.2.3.1 Influencing effect of oxidizing and reducing gas on the depletion layer

As stated above, during the chemisorption process it is formed a surface depletion layer (L_D) at the MOX semiconductor. Focusing on n-type semiconductors, which have an electron-

depleted surface, due to adsorption of atmospheric oxygen as O^{2-} or O^- species (Figure 11a) which tie up electronic carriers, the surface is highly gas sensitive. After oxidizing or reducing gases come into contact with the surface, it may result in two reactions of the depletion layer:

- when an *oxidizing gas* such as NO_2 reacts with the surface, the depth of the depletion layer can be increased (Figure 11b),

- when a *reducing gas* such as CO reacts with the surface, the depth of the depletion layer can be decreased by the removing of chemisorbed oxygen as it is depicted in Figure 11c.
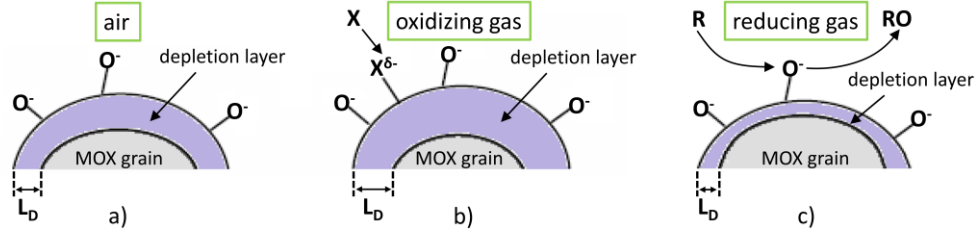
Figure 11. Schematic illustration of gas influence on the depletion layer of n-type MOX grain: a) with dry air, b) with an oxidizing gas and c) with reducing gas.

Detailed illustration of the influence of reducing gas on energy potential levels is shown in Figure 12. During the exposure of an n-type semiconductor to a reducing gas, the semiconductor generates a number of free electrons which cause an increase of conductivity along the conductive channel of a crystalline semiconductor. Additionally, the change in potential energy level between two or more (neighbor) grains also results in a change in the conductivity throughout the entire sensitive layer and may contribute to the measurable signal and the sensor response. When the gas is removed, the surface is again depleted of carriers as the oxygen is again adsorbed on the surface. [60]
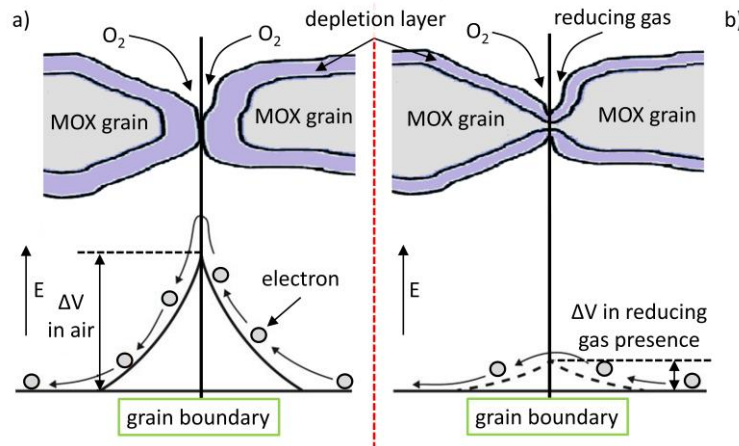
Figure 12. Structural and band illustration of two n-type grains at grain boundaries: a) influence of dry air and b) influence of reducing gas.

On the contrary, when an oxidizing gas gets into contact with an n-type semiconductor and participates in the reaction, the opposite effect occurs, thus, the potential barrier level increase due to the adsorption of more oxygen molecules (from the oxidizing gas, e.g., NO_2) on the surface and conductivity in the channel decreases as a reason of adsorbed NO_2 molecules

with higher electric charge. This effect is opposite in the p-type semiconductor, and thus the reducing gas decreases conductivity, while the oxidizing gas increases it.

Figure 13 gives an overview of the various conductivity mechanism and changes in conduction band induced by chemisorption of oxygen and CO on basic structures of MOX semiconductors. The equivalent electrical models used to represent individual structure are also introduced.
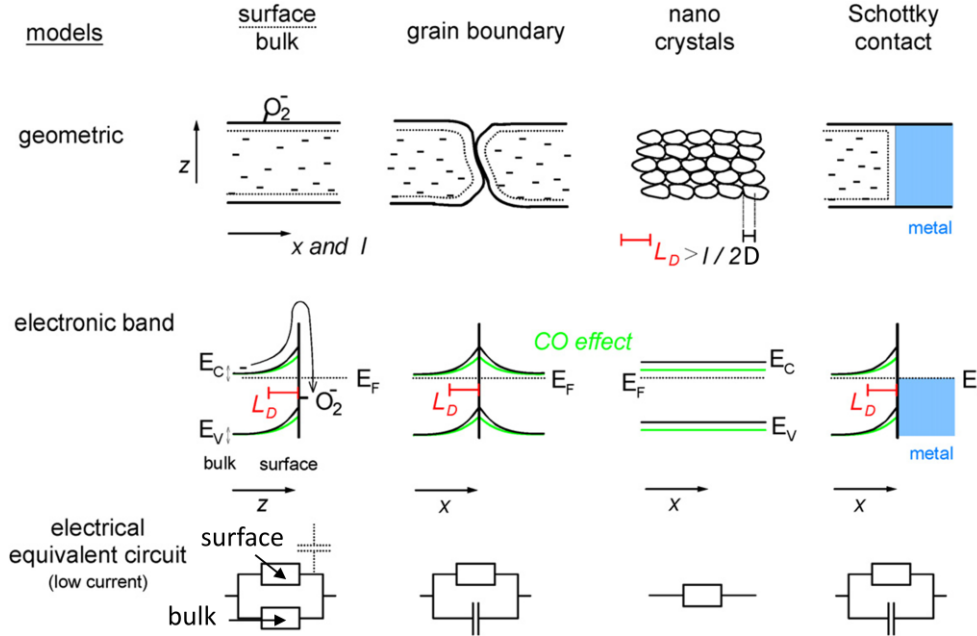

Figure 13. Different conduction mechanism and changes upon O_2 and CO exposure to a sensing layer in the overview [61].

1.2.4 Effect of grain size and crystalline quality

At present, considering all kinds of sensing materials, polycrystalline and nanocrystalline materials, and in special cases, monocrystalline materials, have found the greatest application in gas sensing due to such properties as low-cost design, enough developed surface, structural and electro-physical stability, among others. As it is known, a specific surface area is sharply increased with the decrease of grain size [38]. In polycrystalline materials, not only the surface is exposed to the gaseous phase, but also the grain boundaries, which are depleted of carriers at their surface due to the grain-grain barriers. Therefore, the microstructure of these aggregates is considered to be very important for the transducer function.

Figure 14 illustrates a few n-type MOX semiconductor grains and oxygen molecules adsorbed on their surface. During the chemisorption process, oxygen has captured electrons from the material forming a depletion layer. The thickness of the depletion layer L_D is relatively small compared with the grain diameter D; in most traditional MOX semiconductors about tens of nanometers. Then, two charge transport barriers with the height of energy band bending eV_s are formed as seen in Figure 14. This gives rise to the higher resistance values at the intergranular contact points. [24]
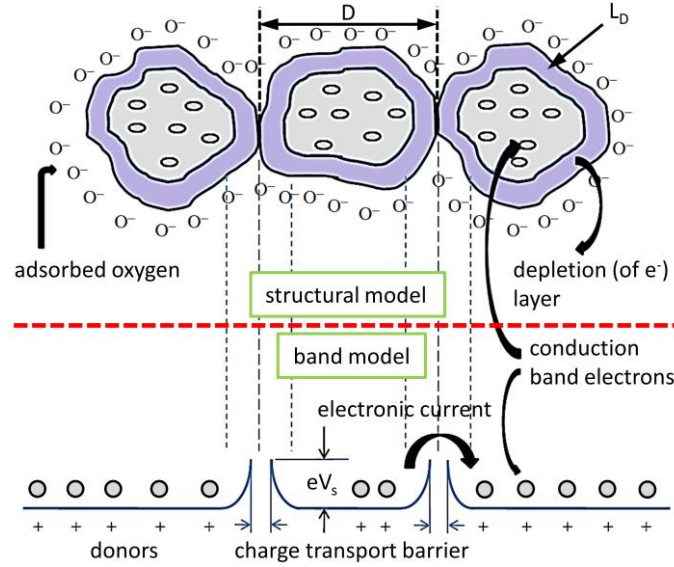
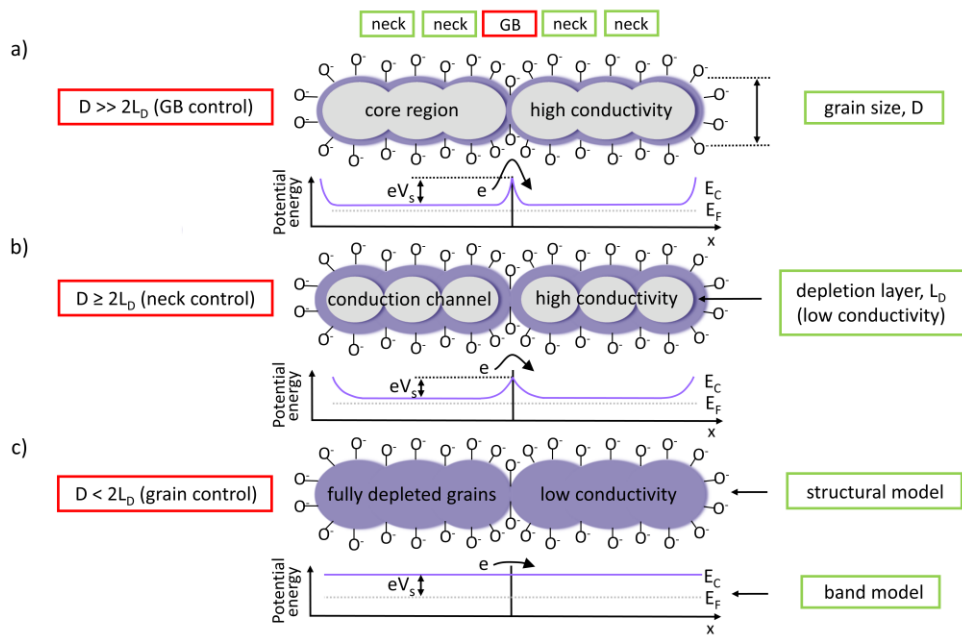**Figure 14. Structural and band model of MOX grains. Adapted from [62].**

In contrast to monocrystalline materials and according to the literature [63,64], the effect of the microstructure in polycrystalline gas-sensitive materials can be described in several model formulations. The general idea, as depicted in Figure 14, shows the polycrystalline material create multiple charge transport barriers, in which each grain, leads to significant changes to the effective charge carrier concentration and the electrical conductivity of the sensing material as a result of the amplifying effect of chemisorbed molecules (e.g., adsorbed oxygen from the air, as in Figure 14). Other formulations describes the effect of the microstructure as a network of barriers with characteristics of the network changing as a consequence of the change in barrier height caused by gas-solid interactions [65], other formulations (widely used as an interpretation of grain size effects in MOX gas sensors) state that the sensor consists of partially sintered crystallites, which are connected to their neighbors by necks or grain boundaries [64]. This last formulation is known as Neck-grain model and is represented by three case formulations that take into account the relationship between the grain size D and length of the depletion layer L_D produced around the surface of the crystallites due to the reaction induced by chemisorbed molecules. These three cases illustrated in Figure 15 will be described subsequently [64]:

a) *GB (Grain Boundaries) control case*, for large grains, i.e., when $D >> 2L_D$, most of the volume of the crystallite is unaffected by the surface interactions with the gas phase. In this case, the predominant effect of the ambient gas atmosphere on the sensor conductivity is introduced via GB barriers for intercrystallite charge transport from one grain (agglomerate) to another, as shown in Figure 15a. Therefore, the conductivity σ depends exponentially on the barrier height eV_s.

$$\sigma \approx exp\left(-\frac{eV_S}{k_B \cdot T}\right) \tag{1.14}$$

Then, for large grains $D >> 2L_D$ the gas sensing mechanism is controlled by the GB barriers. Furthermore, the GB barriers are independent of the grain size, and therefore the sensitivity is independent of D.

b) *Neck control case*, i.e., when $D \geq 2L_D$, as the grain size decreases the depletion region spreads more in-depth into the grains and consequently the core region, which is relatively more conductive comparing to the depletion region adjacent to the surface, becomes smaller. When D approaches to $2L_D$, or it is slightly larger, the depletion region that surrounds each neck forms a compressed conduction channel within each aggregate, as is illustrated in Figure 15b. Therefore the conductivity depends on not only the GB barriers, but also the cross-section area of the channels, which is proportional to $(X - L_D)^2$. Where X is the neck diameter roughly proportional to D and well approximated to $X \approx 0.8D$, as reported by [66,67]. Subsequently, the conductivity is a function of the radio X / L_D (or D / L_D). In summary, the current constriction effect adds up to the effect of the GB barriers. Thus, the gas sensitivity is enhanced concerning the case (a). Moreover, the sensitivity to gases becomes grain size-dependent on grain size, and it increases when D decreases.

c) *Grain control case*, i.e., when $D < 2L_D$ occurs, the depletion layer extends throughout the whole grain, and the crystallites are almost fully depleted of mobile charge carriers. Therefore the conductivity decreases steeply since the conduction channels between the grains are vanished. The energy bands are almost flat throughout the whole structure of the interconnected grains, and since there are no significant barriers for intercrystallite charge transport, the conductivity is mostly controlled by the intercrystallites or grains.

Figure 15. Structural and band model of the effect of the crystallite size on the sensitivity of MOX gas sensor: a) GB control $D >> 2L_D$, (b) neck control $D \geq L_D$, (c) grain control $D < L_D$.

Concerning the neck control case stated above, there are also different possible types of necks, which influence the conductivity of the channel. Figure 16 illustrates the role of necks in the conductivity of polycrystalline MOX and potential distribution across the neck. Three pairs of the neck may be defined regarding the neck form:

- *Narrow-Broad neck*, where the total resistivity via grain conductive channel of the narrow neck is higher than the resistivity of the broad neck, $R_{narrow} > R_{broad}$;

- *Long-Short neck*, where the total resistivity via grain conductive channel of the long neck is higher than the resistivity of the short neck, $R_{long} > R_{short}$;

- *Closed-Opened neck*, where the total resistivity via grain conductive channel of the closed neck is higher than the resistivity of the opened neck $R_{closed} >> R_{opened}$.

The different shape of the neck between grains is mostly defined during the fabrication (synthesis) process, where various parameters play a significant role throughout structure forming, for example, a deposition technique, deposition rate, pressure and so forth. However, a significant step giving rise to the formation of neck-like polycrystalline structures is the extent of the sintering or annealing of the material. Majority of polycrystalline structures used for gas sensing require subsequent post-processing. Otherwise, unsintered polycrystalline structures are pressure and temperature-sensitive leading to quite unstable behavior during the aging time. [62]
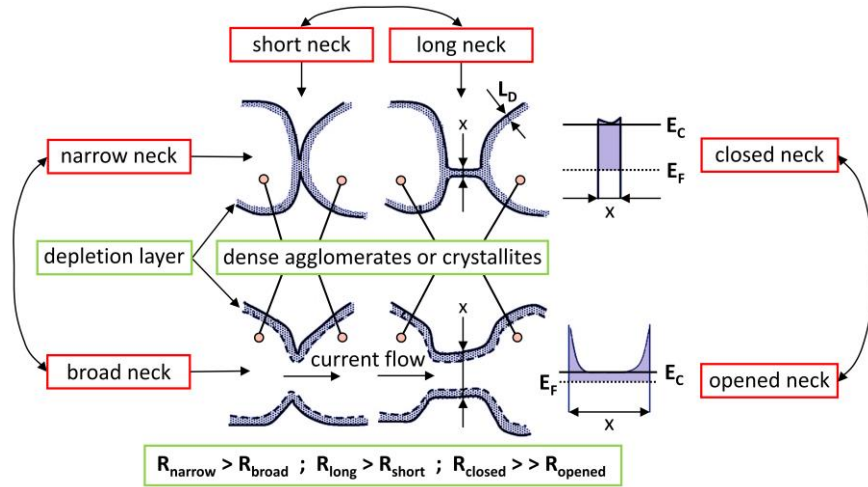

Figure 16. A structural illustration of various neck-like types of polycrystalline MOX. Adapted from [38].

Furthermore, in the early 1990s, Yamazoe, and co-workers [67,68] presented systematic investigations to answer the general question of how nanocrystalline metal oxides increase the sensitivity? More precisely, what happens when D decreases to be comparable to $2L_D$ (i.e. when the depletion layer extends throughout the whole grain $D < 2L_D$)? Figure 17 depicts the influence of grain size on sensor sensitivity under exposure to air (R_a) and a target gas (R_g). It may be seen that a decrease in D down to 6 nm causes a gradual decrease of R_a and R_g, while a further decrease of grain size evokes rapid increase of R_a and R_g. This characteristic changes in behavior at a critical size ($D = 6\ nm$) are associated with changes of thickness proportion between depletion layer L_D and grain size D. When $D > 2L_D$, the grain boundary potential of

the depletion layer is kept quite constant with change in *D*. *T*herefore the electrical resistance becomes *D* independent. As a result of such behavior, the gas response (R_a / R_g) shows characteristic dependence on grain size *D* up to ~ 10 nm, when the response decreases significantly and then becomes almost independent of *D* above 15 nm.
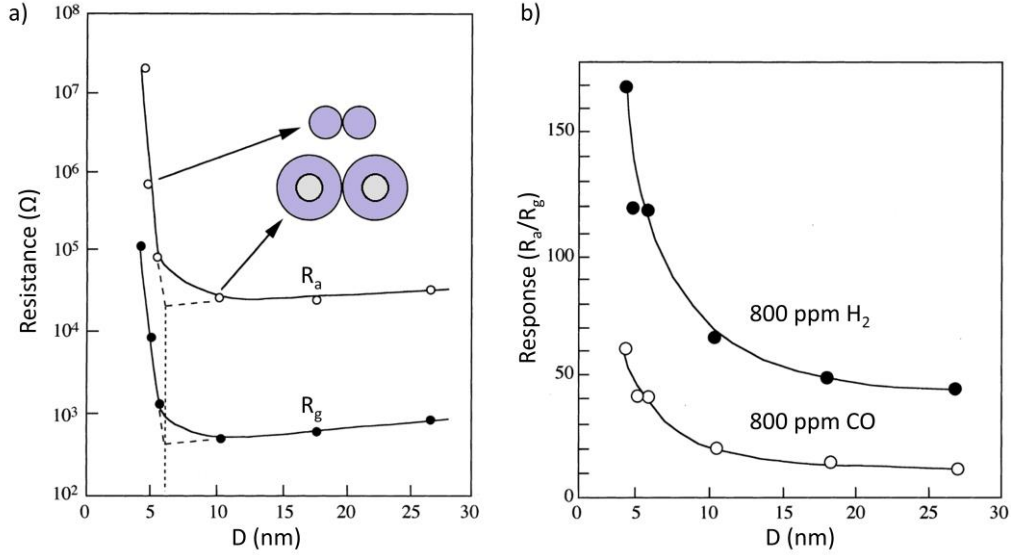
Figure 17. Influence of grain size: a) on electric resistance in Ra and Rg for 800 ppm of H₂, b) on response to 800 ppm H₂ and 800 ppm CO in Air. Both measured at 300 °C. Adapted from [69].

At last, the literature shows that nanosized crystallites lead to significant changes in the effective carrier concentration and the electrical conductivity (or resistivity), even for a very small variation in the trapped charge density from target gas (1 ppm). From this statement, it is evident that the amplification power of the sensor's transducer function, which transforms the interactions between the sensor and the target gas into an electrical signal, is proportional to the surface-to-volume ratio of the sensitive material. This conclusion has had important implications on the design of MOX gas sensors and is still a well-used strategy for optimizing the gas sensitivity, in MOXs. [67]
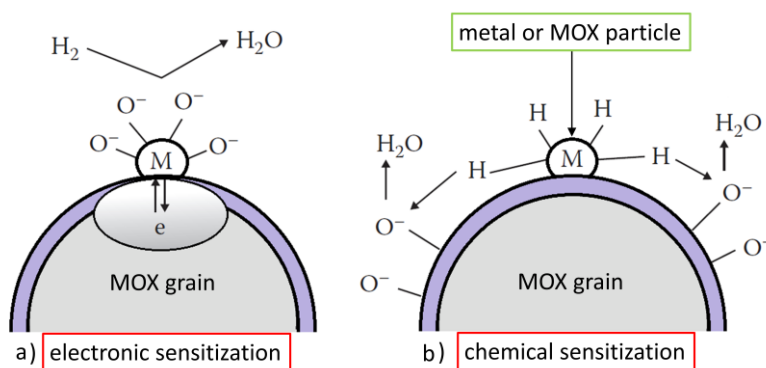
1.2.5 Effect of surface functionalization by noble metals or MOX particles

As mentioned in 1.2.2, gas-solid interaction begins with receptor function, where chemisorption plays the leading role; in other words, adsorption of the target gas species over the surface of the sensitive material. If the sensitive layer, for instance, a MOX semiconductor, has a composition of pristine material, the adsorbed oxygen is used for the oxidation reaction causing changes in depletion layer depth L_D which, in turn, results in a change of conductivity in the conduction channel or the measurable electrical resistance change throughout the gas sensitive material. However, often pristine MOX surfaces are not able to comply with all the demands of a perfect chemiresistor gas sensor due to their poor surface activity. To overcome this natural limitation, various types of foreign materials (intentional impurities, so-called as high-effective catalysts), are deposited on the surface of pristine base materials. This type of functionalization can be seen as a kind of "doping" process, with which, in principle, we add catalytically active sites to the surface of the base material. [69]

In recent years, scientific research [70,71] has shown that surface functionalization by noble metals and/or MOX particles (such as Pt, Au, Pd, Ag, CeO, ZnO, etc.) has a profound impact on the sensor performance. Ideally, this "doping/loading" process improves sensor performance in order to increase the sensitivity, favoring the selective interaction with the target analyte and thus increasing the sensitivity and selectivity, and decreasing the response and recovery time. A reduction of the working temperature may also accompany it, as well as a positive influence on the long-term stability of the sensor. [72]

Figure 18 depicts the possible sensing mechanisms at surface modified materials, which are connected with a chemical and /or electronic sensitization. The electronic sensitization, shown in Figure 18a proposes the formation of the depletion region around the "doping" noble metal or MOX nanoparticles (NPs). The "doping" NP in the oxidized state acts as a strong acceptor of electrons from the MOX grain (pristine base material), inducing a layer strongly depletive of electrons in the MOX grain near the interface. This difference between the oxidized and reduced state is often significant and brings about a large increase in response to the target gas.

The chemical sensitization illustrated in Figure 18b, is the mechanism, in which the atomic product of catalytic reaction (dissociated molecular oxygen caused by the doping catalytic NPs) diffuses to the pristine sensitive layer, resulting in increase of the quantity of oxygen that can repopulate vacancies at the pristine layer and increase the rate at which this repopulation appears. Accordingly to this mechanism, a higher and faster degree of electron withdrawal is present in the reaction. In the catalysis literature, this mechanism is well-established and known as "spillover effect". [28,73]


Figure 18. Mechanism of surface functionalization of MOX by noble metal or MOX additives: a) chemical sensitization and b) electronic sensitization. Adapted from [69].

In the literature, there have been many reports for enhancement of sensitivity by the surface modification or 'doping' of pristine MOXs with noble metals [74,75]. As was stated, these additives can influence certain physical and chemical properties, for example, increase the electron exchange rate, stabilize a particular valence state, modify the catalytic activity of pristine oxide, stabilize the catalyst against reduction and so forth [76]. However, the real situation is more complicated and searching for sensitive material with appropriated properties still requires an entirely empirical approach. Figure 19 shows a multitude of parameters, which

may be altered by introducing a "doping" element to a pristine MOX. Even a small amount of the element added during the preparation process can affect the electronic properties, the morphology of the material as well as the total catalytic activity. [77]
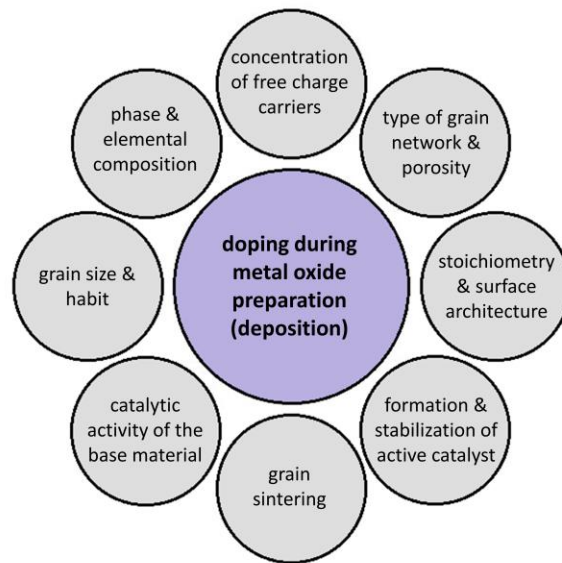
Figure 19. Influencing factors during the preparation of MOX with additional doping elements on its final properties. Adapted from [76].

Several methods have been used for introducing noble metals or MOX additives to gas-sensitive materials, including physical techniques such as sputtering or thermal evaporation, or chemical coatings methods as impregnation, sol-gel and so forth. Indeed, the use of different methods may result in various morphologies of the final structure. For example, different doping states can be obtained by a sol-gel method, where the final structure can be composed of a mixture of noble metals and MOX particles. On the contrary, structures in the form of thin films with pristine material surrounded by noble metals particles are possibly achieved by sputtering or thermal evaporation techniques, where most of the time, the deposition cycle is accompanied by two phases growing process [78]. In this case, the first cycle is realized to grow the pristine MOX layer and the second cycle to incorporate the noble metals or another MOX as additives. The results of both chemical or physical techniques are evaluated accordingly to control parameters such as composition, size as well as their dispersion on and/or into the MOX surface.

Yamazoe et al. [69] demonstrated in their work that the properties of catalytically active NPs, concretely particle size, can effectively control the temperature of operation as well as the efficiency of a catalytic reaction in relation with sensor sensitivity. As shown in Figure 20, the application of different loading methods for the addition of MOX NPs results in significant sensor response shifts of the gas response $\Delta R_a / \Delta R_g$ toward low operating temperatures. In contrast, unloaded pristine SnO_2, PdO loaded SnO_2 layer prepared by chemical fixation of $(PdCl_4)^{2-}$ followed by reduction, as shown in Figure 20 (method 3), the sensor response is several times higher.
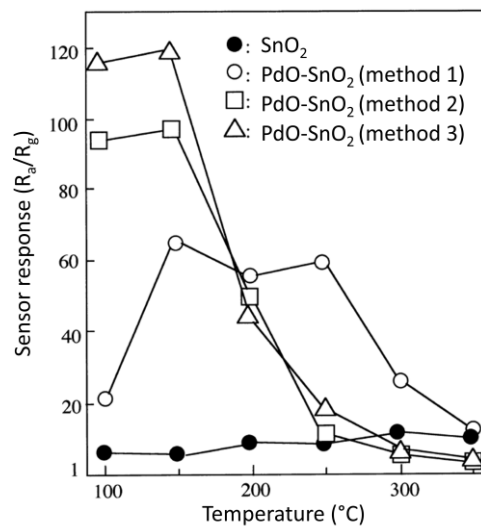
Figure 20. Effect of different loading methods on sensor response to 192 ppm H₂. Loading methods: (1) impregnation of PdCl₂ and reduction, (2) adsorption of colloidal Pd, (3) chemical fixation of (PdCl₄)²⁻ and reduction [79].

Additionally, regarding the size of the catalyst, many works pointed out that the problem with the lack of selectivity of gas sensor can be solved by the elimination of the NP size added onto the MOX matrix. For example, surface functionalization of the low-dimensional MOX, the selectivity toward a target gas may be radically increased, particularly, when the size of the noble metal or MOX NPs is lower than 5 nm. [79] Furthermore, the nanocrystallites shape-control provides energetically different adsorption sites for the analytes on the different crystal facets enhancing the sensitivity of the sensor to various gases as well as its selectivity. [77]

Another possible approach to increase the detection ability of gas sensors is the use of one-dimensional nanostructures such as wires, tubes, rods, and belts. These nanostructures are valuable candidates for the realization of the next generation of sensors. Previously, various works on anisotropic nanomaterials and their compounds demonstrated their high sensitivity and selectivity toward several gaseous species. Due to the novel properties, of structured materials, this area has become a new research field on its own, offering the basis for the investigation of new phenomena in physics, chemistry and material science. This dissertation focuses on these types of structures that might contribute to the improvement of gas sensors. The most promising nanostructures according to its application and the possibility to integrate them into the electronic architecture to build a whole sensing device, will be presented in the following sections.

1.3 *Nanosensors based on one-dimensional nanowires structures*

As stated, with the advent of nanotechnologies, one-dimensional materials (1D) MOX nanostructures have called attention as a new generation of functional materials exhibiting several advantages not only for gas sensors but also for other sensing technologies. Last years it appeared a prospective trend of research which is connected with taking into account structural peculiarities of gas sensitive material. 1D materials such as nanobelts, nanorods or nanowires are the basis of these researches, and they are used as subjects for further fundamental studies, but also the realization of functional devices with a focus on low cost, small size, and low power consumption. All of the latter are materials with promising properties for gas sensing, for example, the dimensions close to the range of biological and chemical species, fast diffusion kinetics and so forth. On the contrary, for the realization of next-generation gas sensors with excellent properties and functionality will be further discussed only one 1D material, which, based on facts noticed in following sections, is potentially suitable candidate meeting the specified parameters. Hereafter, it will be explained why is it so.

Generally speaking, nanowires poses a high surface-to-volume ratio and the ability to achieve great length during their synthesis process. Besides they can be integrated relatively easily into microelectronic devices. Hence, 1D nanostructures like NWs are seen as a favorable candidate for future sensors. Nowadays, there is an intensive search for novel NW materials with metallic or semiconducting properties, or a combination of both properties, capable of realizing single-molecule detection with superior sensing performance [38,80]. This continuing effort in the development of such miniaturized sensors which are expected to be cheaper, faster, more sensitive, selective and more stable compared with conventional "state of the art" sensors lead to new development techniques, which push the gas sensor field toward "nanosensors". Such downsizing of sensing elements not only makes sensors cheaper and more economical but also improves the sensor performance opening, therefore, new technological perspectives. [81]

Nanosensor is the device using nanosized components as the active sensing material. Those nanosized components are in the order of tens to hundreds of nanometers. Nanowires have been defined as wires with at least one spatial in the range of $1 - 100$ nm [82,83]. Nanosensors based on these structures and dimensions show a variety of impressive properties. Although the basic mechanism for gas sensing remains the same (i.e., adsorption and desorption of the molecules) compared to the conventional sensors based on polycrystalline materials, they are characteristic by their high surface-to-volume ratio, which is mandatory for fast reaction kinetics and provides more surface area for both chemical and physical interactions.

Moreover, there are other advantages that make nanowire structures excellent building-blocks for micro/nanoscale gas sensors, compared to their bulk counterparts [80], for instance:

- dimensions comparable to the extension of the surface charge region,
- relatively simple preparation methods allowing large-scale production,

- superior stability due to a high crystallinity of the NWs,

- ultrahigh sensitivity, improved selectivity, and the potential for the integration of addressable arrays on a mass-production scale,

- high-density loading of a target-specific receptor species and a catalyst deposition over the surface for promotion or inhibition of specific reactions,

- better thermo-dynamic stability comparing to nanograins, which promotes the stable operation of the gas sensors at a higher temperature, and [38],

- work at lower operating temperatures due to the minimal amounts of gas that influence the change of electrical characteristic.

To reach all these advantages, an essential goal in current research and development of NWs based sensors is connected with the synthesis and fabrication processes of these functional nanomaterials.

1.3.1 Nanowires synthesis and device fabrication approaches

Nowadays, there are many diverse methods to synthesize NWs, but commonly, these methods are classified into two categories the first based on top-down approaches and the second on bottom-up approaches. Figure 21 depicts the main steps involved in these approaches.
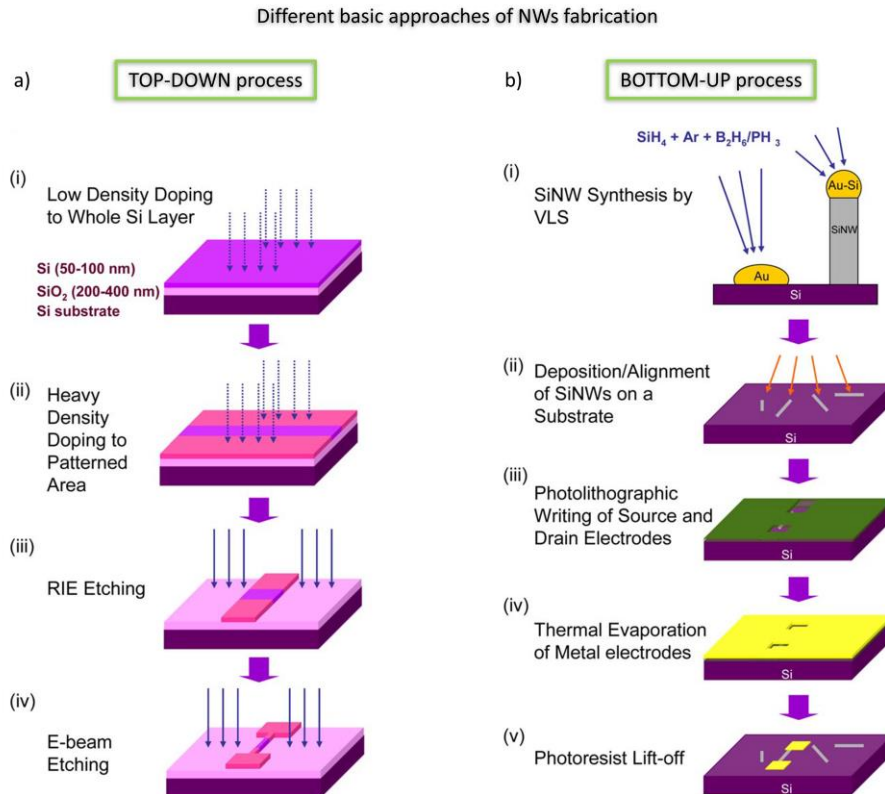

Figure 21. A schematic illustration of typical methods for silicon NWs fabrication depicted step by step: a) TOP-DOWN process, b) BOTTOM-UP process. Adapted from [84].

- *Top-down process* – compared to the ''bottom-up'' method, this approach is more complex because the process relies on high-resolution lithography. For this reason, electron-beam lithography is necessary. Although the ''top-down'' approach needs many expensive instruments, it has advantages of using standard semiconductor techniques to precisely design a desired device-array pattern eliminating the redeposition and positioning of NWs. Another challenge to the ''top-down'' method is that the minimum width of the produced NWs is around 100 nm. To overcome this barrier, single NWs of the triangular section were fabricated to reach a thinner transverse dimension ($\leq$ 20 nm) with a length of several micrometers. [84]

- *Bottom-up process* – compared to the ''top-down'' method, this approach has the advantages of synthesizing NWs of high crystallinity, designated dopant density, and easily controlled diameters in a cost-effective preparation. However, without an intentional alignment for the randomly oriented NWs on the substrate, the device fabrication would suffer from inefficient fabrication yields, which could also limit their development in the industrial applications. Therefore, the success of producing high-quality NW devices requires the development of a uniform assembly of the ''bottom-up'' synthesized NWs on the support substrates. [84]

The first mentioned approach (top-down) permits the preparation of well-organized structures based on standard microfabrication technologies, [85,86] but it has restrictions for large-scale production yet due to the severe drawback, which should be taken into account. As was described previously, for the preparation of 1D nanostructures by the top-down process are using standard semiconductor technologies such as lithography and etching procedures. Among them, for the growing of the sensitive thin-layers serving as an sensing elements in gas sensing, are used various techniques, mostly based on chemical vapor deposition (CVD) or physical vapor deposition (PVD), which not always allow synthesis of highly sensitive materials with properties of single-crystalline materials with specific facets, as those synthesized during crystal growth by bottom-up process, respectively. In this context, regarding the gas sensing principle of 1D nanowires, which will be described in details lately, the gas sensing properties of this sensors to the analytes can be reduced by disrupting the surface uniformity of these sensitive elements as a result of etching procedures and other following operations.

The second approach (bottom-up) consists of self-assembly of molecular building blocks, synthesis via vapor-phase transport, solution-based techniques, or template growth. In general, there are two main strategies to assemble the NWs over the electrode gap creates the electrical interconnection, namely, direct growth of NWs onto a substrate, or transfer with alignment methods (direct assembly of NWs). First mentioned, *direct growth methods*, include growth of vertically or horizontally aligned NW arrays, and also integration by bridging method [87-89]. Among leading *transfer and alignment methods* belongs, for instance, alignment by interactions with chemically patterned surfaces, Langmuir-Blodgett alignment technique, or electric and magnetic fields assisted orientation (alignment) [90]. The latter technique is

considered as the most promising for large-scale fabrication of selective gas sensors because it offers precise placement and ability to line-up the NWs in parallel. Additionally, the process for the alignment of NWs in a liquid medium under electric field is called *dielectrophoresis (DEP)* assembly of nanowires, which is described further in 2.8.3.

In this context, the bottom-up method is advantageous as it provides precise control of the shape and morphology, high purity, and crystallinity, together with low production cost, as compared to the top-down method. The deficiency of this technique is the integration process in planar substrates needed for the exploitation of their useful properties.

1.3.2 Effect of nanocrystals morphology on gas sensing properties

Over the past decades, the main objectives of scientific efforts have been focused on improving the sensitivity and selectivity of gas sensors by several methods. Significant progress has been made in the field of MOX grain size reduction, modification of the surface of pristine MOXs by noble metals and/or the improvement of fabrication techniques. However, the application of these innovative techniques has not recorded much success and usage in massive industrial production yet. On the contrary, most of the commercial MOX gas sensor devices have been using still conventional technologies, i.e., based on thick-film technology. [38]

In recent years, a few research related to material science and catalysis of nanocrystalline materials pointed out notable findings that a catalyst reactivity becomes more effective not just when its size goes down, what as stated can be envisaged from the increased numbers of surface atoms, but also it might be related to the shapes of the particles. The surface atomic structure is one of the important factors that influence the application of nanomaterials. The parameters such as crystal structure, including crystallinity, terminating facets and anisotropy strongly affect the properties of nanocatalysts. Hence, morphological control of nanocrystals provides a way to tailor the physical and chemical properties of these nanomaterials. [91,92]

Generally speaking, gas sensing by MOX semiconductors is based on the oxidation-reduction reaction of the detected analytes occurring on the surface, which leads to an unpredictable change in conductance of the sensor. For this reason, the gas-sensing ability of MOX semiconductors is in theory susceptible to the crystal faces of the sensing materials. Hence, MOX nanocrystals with particularly exposed crystal planes, from the viewpoint of chemical activity, can be good sensing materials. Lately, the exposed facets of a nanocrystal have been found to offer greater versatility than size, shape and other parameters in tuning the catalytic efficiency of the nanocrystal [93]. In this sense, facets are the flat faces on particular geometric shapes. Generally, the shape of nanocrystal has a strong association with the exposed facet, taking into account the surface structures, the fractions of atoms at corners and edges. [91,94]

With the decreasing of the crystal size, more surface is exposed, thus the fraction of atoms in the grain boundary increases, and the grain boundaries contain a high density of defects like vacancies and dangling bonds, which can play a significant role in the transport properties of

electrons of nanomaterials. Accordingly, a large number of dangling bonds or unsatisfying bonds is present on the surface of the material as a result of which the coordination number becomes different from that of the bulk portion. This may increase the active sensing area and therefore, greatly enhance sensitivity. [95]

Furthermore, faceted nanomaterials are of two types, low-index and high-index faceted. High-index facets have high densities of low-coordinated atoms, steps, ledges, kinks, and dangling bonds usually exhibit much higher chemical activity due to more active catalytic sites [94]. Figure 22 depicts the influence of different faceted SnO_2 nanocrystals on the gas sensing properties. In this context, it is evident that the surface with more dangling bonds (221) facet is highly active for adsorption of ionized oxygen species than the surface of (110) facet. It is proof that high-energy surfaces usually exhibit greater reactivity than those with low-energy surfaces.
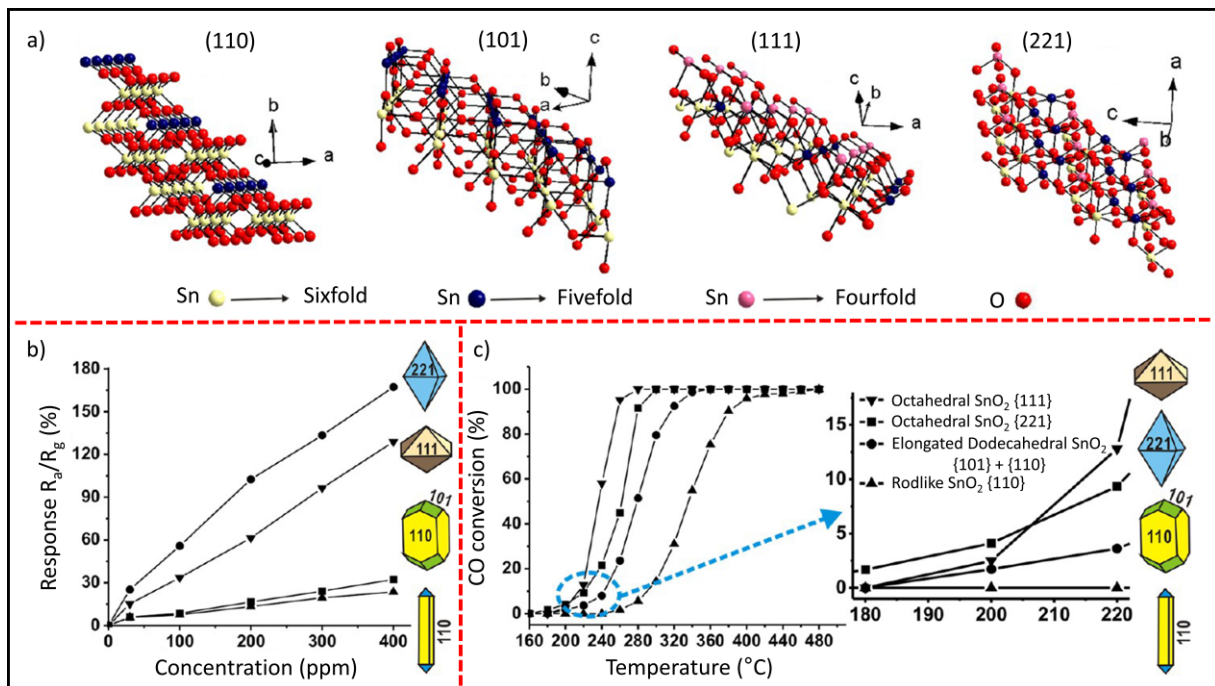
Figure 22. Effect of different crystalline morphology on gas sensing properties: a) atomic configuration of the facets, b) gas sensing response to ethanol and c) CO conversion curves of different faceted SnO_2 nanocrystals and an enlarged detail of the curve with corresponding structural models. Adapted from [96].

Nowadays, control of the exposed high-energy crystal facets is still a challenging research topic, especially for MOXs, in which the surface energy is very difficult to modify because of the strong metal-oxygen bonds [92]. Special attention has been paid to developing techniques, especially those based on the bottom-up approach, to precisely control the growth rate of different facets, shape, size and so on during the nanocrystalline materials fabrication process. Such types of faceted nanocrystals provide a great opportunity to design new catalysts with substantially higher catalytic reactivity, with preferring those high-index facets over low-index facets. [91]

1.3.3 The current approach in gas sensing using multiple nanowire-based structures

This subsection presents the different architectures used for the fabrication of gas sensors based on nanowires. Here are discussed the working principles, as well as the advantages and disadvantages associated with each architecture. The gas sensing platforms are classified according to their suitability for the best parameters for gas sensing, but also considering the possibility of using the structures for mass production will be justified. Moreover, following the previous sections, sensing platforms using preferably high crystalline nanomaterials grown by the bottom-up process will be described. Generally speaking, in gas sensors, nanowires are integrated either as multi-nanowire or single-nanowire structures.

1.3.3.1 Multiple nanowire-based gas sensors

This type of architecture commonly uses bulk or micromachined transducing platforms with Inter-Digital Electrodes (IDE). According to their working mechanism, platform structure, and signal enhancement they can be mainly categorized into conductometric type (detecting the resistance/conductance changes) and field-effect transistor (FET) type, using the same principle of conductometric type but with the advantage of modulating the measured resistance/conductance changes by an external electrical field [97]. Thus, the nanostructure arrangements can be principally divided into three groups:

a) Bottom IDE arrangement

An example of bottom IDE arrangement with vertically grown multiple NWs on the top of electrodes is depicted in Figure 23. As stated, the electrodes configuration is mostly IDE with positive and negative electrode allowing the measurement of resistance/conductance changes of the gas-sensitive (multiple NWs film) materials. Further, Figure 23a shows a structural model for a better image of the platform and the typical current flow distribution across the IDE. The multiple NWs grown on the patterned electrodes consist of several nanowire/nanowire junctions, which act as electrically conducting path for electrons, as seen in the detailed image representing the real structure in Figure 23b. In this type of arrangement, the current flow spreads across the multiple NW/NW connections. The device structure is facile and efficient compared to the structures described in b) and c) because the electrical contact between nanowires and electrodes is self-assembled during the (direct/indirect) deposition of NWs. Thus, the sensing properties of the system depend primarily on the NWs synthesis and integration process, which aim to achieve properly interconnected NWs and to obtain highly crystalline with the high surface-to-volume ratio.
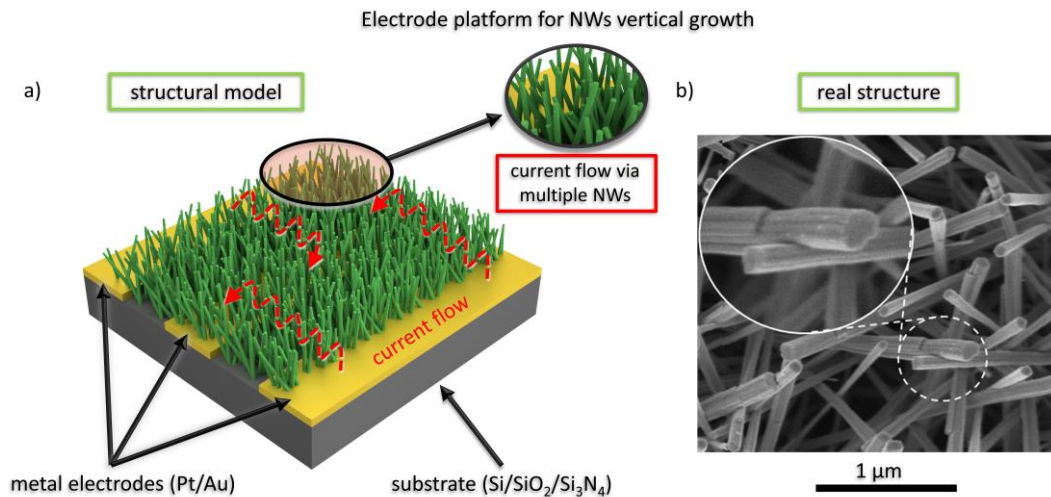
Figure 23. An electrode platform with bottom IDE for NWs bundles vertical growth: a) basic model, b) real structure of gas sensor with multiple NWs depicted by SEM image from the top view. Adapted from [98].

As can be seen, such nanowire networks provide a large surface area in 3D space. When considering NWs bundles, the conduction mechanism is dominated by the characteristic intercrystalline boundaries at NW connections, which act as intergranular contacts modulating the electrical resistance of the film. Unlike the nanograin films, in which the first exposed surface area is the upper layer, in case of multiple NWs systems, in principle, tested gases can immediately modulate the entire surface area of each NW, conduction channel, respectively. [99,100]

This type of architecture also allows for the facile functionalization of NWs with noble metals or MOX particles to enhance the sensing properties, as already mentioned in subsection 1.2.5. An example of modified structures on the top of IDE electrodes is shown in Figure 24, which illustrates the structural and band model of pristine SnO_2 NWs and its functionalized modification loaded with CuO NPs. This structural model (Figure 24a) depicts the distribution of the current flow via various NWs intercrossing and describes the type of conductivity in non-functionalized and functionalized NW surfaces. Thus, one can see that functionalized material, experiment an additional influence on the conducting channel due to the presence of decorating particles at the surface, which, in principle, can be compared to the behavior of functionalized polycrystalline grains. The resulting measured conductivity, in this case, is the sum of the parallel-series combination of all interconnected NWs.

Figure 24b shows the band diagrams in air and a reducing atmosphere with the potential energy barrier occurring at the interfaces. The potential energy barrier at the interface will then be decreased in the presence of a reducing gas that removes adsorbed oxygen. Thus, under air exposure, oxygen adsorption at the CuO surface increases the hole concentration due to the removal of electrons for bonding following by forming an accumulation layer where the CuO becomes more heavily p-type. This causes an overall larger potential energy barrier at this interface compared to that of a non-functionalized structure. [99]
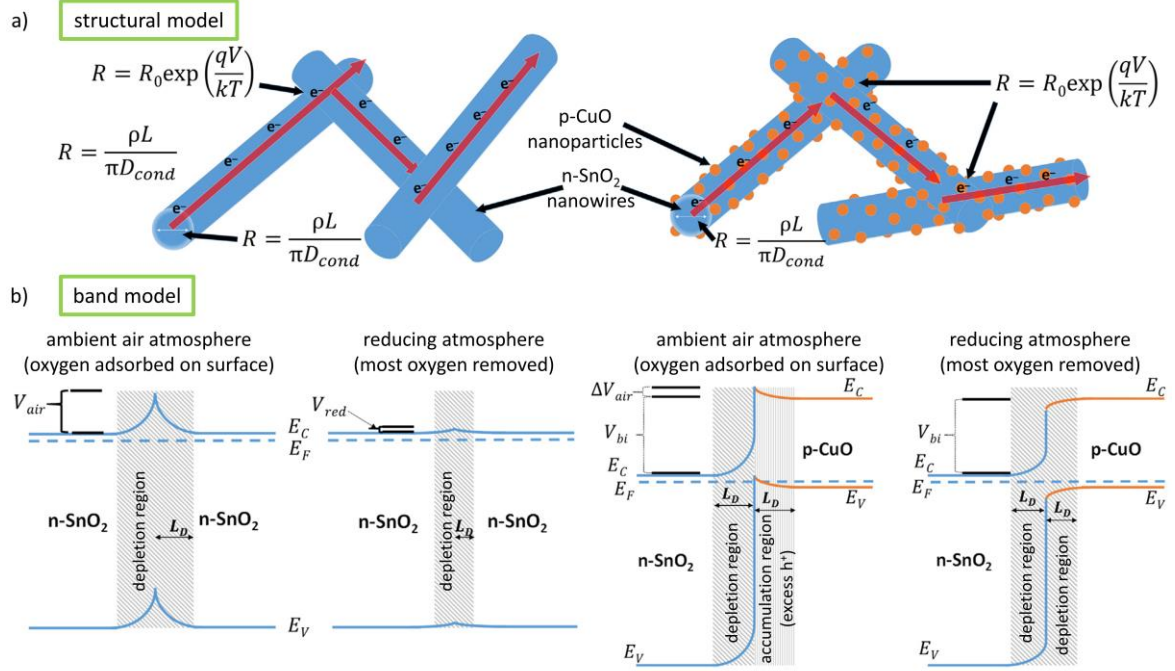
Figure 24. Mechanisms responsible for resistive changes in multiple NW based n-type gas sensors: a) the left picture shows the interfacial mechanism of pristine SnO₂ NWs, the right depicts the same mechanism and material functionalized with p-type CuO NPs; b) band banding model of these two structures underexposing of ambient air and reducing gas atmosphere. Adapted from [71].

Generally speaking, p-type nanoparticles on an n-type core compliment the changes in the depletion region of the core induced by oxygen adsorption. Oxygen creates an accumulation region in the p-type nanoparticles, which makes it more heavily p-type and makes a stronger depletion effect at the interface, driving the depletion region further into the nanowire core in conjunction with oxygen adsorbed on the exposed regions of the n-type core. In other words, at the p-n interface occurs the so-called "built-in voltage" potential V_{bi}, which gives rise to higher resistance in air and thus leads to a more significant response for reducing gases as compared to a non-functionalized surface. Heterostructures using n-type coated n-type nanowires can also be considered similarly. [71]

Below, it is summarized the advantages and disadvantages of bottom IDE arrangments for the integration of multiple NW based films:

- **Advantages**

    a. the large surface-to-volume area which potentially ensures a high response,

    b. direct integration without redeposition and extra steps

    c. simple fabrication technology suitable to produce high crystalline nanostructures,

    d. due to the latter, the target gas species react on the surface of NWs, diffusion into the bulk is negligible, the response and recovery time should be short,

    e. such a structure can be further functionalized by noble metals or MOX NPs in order to enhance sensing properties.

- **Disadvantages**

  a. possible loss of the intergranular (NW-NW) connection due to aging (cracking of the interconnection),

  b. the current flow leads via intercrystalline boundaries; these intergranular contacts provide most of the sample resistance and the sensing potential of the single-channel is unexploited,

  c. also, the NWs which are not interconnected, are not active for sensing,

  d. not possible to use modulation of a measured signal by external electrical field such as FET type so that structure is limited to be used in conductometric mode only,

  e. depends on structure distribution and its proportions, but gas species may react in the topper parts of the nanostructure; thus the bottom parts may be less affected,

  f. it is difficult to control the quality of a nanocrystalline bottom layer (seeds) indirectly grown structures either by VLS (Vapor-Liquid-Solid) or VS (Vapor-Solid) deposition technique,

  g. due to aging instability of NWs network can cause baseline changes, which is an undesirable effect in gas sensing.

b) *Top or bottom-top IDE arrangement*

The realization of such a type of the electrode platform with NWs can be done only under certain circumstances, which depend, in particular, on their size and surface distribution of NWs. For NWs with a length of about 10 μm, the real fabrication of the structure with the top electrode arrangement is from a technological point of view very complicated. This does not apply to cases where the NWs are spread on the surface, or their length is about hundreds of nm. Then, the electrode platform can be made on the top by some deposition technique, as shown in [101]. However, despite this deficiency, this structural arrangement can be used as a model example that could bring further benefits to NW-based systems.

Based on the example in Figure 25, in which vertical nanocolumns [102] were employed with top and bottom electrodes, it is noticed that the integration of a top electrode needs extra post-processing steps (metallization, masks or lithography) that might introduce contaminants to the sensitive films and deteriorate the structure.
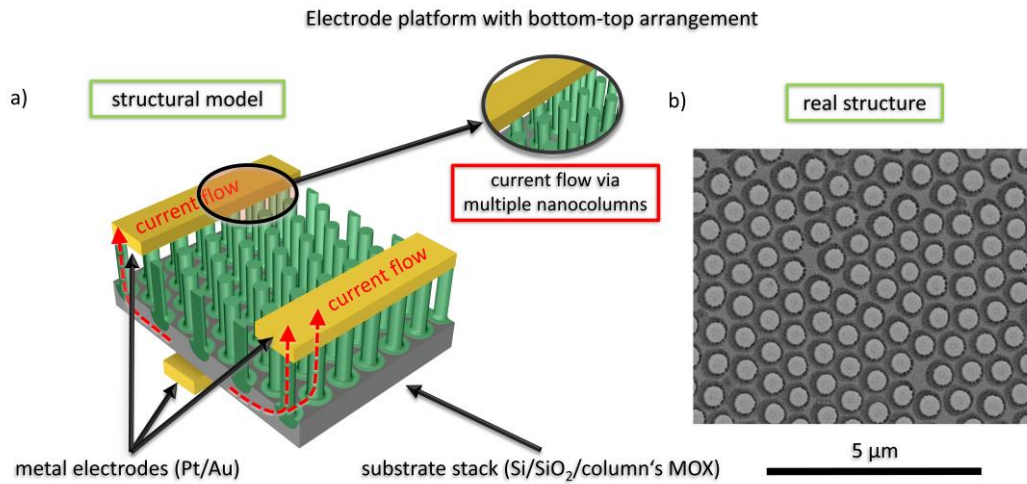
Figure 25. An electrode platform with vertically grown nanocolumns: a) basic model image, b) real structure with hexagonal-arranged Au nanocolumns arrays on the glass substrate, depicted by SEM image from the top view. Adapted from [103].

On the other hand, the architecture shown in Figure 25a, which combines well-organized nanocolumns with top electrodes enables to connect all nanocolumns in parallel without any intergranular boundaries, making the current to flow and distributed between all nanocolumns under the top electrode. Consequently, the gas sensor with as-prepared electrode platform is taking advantage of a large number of sensitive nanostructures, those which are in direct contact with electrodes, respectively. Nevertheless, in very dense structures, the problem with surface density distribution of the gas may arise during the gas exposure, as shown in simulation Figure 26, where the high occupancy of the gas on the surface of nanocolumns occurs primarily in the top parts, but very low in the area under the electrode. This undesirable effect may be crucial for gas sensor parameters such as the sensor response and response time. [104]
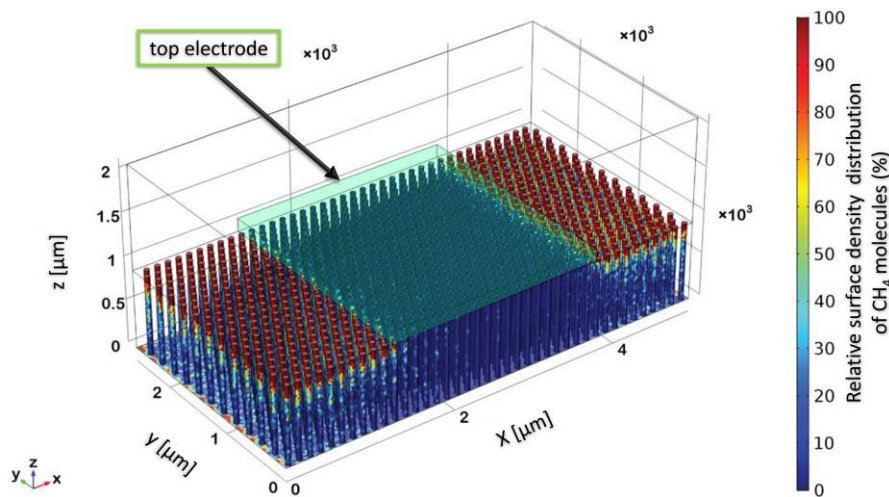
Figure 26. A simulation of a relative surface density distribution of CH_4 molecules in nanocolumn-based structures. Adapted from [104].

The summary of the advantages and disadvantages of the IDE electrode platform with vertically grown nanocolumns:

- **Advantages**

  a. no need usage of any transfer or integration technique to connect a sensitive material when the electrode system can be made on the top side,

  b. top electrodes enable to interconnect a high amount of nanocolumns in parallel with excellent electric contact, which both can provide amplifying of sensing signal,

  c. sensing current flows via single-crystalline nanostructures without any intergranular boundaries,

  d. large and fast response dynamics due to the large surface-to-volume area.

- **Disadvantages**

  a. due to this, possible short-circuits can appear at the bottom of the structure if the seed density is not appropriately controlled,

  b. with this fabrication technology is not possible to integrate different kinds of high-quality 1D nanomaterials such as nanowires, nanotubes, nanocolumns of various kinds (WO_3, SnO_2, TiO_2, functionalized structures) in one sensor device (substrate carrier),

  c. possible contamination of the sensitive material during the post-deposition (lift-off) of the electrode contact but also during fabrication steps (photolithography, coatings and so forth),

  d. possible problem with gas distribution across the nanocolumns due to the top electrode restrains the gas access to the active surface,

  e. possibility to use FET arrangement with the third electrode for enhancing the sensing properties is very limited by fabrication technology.

c) IDE arrangements for planar alignment of NWs

Another possible path to develop sensor devices, which can partially eliminate the disadvantages of the previous structures (particularly those coming from the nanowire-nanowire interface), is the integration of high crystalline 1D nanostructures horizontally to the substrate and across electrodes. However, apart from multiple NWs interconnection, which is achieved in previous architecture by special deposition techniques (e.g., VLS or VS), the planar arrangement platform also offers either an opportunity to use the IDE system for other types of integration techniques, including cost-effective methods suitable for transfer, precisely position, and NWs interconnection.

Among others [84], the most promising techniques to integrate aligned nanowires on IDE systems and avoid the nanowire-nanowire interface connection, include a macroscopically driven technique in which NWs are transferred in a liquid suspension and then drop coated on the top of electrode system following an alignment procedure induced by dielectric forces. This

approach, so-called dielectrophoresis (DEP), solves the concerns of any subsequent micromanipulation or post-processing technique, which is needed so far for the development of devices that combine planar electrode systems with 1D nanostructures. In Figure 27 is illustrated the structural model of electrode platform with IDE organization and the real structure operating as the gas sensor device using this approach.
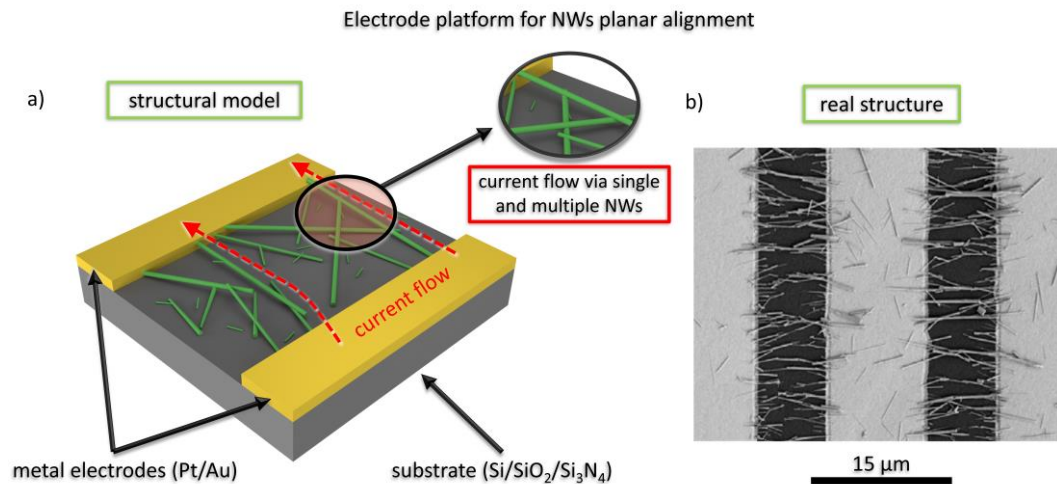
Figure 27. An electrode platform for NWs planar alignment: a) basic model image, b) real structure of gas sensor with interdigitated electrodes depicted by SEM image from top view. Adapted from [105]

Comparing to the previous platform based on NWs, where the intercrossing between bundles of NWs provide current flow, the conduction channel in this structure is realized by multiple NWs interconnection, and over single NWs, both are aligned in parallel as shown in Figure 27b. Accordingly, to this, the device based on this technology is capable of taking advantage of the favorable properties of single-wire devices, which will be described further.

Below, it is summarized the advantages and disadvantages of the IDE electrode platform for planar placement of NWs:

- **Advantages**

  a. facile integration technology able to build up a sensor device with multiple and single NW interconnections by using the suitable macroscopic technique (DEP),

  b. no need of any subsequent micromanipulation, lithography or metallization process,

  c. it is possible to integrate different types of high-quality 1D nanomaterials (nanowires, nanotubes, nanocolumns and so forth) of various kinds (WO_3, SnO_2, TiO_2, functionalized structures),

  d. offer to attain the functionalities and advantages expected from individual NWs and thus a potentially better use of self-heating effect, [99,106]

  e. due to latter, the possibility to develop ultra-low-power devices without a heating system,

    f. large and fast response dynamics due to the large surface-to-volume area, the sensor response may be amplified by using a three-electrode system (field effect transistor arrangement),

    g. simple fabrication technology, similar to the top-down process with features of bottom-up without the need for unique electrode design.

- **Disadvantages**

    a. the current flow still partly leads via intercrystalline boundaries; these intergranular contacts provide most of the sample resistance, so the effect of single NWs is subdued, and the sensing potential of the single-channel is unexploited,

    b. nanowires/metal contacts quality may be poor so that it can cause a possible noisy response of the measured signal,

    c. still, the partial intergranular connection may cause losses due to the aging (cracking of the interconnection),

    d. due to aging instability of NWs network can cause baseline changes, which is an undesirable effect in gas sensing,

    e. material for the IDE electrodes should be made of non-corrosive metal (gold, platinum) due to the use of liquid suspension for DEP purposes, which can cause degradation problems during aging.

1.3.3.2 Single nanowire-based gas sensors

In this sub-section, the attention is focused on sensor configurations that focus on the use of single NWs to avoid the grain (or nanowire-nanowire) boundaries present in polycrystalline and multiple nanowire systems. In this line, recently published studies [107,108] concluded that the structures based on single-crystalline NW connection exhibit novel properties attributed to their well-defined geometry and negligible presence of grain boundaries. These findings give rise to build a new generation of gas sensors, which are more efficient than their counterparts based on multiple-NWs or thin-film (polycrystalline) layers, namely, due to extremely low consumption, small dimensions of active sensing element taking a tiny place on the chip and unique possibility to modulate their sensing properties (i.e., sensitivity and selectivity) by additional functional blocks.

Figure 28 illustrates the operating principle differences between MOX sensor formed by a thin-film layer of nanocrystals (which is comparable to the multiple NW-based sensor approach) and single NW-based approach with monocrystal structure. As stated above, the operating principle of chemoresistive MOX sensors is based on their conductance/resistance changes during gas exposure. However, as can be seen in Figure 28b, the modulation of the conduction channel by the adsorbate gas species in polycrystalline films differ from that of monocrystalline structures (e.g., single NW). In polycrystalline films (joined mostly by necks

and grain boundaries) the gas-solid interaction involves only upper grains, whose are in direct contact with adsorbates results in unclear determining of the gas influence on the sensor response. In other words, the electric field that causes the band bending at the surface due to gas-solid interaction (marked as E_{bar} in Figure 28) does not significantly affect the entire conductive channel in conductometric measurement performed by externally applied electrical field (E_{bias}), which can be represented by sensing current.
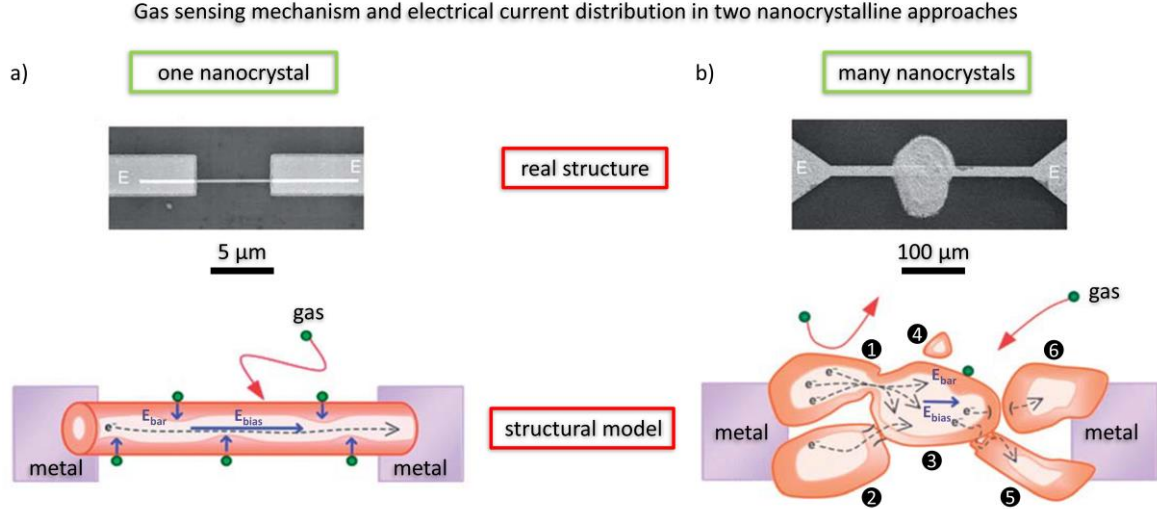
Figure 28. Different approaches in the development of nano-chemiresistors showing gas sensing mechanism and electrical current distribution in: a) one nanocrystal and b) many nanocrystals approach, where the numbers represent different types of necks and grains boundaries. Adapted from [13].

In contrast, Figure 28a shows the approach in a monocrystal (single NW), in which pure surface effects can theoretically describe the gas sensing principle without the contribution of gas diffusion among nanograins/nanowires. In this case, the intensity of the associated electrical field (E_{bar}) caused by adsorption of gas molecules at the surface of NW modulates the width of a depleted region, which have a direct influence on the sensor response related to conductance/resistance changes along the entire conductive channel. [109]

A couple of examples related to the electrode arrangements for the realization of a single NW based gas sensor is depicted in Figure 29. Generally, the electrode configuration for gas sensor based on single NWs include systems with two electrodes to apply conductometric principle for the interpretation of the measured response (conductance/resistance changes), or systems with three electrodes, in which the third electrode is used to enhance the sensing performance (tune the carrier concentration along the NW) by an additional electric field, similar to the principle based on field-effect transistor (FET). Typically, the fabrication of these electrode systems requires standard lithography techniques followed by metal deposition, but most of the time, these fabrication steps need to be combined with electron-beam lithography (EBL) or focused-ion-beam/electron-beam technique (FIB/EB). The application of one or another step depends on the method of synthesis or integration of NWs assembled to the electrodes. For instance, NWs can be integrated lithographically across the electrodes (top-

down approach), or be synthesized and transferred onto the final device substrate (bottom-up approach depicted in Figure 29b), as described in 1.3.1 subsection.

In the case of single NW FET gas sensors (i.e., structures with a third electrode operating as the gate) usually, the third electrode acts as bottom-gate (label G), whereas the other two act as drain-source (labels D and S), as shown in Figure 29a. In these systems, the concentration of free carriers in the conductive channel is modulated by the gas-solid interaction on the surface of NW, as in regular chemiresistors, but due to the third electrode, the conductive channel can be further tuned via the gate voltage and thus enhance the gas sensitivity of the sensor.
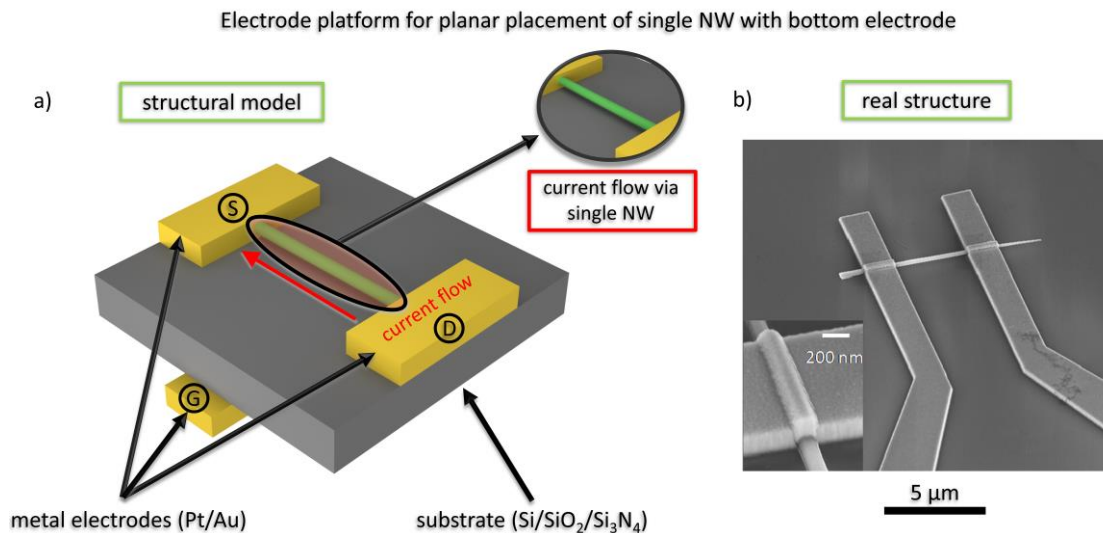
Figure 29. Electrode platform for planar placement of single NW with bottom electrode: a) basic model image, b) real structure for measurements of ZnO NW photoluminescence properties using deposited electrodes over the NW, depicted by SEM image. Adapted from [110].

In addition to gas sensitivity, the rate and extent of oxidation and reduction reaction taking place at the surface of NW (n-type) can be modified by changing the electron concentration via tunning the base conductance of the wire through the gate voltage, which is a characteristic property of NW FET gas sensors. When the gate voltage is carefully selected, the sensor response can raise extremely high or decrease down to the state, in which case the NW channel is deeply depleted, and no response can be detected to both oxidizing and reducing gases (seen in Figure 30b). This behavior is different in contrast to the conventional two electrodes conductometric gas sensors, in which the base condition of the channel remains fixed, as depicted in Figure 30a.

Gas sensitivity is not the only parameter that can be affected by manipulation with the gate potential. Figure 30c depicts an interesting example of selectivity improvement by applying the gate voltage potential. In this example, NW functionalization together with gate voltage influences the working conditions of sensor exhibiting the unique single target gas response to CO. Figure 30d shows the reason of such behavior, showing that only CO brings about a remarkable change in the output current (I_{DS}) for Au decorated NW, while the gate voltage (V_{GS}) is about -5 V up to 10 V, approximately. In this range, the alternation of gate

voltage (V_{GS}) is not sufficient to switch the FET to on-state, in other words, be able to sense other reducing gases, as it is described in [111].
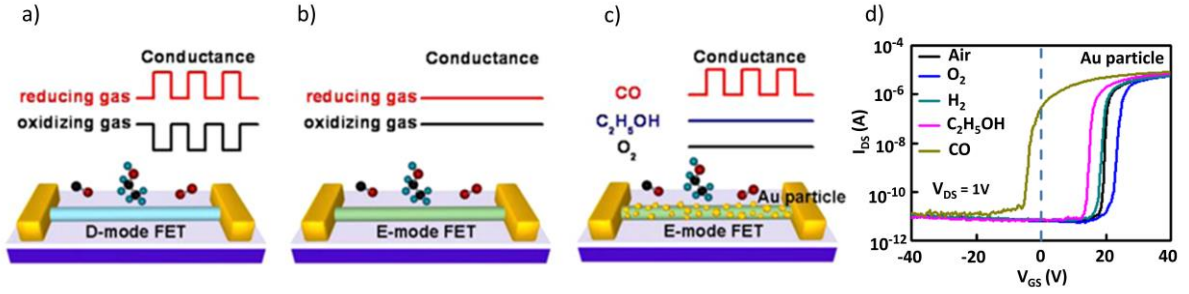
Figure 30. Illustration of the single NW (n-type) gas sensor response enhancement by the third electrode combined with NW functionalization and its influence on gas sensing properties: a) conventional depletion mode for detection of both (red./ox.) gases, b) deep enhancement mode with very large positive threshold voltage yield no response to any targe, c) combing mode – deep E-mode + functionalized NW with Au NPs exhibiting the unique single target gas response, d) I_{DS}-V_{GS} curves at V_{DS} = 1 V for the back-gated In_2O_3 FETs with the noble metal functionalization . Adapted from [111].

As stated, if the NW channel is deeply depleted by applying gate voltage potential, the sensor has no response to both oxidizing and reducing gases. Thus, when the surface of NW is functionalized by a decoration of selected catalytic metal NPs, such as Au, Pt or Ag, it influences both sensitivity and selectivity of the gas sensor, but also a value of threshold voltage (V_{TH}) as compared to that measured for pristine NW.

The decoration of catalytic metal NPs on oxides has been an effective method to improve the activity of oxide surfaces, and this can be done either directly after the NW growth or when they are transferred to the final substrate. Figure 31 illustrates the influence of the functionalization on n-type NW conducting channel and the mechanism responsible for the resistance changes under the exposure in a different atmosphere (air, reducing gas H_2). The NW functionalization and the effect on gas sensing mechanism are similar to grain functionalization, which is described in 1.2.5 subsection.

a)

NW cross-section model

$L_D \approx 0$ $D_{cond} \approx D_{NW}$

L_D D_{cond}

L_D D_{cond}

non-functionalized

no oxygen adsorption

significant oxygen adsorption (air)

reduced oxygen adsorption (H_2 present)

b)

NW cross-section model

L_D D_{cond}

L_D D_{cond}

L_D D_{cond}

functionalized with NPs

no oxygen adsorption

significant oxygen adsorption (air)

reduced oxygen adsorption (H_2 present)
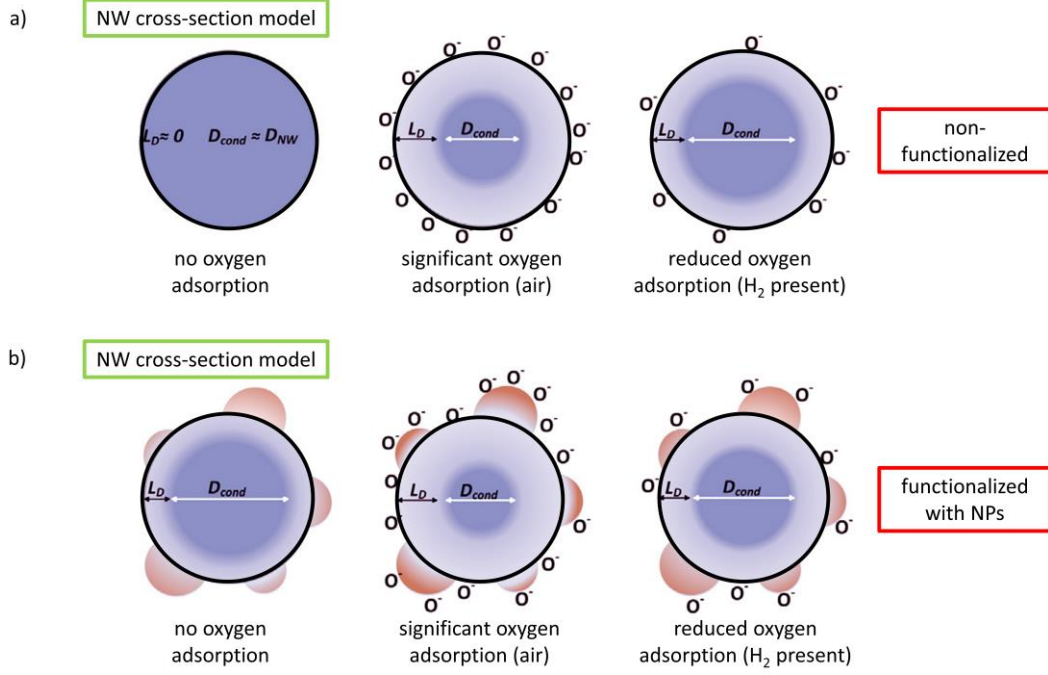
Figure 31. Cross-section model showing changes in the depletion layer and conducting channel of n-type NW during various atmosphere exposure: a) non-functionalized NW, b) functionalized NW with noble metal NPs. Adapted from [71].

Additionally, there are other relatively new attractive features related to single NW-based structures, which are intensively investigated, and recently recognized as promising tool that play an important role in further enhancing gas sensing properties of two electrodes (conductometric) and/or three electrodes (FET) configuration:

- both configurations are capable, under certain conditions, to work at room temperature, even though the conductometric sensors usually work at $200 - 400\,°C$. Self-heating effect was found to be an effective feature for additional reduction of operational power as well as recovery characteristics. Here NW can work as an ultralow-power nanoscale heater provides its temperature via Joule heating effect [106],

- under the same conditions, at room temperature, the gate potential (FET) can be used as an effective method to "refresh" the NW sensors. The recovery process is accelerated usually by massive gate potential, which is high enough to reach the activation energy for desorption [112].

The features mentioned above might help to miniaturize gas sensors significantly, as well as to reduce the power consumption due to no further needs of additional external heaters.

2 Fabrication and development techniques

This chapter is dedicated to fabrication and development techniques, which were performed during the realization of the experimental part of this thesis. Since this work is focused on to present a new generation of a gas sensor based on nanowires, the fabrication of such a device is required. Hence, the basic description of the methods as well as the fundamental purpose for which they were used, is presented. Also, the type of equipment, their working functions, and features are listed.

2.1 Substrate cleaning and surface preparation before lithography

The purity of substrate surfaces is an essential requisite for the successful fabrication process. Techniques and processes to generate very clean wafer surfaces avoiding the unwanted contamination and/or impurities are critically important. Contaminants, which occur on silicon wafer surfaces can have different nature such as discrete particles, metallic contamination, adsorbed gasses, and many others. Generally speaking, the wafer cleaning procedure is about contamination control, which means, in principle, leaving the surface in a controlled and known condition for further fabrication steps.

2.1.1 Wet-chemical treatment

In this work, silicon wafers of various sizes with a silicon dioxide layer 300 nm, approximately, was used as a basic substrate. The oxide layer provides good dielectric insulation between the silicon and conductive path for an electrode system, which was deposited in the form of a thin layer, mostly for the first fabrication step. For this reason, standard wafer cleaning procedures, e.g., RCA cleaning steps (named after Radio Corporation of Amerika company), which include thin oxide layer removal step, could not be carried out. Instead, wafers were cleaned by a solvent clean procedure performed with high-purity chemicals in an immersion bath (glassware) or with another technique support (spin-coating), followed by deionized water (DI) rinse and drying step. Typically used wet-chemical treatment procedures performed preferably in sequence:

- **NMP-based solvent stripper bath** – this solvent is designed for efficient removal of a wide range of resist films compatible with PMGI, PMMA and copolymers, SU-8, and other resists placed on silicon, silicon dioxide, and many others substrate surfaces. In immersion mode, a two-bath system was used to reduce the possibility of redeposition followed by isopropyl alcohol (IPA) and DI rinse and dry. Immersion combined with a sonication bath is a suitable technique either for the lift-off process. However, NMP-based procedure with sonication was mainly used for resist removal after every lithographic step.

- **Single-wafer spin cleaning** – this procedure was performed as a basic wafer cleaning technique which includes two-solvent clean with acetone followed by

IPA rinse while using a spin-coater tool (described later in 2.1.4). Wafer cleaning with this procedure was preferably accompanied by oxygen plasma treatment for maximum efficiency of organic contaminant species removal.

2.1.2 Oxygen plasma ashing treatment

As stated, oxygen plasma treatment is the process of removing organic compounds by using plasma source, which is created in a process chamber by exposing oxygen gas under vacuum conditions to a high-frequency voltage source. Concerning photoresist treatment, this process is called plasma ashing or stripping in semiconductor manufacturing.

In this work, Diener Nano plasma cleaner was useful tool, which provided a diverse range of operations, from wafer surface cleaning before spin-coating, photoresist stripping, to the surface modification/activation process, for example, change the surface energy properties in order to enhance the quality of adhesive bonding. Additionally, among important technique, with which the fabrication process would not be successful, there is the so-called "descum" process. It is a process, which removes a few hundred angstroms of undetected photoresist residues ("scum") remaining after insufficient developing of the pattern in trenches, see in Figure 32. Descum was used after every wafer coating as a pre-step before deposition or etching procedure to prevent non-uniform resist profiles because even a very thin layer of resist residue can cause completely fail of a subsequent fabrication step. [113]
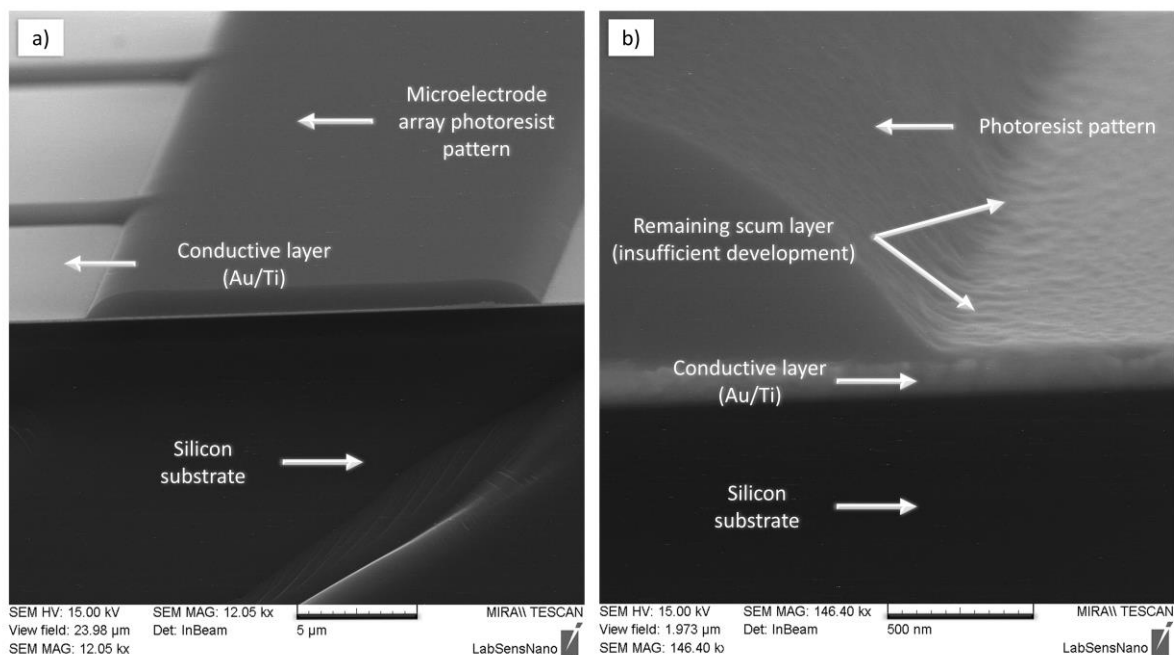
Figure 32. SEM inspection of insufficient development process remaining photoresist residues: a) cross-section of a microelectrode pattern, b) cross-section detail view of remaining scum layer (resist leftovers).

2.1.3 Lithography process chemistry

Precisely cleaned wafer surface must be pretreated in order to obtain uniform coverage of the resist for the lithography process. Hence, an adhesion promoter has to be used to enhance the sticking properties between the wafer surface and resist. However, firstly, the adsorbed

water on the surface of the wafer is removed by dehydration bake procedure at a high temperature between 150 and 200 °C. Then the adhesion promoter is applied on the wafer surface, in our case silicon dioxide (SiO_2). This results in a reaction that produces a high water repellent layer and prevents unwanted lifting of small photoresist structures in the pattern. A very thin uniform coating (approximately tens of nm) is achieved typically by liquid dispensing of fixed volume on the spinning wafer or by evaporation of the adhesion promoter over the entire wafer surface. Hexamethyldisilazane (HDMS) using both techniques and also Allresist GmbH AR 300-80 using spin-coating method were used as adhesion promoters in this work. [95]

The film forming 3D relief images of the designed pattern in the plane of the substrate is called resist that is sensitive polymer consisting typically of at least three components: a base material (resin), a sensitizer responsible for chemical reaction and a solvent that controls the mechanical properties, such as the viscosity state of the polymer. One of the most basic categories into which resist can be divided is its polarity, as shown in Figure 33.
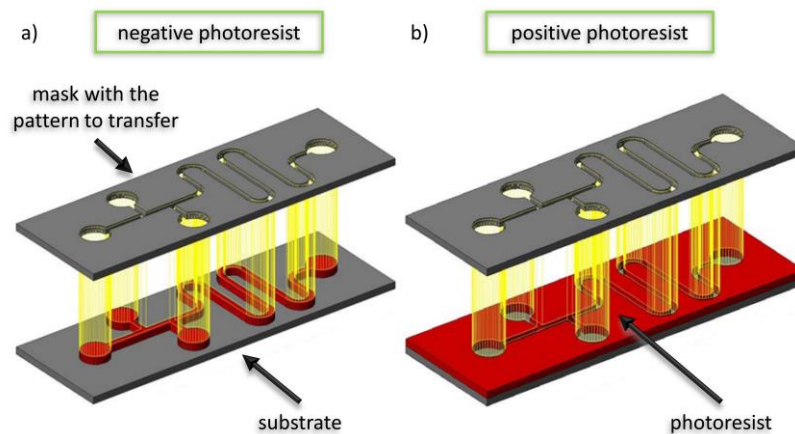
Figure 33. Illustration of the positive and negative photoresist essential. Adopted from [114].

When resist is exposed to the radiation, which, in principle, can be either UV light as well as electron-beam, and after the immersion in a developer, positive resist react in the way that ideally the unexposed regions remain unchanged, the exposed regions dissolve faster during the development process, respectively (Figure 33b). Upon exposure to light, a chemical process occurs by which the inhibitor becomes a sensitizer, increasing the dissolution rate of the matrix. In contrast negative resist, in which the exposed regions are dissolved in the developer, while exposed regions stay covering the surface (Figure 33a). The developer is basically a solvent that selectively dissolves the resist in a chemical reaction with its parts (enlightened vs unenlightened). Currently, non-alkaline developers mostly based on hydroxides, e.g., tetramethylammonium hydroxide (TMAH) or sodium hydroxide (NaOH), are used in developing process of photosensitive resist and organic solvents for electron-beam resists. [115]

Selected resists (from Allresist GmbH) further used in this work:

- **AR-P-3540** – is a highly sensitive and high-resolution positive-tone standard resist suitable for lithographic mask processing of integrated circuits, designed for the use of strong TMAH developers, such as AR-300-44. The resist exhibits excellent adhesion on metal and oxide surfaces. [116]

- **AR-N-4340** – is a highly sensitive, chemically amplified photoresist. The resist exhibits similar adhesion properties as later. Additionally, it can be developed in an aqueous alkaline developer (AR-300-475 recommended), and by a variety of developing process, undercut profiles sufficient for lift-off process can be reached. [117]

- **AR-BR-5400** – is optically transparent, non-light sensitive poly-methyl methacrylate (PMMA) copolymer, specially designed for thermal stable resist structures (up to 230 °C) and lift-off applications. The resist can be used in combination with both positive and negative photoresist as a bottom layer, which is dissolved in developing step with an upper photoresist that gives rise to isotropic profile undercut. Moreover, this double-stack resist solution can prevent the problems with redeposition (fence-like structures) which occurs during dry etching processes, in particular when using etching by accelerated ions. In this context, the removal procedure after etching is easier with double-stack than with only one-layer (top) resist. [118]

- **AR-P-6200 (CSAR 62)** – is a positive-tone electron-beam resist provides very high sensitivity with resolution down to 10 nm. The resist is suitable for a wide range of acceleration voltage (1 − 100 kV) and fabrication of lift-off structures. [119]

In this work, the e-beam resist was used for the realization of the finest nanoelectrode structures (typically structures up to 1 μm), unlike the photoresists, which are used for structures from 1 μm up.

2.1.4   Applying and developing resist

In general, there are several types of techniques for photoresist coating, namely, spray coating, spin coating, or coating by immersion. The coating of the wafer is usually done by spin coating, which is a standard method widely used in microfabrication providing deposition of uniform thin films to flat substrates. A small amount of coating (1 ml/inch) is applied to the center of the substrate spinning at low speed or not spinning at all. In order to spread the coating material, the substrate is rotated at high speed using centrifugal force, which results in a uniform coating over the wafer. The schematic illustration of the spin coating technique is shown in Figure 34. [120]

After the exposition and depending on the resist type (positive/negative), the patterned areas are soluble or insoluble in chemicals developers. For the photoresist development can be used dipping bath (immersion development), spray or puddle processes and several others. A preferable technique applicable for experimental work (low series and small samples) is immersion in a dipping bath.

In this work, spin coating and development were made using SÜSS MicroTec coating and development (industry) system RCD-8, which, among others (like simple spin-coater Labspin6), promotes a wide variety of application from HDMS adhesion treatment, metal lift-off procedures to cleaning or resist stripping. This equipment comprises a basic manual spin coater to a GYRSET® enhanced coater and puddle and spray developer tool.
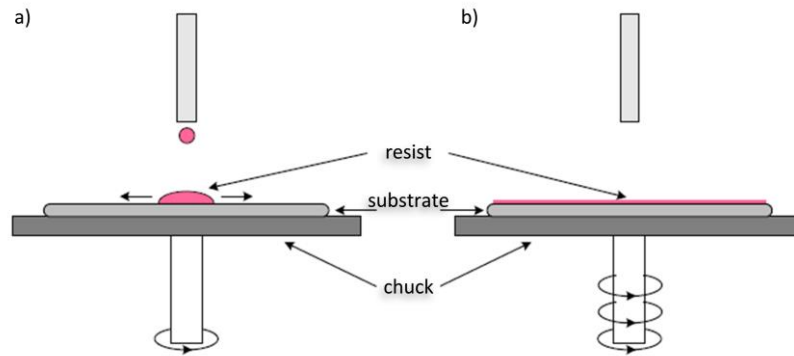
Figure 34. Schematic illustration of a spin coating technique using SÜSS MicroTec RCD-8 and Labspin6 [121].

2.2 *Software for the chip design and lithography software for exposure optimization*

2.2.1 Design editor and viewer for the chip layout

Typical lithography package usually contains the editor of one or more commonly used file formats. The strict difference in between the opensource and commercial application lies in the presence of library support and design acceleration toolkits which contain guided design rules and building blocks. Since the work is mainly oriented on the design and development of a unique structure, the commercial package would not be beneficial. Instead, an open-source utility kLayout high-performance layout viewer/editor was used.

The kLayout is a fast-growing software package bringing all major necessary utilities for parametric cell design drawing, design rule check and it is widely opened for user modification and scripting. The software supports all the industry-standard file-formats including GDSII and OASIS.

2.2.2 Advanced design optimization tools

A high-resolution electron-beam (E-beam) and laser-beam lithography are severely impacted by process effects such as beam scattering effects (proximity) and tool implied artifact forming effects, which are causing the non-ideal pattern transfer. Although the E-beam printer

is highly sophisticated equipment, in highly demanding applications (demonstrated in this work later) the pattern data and those effects causing by various error sources must be optimized.

GenISys Tracer® is a Monte Carlo simulator that computes the electron-solid interaction of arbitrary material stack and performs advanced process calibration for E-beam proximity effect correction. A final product of the simulation is spatial energy distribution described as Point spreading function (PSF), shown in Figure 35. [122]
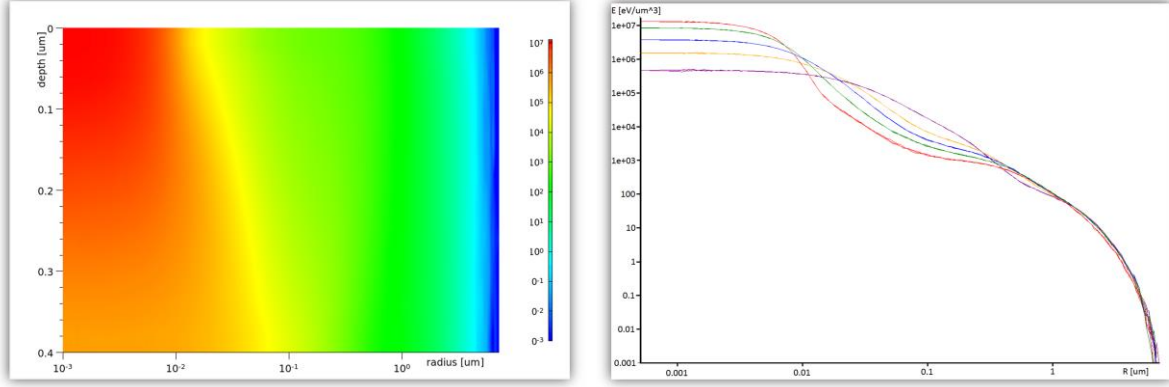
Figure 35. Illustration of spatial energy distribution simulation.

Information from PSF description of real energy deposited to the resist together with proximity effect correction (PEC) could be used for design modification, with which is possible to achieve a high-resolution throughput. Software package GenISys BEAMER® performed these operations, where the result of the simulation shows modified proximity corrections applying different energy dose to different points in the designed structure to flatten the energy density across the pattern, as shown in Figure 36. [123]
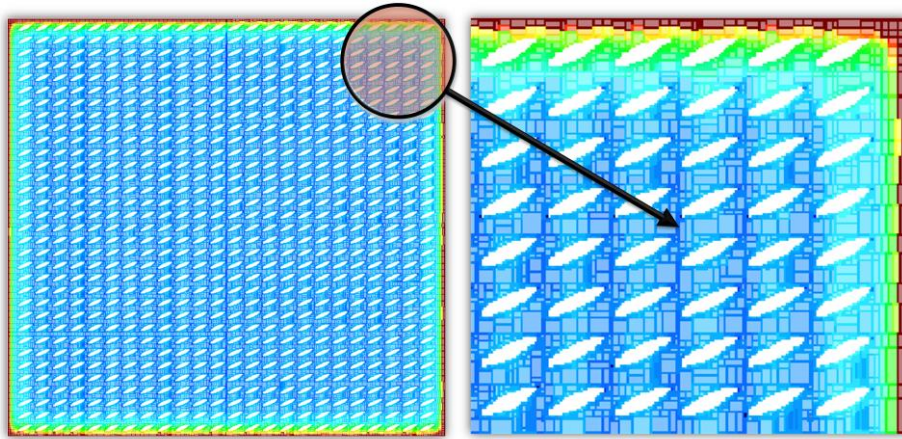
Figure 36. Illustration of proximity correction simulation with various energy doses across the pattern.

2.3   *Pattern transfer lithography techniques*

In this subsection, lithography techniques used in this work are divided into three types by photolithography using direct writing laser, masks or templates and E-beam lithography. A fundamental principle of the method and description of the equipment is briefly described.

2.3.1 Direct-write laser photolithography – maskless lithography

In general, maskless lithography is a method, with which designed layout is directly transferred onto the substrate without utilizing an intermediate static mask. Direct writing is a form of maskless lithography, where the radiation is focused to a narrow beam that is scanned in vector over the wafer with resist. Direct laser writing is a part of maskless optical lithography, which offers a cost-effective and flexible method for R&D applications (prototype designs).

Direct-write laser system (DWL) Heidelberg 66FS was used for the realization of microstructures with resolution down to 1 μm mostly on wafers, but also photomasks were developed. This research equipment allows working with any flat substrates coated with photoresist from 20x20 mm up to 200x200 mm. The system can utilize a variety of different lasers, which makes it possible to expose nearly all photoresists. Furthermore, the DWL is equipped with high-resolution CCD cameras, which can be used for alignment purpose, to perform overlay exposures, respectively. Figure 37 depicts a similar device and its main components.

Among the advantages of this technique, we could say it is a possibility to make any patterns of any size, with the only limitation given by the critical dimension. On the contrary, this technique suffers from low throughput of fabrication as compared to traditional photolithography (see in 2.3.2).
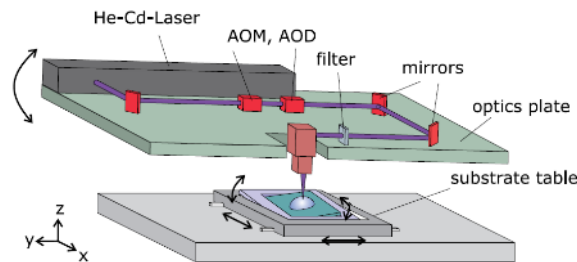
Figure 37. Schematic illustration of the direct-write laser exposure technique [124].

2.3.2 Contact and proximity photolithography – through-mask lithography

Compare to the direct writing lithography, the contact/proximity lithography uses a mask that contains an image of one layer of the process. In principle, the wafer is aligned with the mask, clamped together, and then the radiation from a high-intensity lamp is used to expose the wafer with the pattern on the mask, shown in Figure 38b. In contact lithography, the distance between the mask and wafer goes to zero. Therefore, it causes defect degradation of the resist-coated wafer as well as the photomask. For this reason, the proximity printing was developed to eliminate unwanted damage by the separation gap between the wafer and mask with a distance of about 10 – 50 μm, usually. Then, the resolution is slightly limited primarily by light scattering in the resist. The illustration of the proximity method is shown in Figure 38c.

Süss MicroTec mask-aligner MA8 standard UV lithography was used for exposing wafers through a mask with patterns. The working function was mostly verified in low-series production by prototype structures. The photoresist-coated wafer is illuminated by UV light in the range of 350 – 450 nm wavelength, which is produced by 1000 W mercury vapor lamp.

Exposure can be carried out over the surface of up to 6-inch wafer in either proximity or contact mode. The maximal resolution, which can be accomplished with this equipment depends mainly on the finest structures realized on the mask. A schematic example of such a device is depicted in Figure 38a.
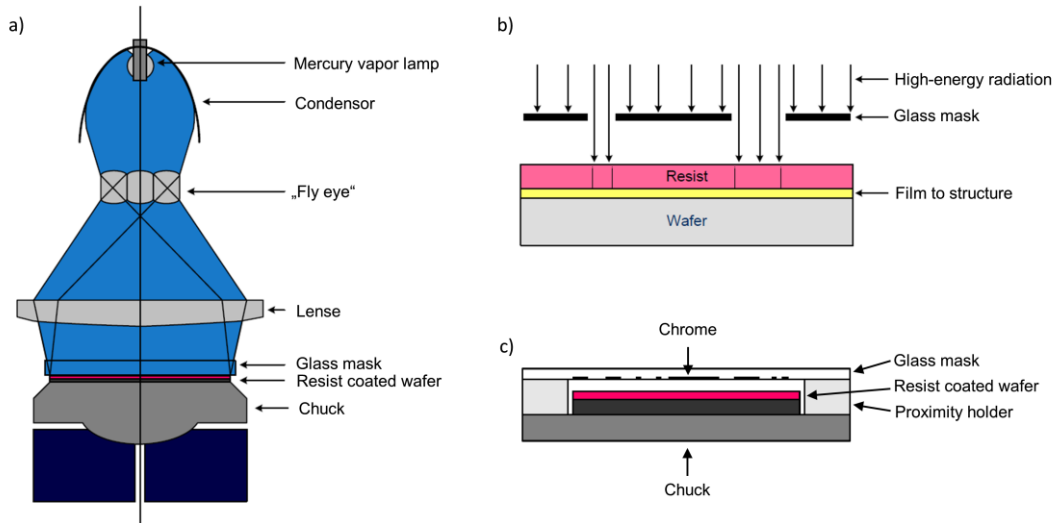
Figure 38. Schematic illustration of through-mask lithography: a) mask aligner system, b) through-mask exposure principle, c) proximity mode system. Adopted from [121].

2.3.3 Electron-beam lithography

Electron-beam lithography (EBL) belongs among direct writing techniques, which allows the creation of structures down to a few nanometers dimensions. In principle, lithography is performed using a scanning electron microscope (SEM), in which accelerated electron beam formed through a series of electrostatic lenses and variety of apertures into a narrow beam is directly patterned into the electron-beam sensitive resist by one pixel at the time. Figure 39 shows a typical inside organization of EBL system.

A high-resolution EBL system Raith 150 Two was used for fabrication of the finest nanoelectrodes and other nanostructures made in this work. It is equipped with ultra-high resolution Carl-Zeiss Gemini electron optics system with InLens and SE detector, sample holders capable of mounting up to 6-inch wafers. The lithograph offers a selection of broad ranges of voltages from 0.3 up to 30 kV and apertures, to control the beam current. High precision writing is possible due to the laser interferometric stage with the lateral movement resolution of 2 nm and large-scale Z travel.
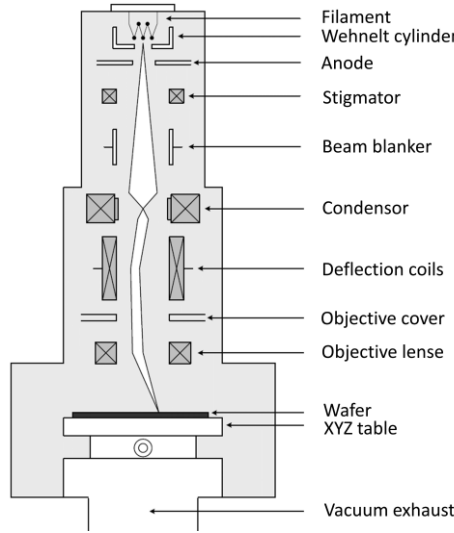
Figure 39. Schematic illustration of an EBL system [121].

2.4 *Physical vapor deposition techniques*

Physical vapor deposition (PVD) is a technique which can be used to produce thin-film layers and coatings, typically in the range of nanometers to a few micrometers. Deposited films can span a range of chemical compositions based on the source material which has the properties of conductive, dielectric, or insulating layers. The most common PVD processes are sputtering and evaporation, in which the resulting vapor phase is subsequently deposited onto the desired substrate through a condensation mechanism [125]. Figure 40 shows the fundamental principle of these techniques and also, the slight structural differences in resulting layers which can be achieved. Moreover, this can give us an idea of which technique might be suitable for use in the various phases of fabrication processes, specifically for the lift-off process (described in more details in 2.6).
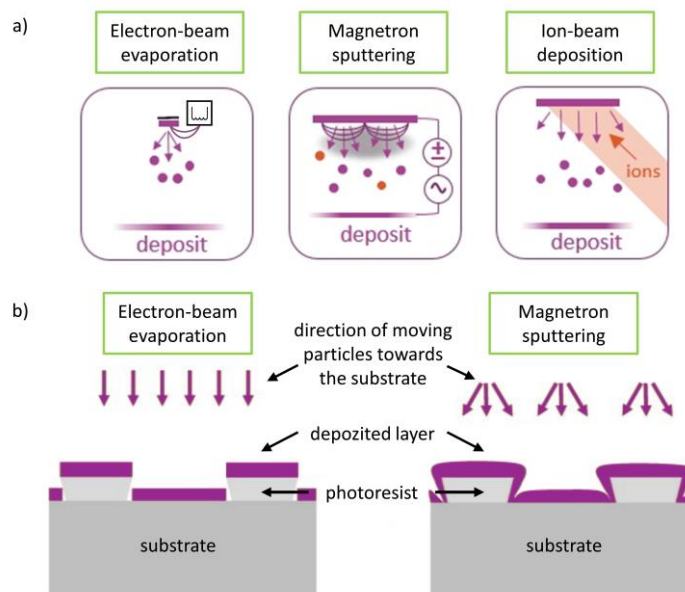
Figure 40. Schematic illustration: a) physical vapor deposition techniques, b) differences between E-beam evaporation and magnetron sputtered layer. Adopted from [126].

2.4.1   Ion-beam-assisted deposition and magnetron sputtering

Sputtering is a plasma-assisted technique that creates vapor from the source target through bombardment with accelerated gaseous ions; typically Argon is used. The ejected material diffuses to and collects on the surface of the wafer, as shown in Figure 40a. In this work, the deposition of conductive and dielectric layers was performed using BESTEC – High vacuum sputtering system (magnetron) and BESTEC – Ultra-high vacuum sputtering system (ion-beam assisted deposition, IBAD) systems. The primary advantages of sputtering compared to evaporation are improved step coverage and ease of deposition of alloys and compounds. Some compounds may also be deposited by reactively sputtering the target with a dilute mixture of argon and reactive species, such as oxygen. [127]

2.4.2   E-beam evaporation

Evaporation is a deposition technique that relies on vaporization of source material by heating the material using appropriate methods in a vacuum. The material to be evaporated is heated in a crucible. Then, the vapor of the material travels in a straight line to the substrates. Crucible heating can be done resistively, inductively, or with a beam of electrons. BESTEC – UHV Evaporation system was used for the creation of conductive layers in this work. The primary problems with evaporation include step coverage, alloy formation, and, in electron-beam systems, radiation damage. [125,127,128]

2.5   *Chemical vapor deposition techniques*

Chemical vapor deposition (CVD) is a technique which can be used to deposit materials in various form including monocrystalline, polycrystalline, amorphous and epitaxial. The differences between PVD and CVD techniques is that the CVD process involves depositing a solid material from a gaseous phase which is achieved through a chemical reaction between volatile precursors and the surface of the materials to be coated. When the precursor gases pass over the surface of the heated substrate, the resulting chemical reaction forms a solid phase which is deposited onto the substrate. The substrate temperature is crucial and can influence the incidence of different reactions. [127,128]

2.5.1   Atomic layer deposition

Atomic layer deposition (ALD) is a subclass of CVD thin-film deposition method in which a film is grown on a substrate by exposing its surface to other gaseous species, generally called as precursors. In contrast to traditional chemical vapor deposition, the precursors are never present simultaneously in the reactor, but they are inserted as a series of sequential, non-overlapping pulses. During one cycle, the precursor is pulsed into a chamber for a designated amount of time to allow the precursor to completely react with the substrate surface through a self-limiting process that leaves no more than one monolayer at the surface. Subsequently, the chamber is purged with an inert carrier gas to remove any unreacted precursor or reaction by-

products, typically N_2 or Ar. By varying the number of cycles, it is possible to grow materials uniformly in the composition of the films at the atomic level. [129,130]

Atomic layer deposition system Ultratech/Cambridge Nanotech Fiji 200 was used to deposit high-quality dielectric layers with a uniform surface. The equipment is enabled to use a variety of materials (precursors) to create metal-oxides and nitrides thin layers such as HfO_2, SiO_2 or AlN. For this work, HfO_2 and SiO_2 layers were used primarily to provide insulation layers between the top electrodes and the gate in the FET structures.

2.5.2   Aerosol-assisted chemical vapor deposition – NWs fabrication

Aerosol-assisted chemical vapor deposition (AACVD) is a variant of conventional CVD process, in which aerosol droplets transport a liquid precursor solution (with the aid of an inert or reactive carrier gases) to the reaction zone at atmospheric pressure, where the solvent goes rapid evaporation and/or decomposition, forming the precursor vapor at relatively high temperature. This technique is advantageous when the precursors for conventional CVD are non-volatile or thermally unstable, as in AACVD the requirement for volatility and thermal stability of precursors become less stringent [131]. AACVD has been used previously as a route for the formation of multi-component and straightforward metal oxide films and coatings, for instance, TiO_2, WO_3, SnO_2, ITO, $LiTaO_3$, $NiO-Al_2O_3$. Recently this technique has shown the possibility to produce columnar metal oxide structures via a vapor-solid mechanism at low temperatures (400 – 600 ºC) compared to those often used in conventional CVD (1000 ºC or more), making this technique compatible with device fabrication technology. [132]

The AACVD materials, synthesized to be used in this thesis, were processes in a laboratory AACVD setup consisting on a home-made stainless-steel cylindrical reaction cell with an internal volume of ~7,000 mm^3 (diameter: 30 mm, height: 10 mm) with integrated heaters that allow for reaching temperatures up to 600 ºC. The system was also provided of a piezoelectric ultrasonic atomized (Johnson Matthey, Liquifog) operated at 1.6MHz to generate an aerosol of the liquid precursor solution and mass flow and temperature controllers, as shown in the scheme in Figure 41.
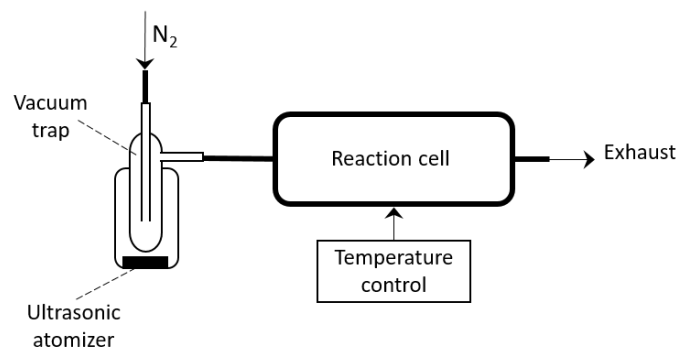
Figure 41. Schematic illustration of AACVD deposition system.

2.6 Etching techniques

Once the photoresist pattern (mask) is transferred on the surface of a wafer, the following step include either deposition (lift-off) or etching over a mask (etch-back) on a substrate surface to fabricate the structure's pattern in a place where the mask is not present, the surface to be patterned stays uncovered respectively. The deposition over the mask is called a lift-off process which was primarily developed to avoid the need for etching altogether. It is still popular as an alternative technique for patterning of materials difficult to etch. Such an example of the lift-off process can be seen above in Figure 40, where it is noticed that evaporation is a better technique for deposition than sputtering, which fails in covering high aspect ratio features. The disadvantages of using lift-off process is connected with the high possibility of material redepositions (resist sidewalls); an issue that is well-known and reported in the literature [133,134].

In contrast to lift-off in the etch-back process a layer is firstly deposited to be etched. This layer is etched subsequently through a mask as described in [95]. The etching processes can be divided into wet and dry etching or chemical and physical etching. Depending on the method, the etching is called isotropic when it occurs in both lateral and vertical direction. On the other hand, if the etching is ongoing only in one direction, it is called anisotropic. The etch rate, which has a dimension of thickness per unit time, commonly hundreds or thousands of angstroms per minute (Å/min), is one of the key parameters in the etching process. Another important parameter to be considered during the etching process is the selectivity, which is given by the ratio of the etch rates of various materials exposed to the etchant, typically the photoresist and the underlying layer to be etched.

2.6.1 Wet etching procedures

Wet etching is a purely chemical process that can be highly selective. In principle, it is the conversion of solid materials into liquid compounds using chemical solution. However, notice that in most of the wet etch processes, the layer to be etched is not directly soluble in the etchant, so usually, it is necessary to use a chemical reaction to change the material from solid to liquid or gas. Although, this process is still used in some specific areas, the wet etching struggle from serious drawbacks as its lack of anisotropy, poor process control, significant amounts of chemical waste and many others. For that reason, it continues to be used in noncritical operations. In a practical matter, this process is not regarded to be suitable for structures smaller than 2 μm. [127]

In this work, following wet etch procedures were performed by simple immersion in a laboratory beaker:

- **Au etching** – etching of the microelectrodes with width down to 2 μm,

- **NiCr and Ti etching** – etching of the adhesion layer between gold electrodes and substrate (silicon wafer) or underlying layer (SiO_2 dielectric layer),

- **SiO₂ and HfO₂ etching** – etching procedure of contact pads area serving for wire bonds, which was covered by a double stack dielectric layer of SiO_2 and HfO_2. During this fabrication step, pad areas were "opened" in order the subsequent deposition of Au/Ti conductive layer providing intermetallic interconnection.

2.6.2 Reactive-ion etching

As can be seen from the name, reactive-ion etching (RIE), sometimes called ion-assisted etching, is a chemical-physical dry etching technique in which ions are not only the etching species in this process. In detail, inside the process chamber, the surface of the substrate is exposed to an incident flux of high-energy ions, radicals, electrons, and neutrals (plasma), which is initialized by applying a strong electromagnetic field with high frequency. Thus substrate material is etched by physical etching related to the accelerated ion flux accompanied by the chemical reaction with the surface depending on both ion flux and the radical flux. RIE has good selectivity, etch rate, and unlike wet etching, reproducibility can be controlled better. Also, due to the almost perpendicular direction of reactive ionic species, the resulting etch profile is mostly very anisotropic. [127,135]

Oxford Plasma NGP-80 processing tool was used due to the need for uniform anisotropic etching technique for the structures under 1 μm. This equipment uses radio frequency (RF) power to create a plasma inside the process chamber. The resulting etch process can be varied by altering the plasma conditions, the source gas for the plasma, the vacuum pressure, the substrate temperature, and various other parameters. During this work, the equipment was used for the etching of SiO_2 layers and remaining Ti (titanium) layers after the electrodes etching. This followed-up chemical-physical process of Ti residues served to assure that no conductance will appear in between the electrodes and validate the etching process. Figure 42 shows a schematic illustration of a conventional RIE reactor.
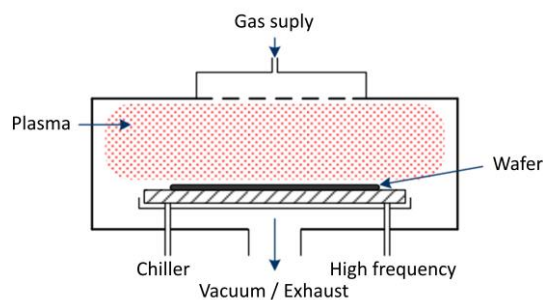
Figure 42. Schematic illustration of the reactive ion etching reactor. [135]

2.6.3 Ion-beam etching

Ion-beam etching (IBE), sometimes referred to as ion milling, involves no chemical reaction with the etch material. It is strictly physical dry etching process analogous to sputtering. In principle, argon ions are accelerated in the system of grids by a strong vertical electric field which leads to the mechanical impinging of substrate material to be etched. The ions are primary etching species in this process. The chamber pressure is so low that atomic collisions

are extremely unlikely. The wafer can be held perpendicular or tilted into the ion beam. The selectivity is low because there is no differentiation of the individual layers, but the etch progress is highly anisotropic. [127,135]

SCIA coat/mill 200 system was helpful for applications in which RIE was not successful, or it was not recommended to use. Typically, etching of gold (Au) and titanium (Ti) layers, especially nanoelectrodes, were performed with this equipment in order to achieve a highly anisotropic etch profile of fabricated structures. For instance, tilting and rotating substrate stage allows altering ion angle of incidence, which results in substantial improvement of the etch profile and avoid material redeposition. Another advantage of this tool is the presence of endpoint control with SIMS (secondary ion mass spectroscopy) to monitor sputtered material species, allowing etching to be stopped at specific layers. A schematic illustration of such a device is shown in Figure 43.
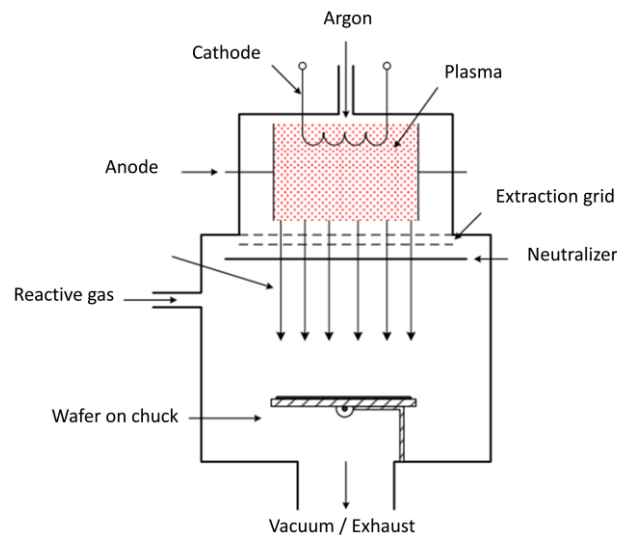
Figure 43. Schematic illustration of an ion-beam etching reactor. [135]

2.7 *Measurement, characterization and inspection techniques*

This section presentes the techniques that were used to characterize the samples after each fabrication step. These techniques were useful to create a standard procedure methodology for the fabrication process among various devices designed to measure or characterize the required parameters of the testing structure. To be specific, every fabrication step requires end process inspection with results evaluation. For instance, the resulting pattern of a metal layer after selective etching can be evaluated by optical inspection, which is, in principle, a simple method with the possibility to recognize etched areas, but it does not show the thickness of the layer already etched, or if the conductive paths (metal electrodes) are not in short-circuit state. The techniques that help to characterize the parameters mention above are methods such as surface profilometry (thickness or depth measurement) and electrical characterization (resistance measurement). Therefore, to validate each fabrication step it was necessary to develop protocols of characterization after each process. Below are listed the techniques employed for inspection of the process.

2.7.1 Surface contact profilometry of objects down to 1 μm

This method is based on measuring a surface profile by moving a diamond stylus laterally across the surface at a specified contact force. Its vertical displacement gives the result as a function of distance (position). Brucker Dektak XT equipped with diamond stylus radius from 0.7 to 12.5 μm was used for the measurements of structures profiles with dimensions down to 1 μm. Profiles, for example, after the resist development, an etching process or depositions of thin films, were performed in the basic 2D (two dimensions) single scan mode. Besides this mode, the profilometer provides the ability to measure the surface morphology along an extensive area of a sample by 3D analysis, which was used in the characterization of test structures for estimation of exposure parameters (dose and critical dimension test).

2.7.2 Scanning probe microscopy of objects smaller than 1 μm

Scanning probe microscopy (SPM) is a similar technique to 3D scanning profilometry with the difference that it is capable of imaging surface morphology at the atomic level. Instead of the diamond stylus is a sharp tip (cantilever), typically from silicon nitride. However, the nature of the cantilever depends primarily on selected SPM method but also on the specimen topography and its surface properties (roughness, material composition and so forth).

Bruker Dimension Icon is an atomic force microscope (AFM), with which was possible to imaging sample topography at high resolution in nanoscale. Since a maximal scan range is 90 μm^2, this equipment was mainly used to display small areas, which could not be scanned by profilometer regarding the limitation of the stylus radius. The radius of the AFM tip is usually in the order of units up to tens of nm. Also, the microscope is equipped with proprietary ScanAsyst$^®$ automatic image optimization feature, which eliminates the need to manipulate with parameter settings and provides easier and faster achievement of consistent results.

2.7.3 Spectroscopic reflectometry for thickness measurement of thin films

There are several techniques to measure the thickness of thin-film layers. One of the common ways is using their optical properties results from reflection and interference. Spectroscopic reflectometry utilizes the reflectance method in which the amount of reflected light from a thin film is examined over a range of wavelengths with the incident light normal to the sample surface.

Thin films reflectometry system Ocean optics NanoCalc 2000 allows analyzing the thickness of optical layers from 10 nm to 250 μm with a resolution of 0.1 nm, approximately. This tool is suitable for on-line thickness measurement and removal rate application of the various materials such as oxides, silicon nitrides, photoresist, and many other coatings. In this work, NanoCalc 2000 was used primarily for the measurement of SiO_2 layer thickness, for example after the deposition (ALD) or etching (IBE) procedure.

2.7.4   Optical microscopy inspection – microscale imaging

An optical microscope uses visible light and system of lenses to magnify images of small objects. In fabrication, this tool was commonly used for imaging the process results after or before each fabrication step. It is simple and one of the core inspection technique supposed to be used as a first to reveal the process errors, e.g., unsatisfactory lithography, or etching.

Carl-Zeiss Axion Imager is an optical microscope offers a wide range of magnification from 5x up to 100x, darkfield vision usable, for example, for enhanced sidewalls detection made during redeposition in lift-off process, and many other features. With this microscope, it was possible to see structures with size hundreds of micrometers, but also structures around 1 μm were visible.

2.7.5   Scanning electron microscopy inspection – nanoscale imaging and analysis

Scanning electron microscope (SEM) is a type of microscope where accelerated focused electron beam impinging on the surface of specimen results in a cascade of collisions which, in turn, generates a variety of signals, mostly secondary (SE) and backscattered (BSE) electrons emitted from the area of interest. The sample image is formed by detecting these electrons over the scanning area. A wide range of detectors can be integrated into the chamber of SEM, which can be utilized for imaging of the sample surface, or they can either serve for analytical purpose. Apart from the secondary and backscattered electrons generated from the electron-beam interaction with the sample, there are more signals attendant, which can be detected and measured like photoemission in the form of X-ray, cathodoluminescence, and others.

Various electron microscope types were used in this work, mostly for imaging structures with the ultra-high resolution in nanometers. As was stated, with Carl-Zeiss Gemini electron microscope was performed electron-beam lithography as well as a screening of the results of the lithography and other fabrication processes, for instance, nanoelectrodes made by ion-beam etching, mainly for the reason that the stage holder is capable of holding wafers up to 6-inch size. JEOL JXA-8230 electron probe microanalyzer was used during the internship at the University of Barcelona as an imaging tool to evaluate the NWs alignment process. The most common SEM tool in this work was Tescan FE Mira II-LMU equipped with energy dispersive X-ray (EDX) and wavelength dispersive X-ray (WDX) detectors, which can provide elemental composition analysis and identify individual elements of the sample. Apart from these analyses, this microscope was also used for imaging of NWs and all synthesis processes which needed screening with nanometer resolution.

2.7.6   Electrical characterization and measurements

Electrical characterization and other electrical measurements related to the fabrication process were performed with modular probe stations system Cascade Microtech MPS150 connected to parameter analyzer Keithley 4200-SCS. This system served to prove zero conductivity between electrode contacts and for electrical characterization of NWs properties

(I-V curves). Since the probe station is equipped with four-probe terminals, the 4-wire sensing to measure very high resistance is enabled.

2.8   Packaging techniques

After the fabrication of the arrays of electrodes the packaging of the die or chips took place. Firstly, the whole wafer with fabricated structures was cut into separated pieces, so-called chips or dies, so the chips could be used directly for various types of operations using a probe station, or be mechanically mounted and electrically interconnected to the package (a chip carrier/support). While the direct usage of the probe station can suffer from, for example, a limited amount of a probe positioners, the integration of the "chip on the package" offers numbers of advantages, e.g., each contact pad on-chip can be individually interconnected with package pin without any further interventions, the package with chip is portable and can be easier connected with other devices providing further advanced applications or examination suitable for gas sensing. Below are described the two process employed for dicing and bonding the chips.

2.8.1   Wafer dicing process

The process by which the chip is separated from a wafer is called wafer dicing. This fabrication step can be done by several techniques, the most common techniques include mechanical sawing and laser cutting. Both methods were used in this work. In mechanical sawing an extremely thin diamond blade is enabled to cut only whole substrates (e.g., silicon wafers, glass), whereas in laser cutting, a range of infrared, visible and ultraviolet laser sources give fast machining of a wide range of materials, but also various size and shapes.

Compact laser micromachining system Oxford Lasers A-series was used to cut silicon wafers with and without structures, and alumina (Al_2O_3) ceramic substrates, e.g., heater elements. A part of the work was also done using trimming laser Aurel ALS300.

2.8.2   Wire bonding – electrical interconnection from chip to package

As was stated, when chips are separated from the wafer, their contact pads can be either directly contacted by probes using metallic needles. Another option is to make the electrical interconnection with the package by wire bonding, which is a technique that might be considered as kind of a micro-welding. The methods are divided into three main concepts: (1) ultrasonic, (2) thermo-compression, or their combination, (3) thermo-sonic bonding. The materials of the wire are usually gold, aluminum, silver or copper with diameters from 15 μm up to hundreds of μm, depending on the application.

TPT HB16 thermo-sonic wire bonder for wedge and ball bonding provided electrical interconnection between fabricated chips, containing a system of electrodes and other functional elements, and package, typically TO-8 type with twelve pin terminals. Besides the chip/package interconnection, the wire bonding technique was also used for interconnection of

individual parts on a chip-level, e.g., the interconnection of grounding electrodes, gate electrodes and so forth. The equipment was used in a wedge mode with 25 μm thick gold wire.

2.8.3 Nanowires processing techniques and assembly using dielectrophoresis

NWs removal process

As-deposited NWs (mostly WO_3) produced by AACVD were removed from the silicon substrate and suspended in DEMI water using sonication tool Bandelin SONOREX® Digital 10P, which has the option to adjust the intensity of the ultrasound preventing damages of the structures, in particular, avoiding the shortening of NW length. A contact-angle measurement station SEO Phoenix 300 was used to adjust the dropping of the suspended NWs, instead of using standard laboratory pipette, which does not allow controlled positioning. The contact-angle measurement station facilitated the alignment of the syringe with the electrode system by means of CCD cameras.

NWs assembly process

Dielectrophoresis is a very versatile methodology, which utilizes an inhomogeneous electric field (AC voltage), typically formed between a pair of planar electrodes, to manipulate the placement of NWs via interaction with their induced dipoles in order to provide NW-electrodes interconnection. [136] Additionally, polarizability is a measure of the ability of a material to respond to an applied electric field and to produce charges at interfaces. A difference in charge density on either side of a NW in an applied non-uniform electric field gives rise to an effective or induced dipole across the particle. NWs move toward regions of highest electric field strength if the polarizability of the NWs is higher than that of the dispersed medium; otherwise, they are repelled. At low frequencies, free charge movement is the dominant mechanism responsible for charging the interface, while the polarization of bound charges (permittivity) dominates at high frequencies. This method was selected as an essential technique to build a gas sensor based on NWs since it best suits the requirement for NW integration to prefabricated electrode systems. [137]

Signal waveform generator Agilent 33220A was employed to integrate NWs with the electrode system. The generator was used in settings with a connected probe station or with an indirect connection through a printed circuit board (PCB) designed for the TO-8 package with a chip.

3 First chip generation: Microelectrode array system for nanowires integration using dielectrophoresis technique

This chapter presents the first generation of chips focused to provide a platform of electrode arrays (system) for selective integration of various functional NWs arranged in parallel. This with the aim to obtain arrays of gas sensing elements based on single NWs. To achieve this goal, it was necessary to select the methods for the whole fabrication and adjust the parameters of each individual procedure to optimize the processes. To this purpose the attention was focused on four main topics: (1) deposition of WO_3 NWs and their dimensions, (2) NWs removal process, (3) design and fabrication of microelectrode array, and (4) integration of the NWs into microelectrode array systems.

Briefly, the following technological steps were realized for the implementation of this work. Highly single-crystalline WO_3 NWs were fabricated using AACVD deposition technique based on a methodology developed previously at FEEC. More details of the material characterization and gas-sensing properties of similar structures are already published in [138-140]. Since the drop-coating method was chosen to re-deposit the NWs onto the electrode array, their dimension (e.g., the length), after the removing from a basic substrate into the solution, stayed unknown. Therefore, the NWs removal process was adjusted using sonication forces in liquid medium (mechanically), as described in [137]. The adjustment was particularly focused on choosing the appropriate solvents to avoid possible chemical damage and the change of material properties. This process also took into account the appropriate times of sonication and intensities used in order not to diminish drastically the NWs length. In parallel, several microelectrode arrays with various testing structures were fabricated using silicon substrates and related fabrication techniques, including direct-write lithography, sputtering, or wet etching. The electrode arrays were designed based on several factors, particularly the NWs dimensions, limits of fabrication (e.g., lithography, etching) processes, and follow up processing and characterization (e.g., measurement) and techniques to be used during gas testing. dielectrophoresis (DEP) was found the most convenient method for the integration and connection of NWs in between the electrodes. This method employs an alternating electric field, which forces the NWs to move toward the electrodes with subsequent NWs assemble over the electrodes gap, as was described in [141,142].

Overall, this work was the first practical introduction to the topic and its issues related to the electrode arrays based on NWs. After the development of the first chip generation, it was acquired a greater awareness of all used methods, and their pros and cons for the application targeted. The experience gained during the fabrication process was further used for the fabrication of second chip generation of gas sensing elements based on nanoelectrode arrays with single NWs interconnection.

3.1 Experimental and methods

This section is dedicated to describing the methods used to implement the three core processes for the fabrication of first chip generation, namely, NWs removal from basic substrate, on-chip integration (redeposition) of NWs via DEP forces, and design and fabrication of a test chip containing electrode arrays with variable dimensions and shapes.

3.1.1 Nanowires preparation, removal and redeposition for evaluation of dimensional properties

As stated in 2.5.2, AACVD is a variant of traditional CVD in which a precursor solution is transported to the substrate in the form of an aerosol. With this method is possible to produce nanostructured MOX (e.g. WO_3) by controlling the degree of homogenous and heterogeneous gas-phase reaction via different process conditions such as the deposition temperature, carrier solvents, and concentration of reactive species. Tungsten oxide nanowires were grown on tiny silicon tiles (1x1 cm) employing the AACVD system described previously in [132]. Figure 44 presents a photograph of the system and its parts installed in a fume hood.
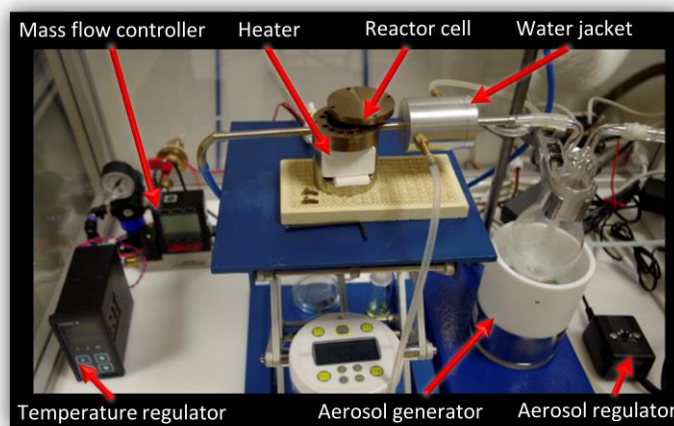
Figure 44. Illustration of AACVD system for production of MOX nanowires.

Briefly, the conditions to grow tungsten oxide nanowires from $W(CO)_6$ via AACVD involved a screening of deposition temperatures, solvents, and solution concentrations. The optimal condition for the growth of nanowires was found at 390 °C using a solution of methanol (5 ml, Penta, ≥99.8%) and tungsten hexacarbonyl ($W(CO)_6$, 20 mg, Sigma-Aldrich, ≥97 %). A commercial piezoelectric ultrasonic atomizer was used to generate the aerosol from the methanolic solution of $W(CO)_6$, and the aerosol droplets were transported to the heated substrate using a controlled nitrogen gas flow (200 sccm). The entire volume of solution was transported in about 70 minutes. In this work, apart from pristine WO_3 NWs, it was also grown NWs functionalized with platinum NPs. These modified structures were synthesized in a single-step co-deposition via AACVD deposition using hexachloroplatinic acid hydrate ($H_2PtCl_6 \cdot x$ H_2O) (Sigma–Aldrich, 99.9%), more details of the synthesis process are described in [143]. Figure 45 displays SEM images of the WO_3 NWs grown on a basic substrate carrier, which was silicon tile about 1x1 cm. However, it is possible to use other substrates such as glass, or even flexible substrate platform (e.g., polyimide foil). [144]
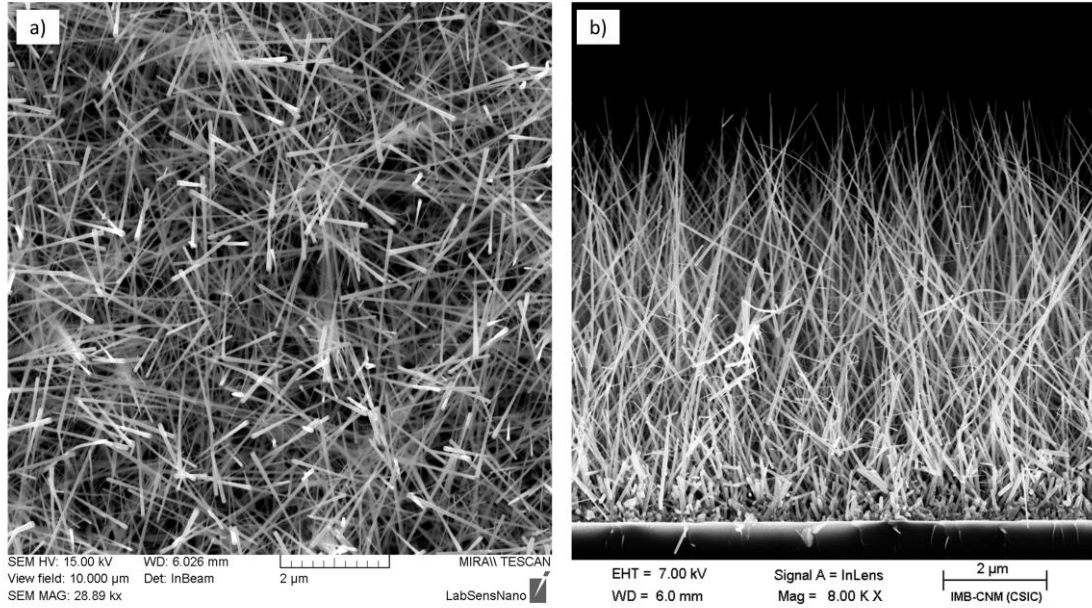
Figure 45. Deposited WO₃ nanowires grown by AACVD on silicon substrate tile 1x1 cm: a) top view, b) cross-section view.

In Figure 45b it is observed a cross-section view of as-deposited NWs, which indicates that NWs length is about 10 μm on the basic substrate. To remove the NWs for their re-deposition and DEP alignment, the substrate with NWs was immersed into a beaker with 1 ml of deionized water (with resistivity around 18 MΩ.cm⁻¹) and subsequently sonicated (Bandelin SONOREX®, Digital 10P) a 50 % power sonication for 10 sec. The use of deionized water was based on previous experience for DEP applications, in which as a polar medium with high permittivity (dielectric constant), and also lower evaporation coefficient suits better compares to other liquids, such as ethanol, or acetone. [141] The water solution containing dispersed NWs was placed into the 3 ml syringe connected to the contact angle measurement station (SEO, Phoenix 300). This equipment is suitable to apply a defined volume of the water drop. Thus, a drop (5 μl) with NWs was applied on a surface of a small silicon tile and dried on the hotplate at 80 °C. The NWs dimensions parameters were evaluated using SEM. This revealed that the NW length after sonication ranges from 3 to 12 μm approximately.

3.1.2 Design requirements of the functional blocks of the microelectrode system

The first chip generation was used to find out the behavior of dispersed NWs in the water drop during the influence of the alternating electric field, dielectrophoretic forces, respectively. Therefore, the first design contains several types of electrode arrays with various shapes. The dimensions were adjusted based on the parameters (lengths and diameters) observed in section 4.1.1. Apart of the various arrays integrated in the chip, the design of the first generation also contains incoming contacts, pads for contacting, labels, and structures to prevent the droplet from moving through the substrate. The layout of the first chip generation is designed as a function of the minimum resolution of DWL equipment, which is about 1 μm. A detailed view of the chips is described below:

- *Contact pads and side structures* are placed around the periphery of the chip, as shown in Figure 46. In total, there are twenty-four contact pads (illustrated in detail as left, right, top, and bottom side electrodes), and their size is designed quite large (500x500 µm), because an electrical connection of such a test chip with external devices (e.g., signal generator, or parameter analyzer) is provided by a probe station instead of using wire-bonding. This size is enough for easy manipulation with probes, with tips available in sizes from 25 µm or higher, respectively. Besides contact pads, there are also label marks (situated above or below the pad), which are part of the pad describing the current array modification (type). These labels are explained further.
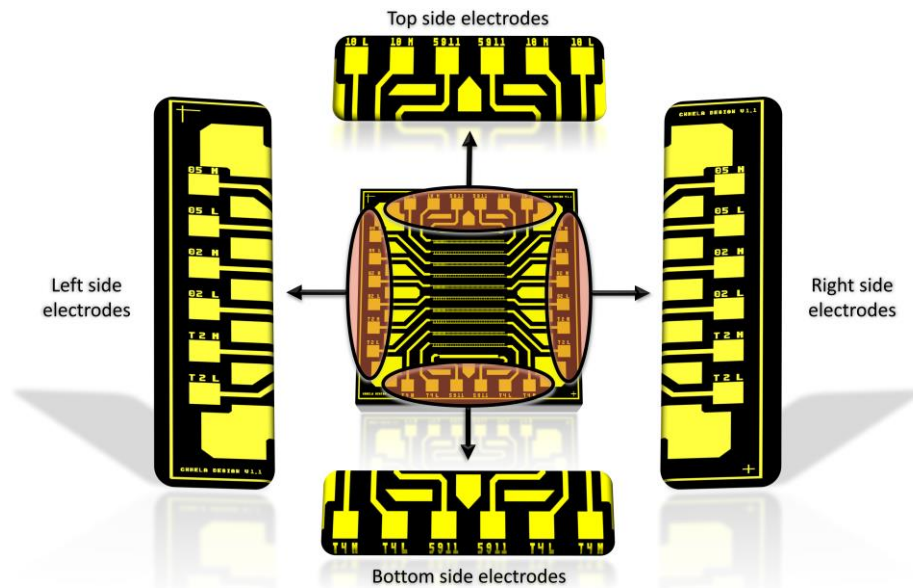
Figure 46. First chip generation layout – general view of the organization of the structures (colors: yellow – electrodes and other structures (gold layer), black – thermal oxide layer (SiO_2)).

The main microelectrode array system is situated in the center of the chip, where the alternate electric field is applied on electrodes in order to align NWs dispersed in the water drop. There are twelve electrode arrays in total, which two electrode arrays are identical (type 1), and ten are designed with different electrode end features and shapes (type 2), shown in Figure 47. Further description of the microelectrode array design and its modifications is presented in detail below:

- *Electrode array (Type 1) –* the first type comprising of a few straight horizontal electrodes with different distance between each other. A first array is taking place on the top and the second at the bottom side of the chip. One electrode array includes four straight line electrodes with a length of 2,5 mm and width 25 µm. The gaps between electrodes are designed by various dimensions, 5, 9, and 11 µm, respectively. The contact pads of these two electrode arrays are labeled according to the gap lengths as 5911. This structure served to prove the DEP and establish the first protocols for the DEP of WO_3 NWs. Design of the structure is shown in Figure 47a.

- *Electrode array (Type 2)* – the second type of the microelectrode array is made of faced electrodes (perpendicular to each other), in which individual pins ("electrode fingers") are 2 µm thick and different gap (2, 4, 5, and 10 µm). With this type of electrode array, it is possible to build the array of parallel NWs interconnections using DEP. As stated, one chip containing ten of those electrode arrays with different numbers of electrodes and end shape (e.g., in the form of round or spike, shown in Figure 47c, or different spacing between individual electrode fingers (50 and 100 µm), shown in Figure 47b), aiming to optimize the device for the dielectrophoresis processes. In this context, different spacing and shape of electrode finger end significantly affect NWs electrohydrodynamic behavior (motion trajectories) during positioning under applying of DEP forces, described in [145]. Each electrode array is connected via incoming electrodes (100 µm thick) leading to the contact pads on sides.
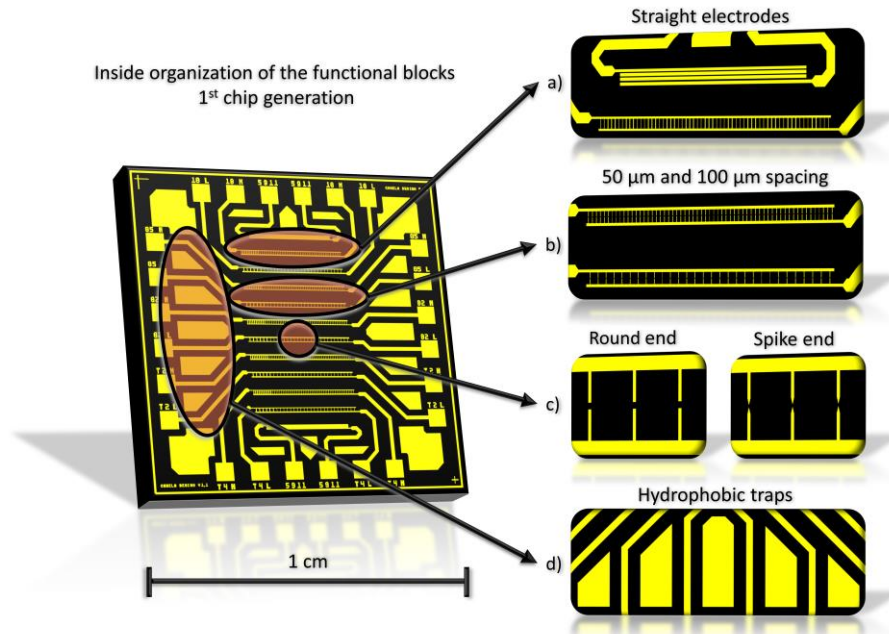
Figure 47. First chip generation – the inside organization of the functional blocks (colors: yellow – electrodes and other structures (gold layer), black – thermal oxide layer (SiO_2)): a) straight electrodes, b) 50 µm and 100 µm spacing between electrode fingers, c) round and spike shape of electrode end, d) hydrophobic traps for the drop with dispersed NWs.

- *DI water repellent structures (hydrophobic traps)* – these structures are designed to keep the water drop with dispersed NWs in the middle of the chip, in the area of microelectrode array, respectively. Hence, the structures fill the space between the incoming electrodes, see in Figure 47d. In general, the water drop, after contact with the surface, prefers to bind to oxygen bonds, which are characterized by higher surface energy (lower contact angle), than the areas with lower surface energy potential (higher contact angle), as described in [146]. Accordingly, to results presented in [147], the contact angle measured for silicon dioxide layer (black color) is lower, in contrast with the contact angle recorded for a gold layer (yellow color), which, in turn, should repel the drop against its movement through the chip surface.

- *Chip size* – the chip size in most cases depends on fabrication technology and subsequent application. This chip serves to find out a proper setting for NWs alignment using an alternate electric field, and a suitable structure for optimal DEP function, in this context the integration into the package was not necessary. Then, for easier the chip size as set to 1x1 cm (Figure 47).

- *Additional marks and labels* – the fabrication process of the first chip include only one lithography step, i.e., alignment marks for the next lithography steps were not necessary. however, there are two simple crosses. There are also chip generation labels in the opposite corners, see in Figure 46.

3.1.3   Fabrication of the microelectrode array system using wet etching process

The fabrication process of the first chip generation is described in the following paragraphs below. As stated, the chip structures (microelectrode arrays) are performed using one lithography step, deposition, and wet etching technique.

Fabrication procedure of the first chip generation

1. Substrate processing

The fabrication was performed on 4-inch silicon wafers electrically isolated with a thermal silicon dioxide layer (500 nm thick). The substrate was cleaned by DEMI water and dried with nitrogen. Before spin-coating, the substrate was left on a hotplate at 180 °C for 5 minutes, to desorb the water from cleaning (recommended).

2. Deposition of NiCr/Au conductive layer

Gold was used as a conductive layer particularly due to its high conductivity and noncorrosive properties, which allow using a liquid media (DEMI water) for the redeposition of NWs. Thus, nickel-chromium was used as an adhesive layer, between the conductive gold layer and silicon oxide dielectric layer. Both layers were sputtered by IBE deposition system (Bestec) equipped with RFICP Kaufman ion-beam source (Kaufman & Robinson – KRI®). The deposition parameters, including the deposited thickness of the layers, are described in Table 1.

Table 1. Parameters of NiCr/Au thin film layer deposition using UHV sputtering system (Kaufman).

PVD deposition – BESTEC – Ultra high vacuum sputtering system (Kaufman)		
Parameter	Material	
	NiCr	Au
Beam Voltage (V)	600	800
Beam Current (mA)	16	50
Acceleration Voltage (V)	600	400
RF Power (W)	50 (var.)	110 (var.)
Initial pressure (mbar)	$5\cdot10^{-9}$	$5\cdot10^{-9}$
Deposition pressure (mbar)	$2.2\cdot10^{-4}$	$3.1\cdot10^{-4}$
Substrate rotation (rpm)	5	5
Deposition rate ($\text{Å}\cdot\text{s}^{-1}$)	0.39	2.6
Layer thickness (nm)	20	80
Source Gasflow Ar (sccm)	2.5	3.8
Neutralization Gasflow Ar (sccm)	3	3

3. Optimization of lithography and development of a negative tone photoresist

After the deposition, the substrate was coated with an adhesion promoter (AR-300-80) and negative tone photoresist (AR-N-4340) using procedures described in the product datasheet. [117,148] Both coatings were performed using spin-coater (Labspin) with rotation speed 4000 rpm. Thus, the lithography process was carried out using the DWL system (Heidelberg Instruments, DWL 66-fs), in which a focused narrow beam transfers the pattern with specific intensity. For this reason, the parameters of the exposure could not be set from datasheet values, but they were set experimentally.

The exposure tests were done using a testing pattern, including lines and rectangles with resolution from 1 to 50 µm (see Figure 48b). The process conditions of the development step were set according to the specification from the datasheet for an immersion bath with the (AR-300-475) developer from the datasheet. Figure 48a shows the real structure after development, which reveals that a minimum resolution between 1 and 2 µm approximately was obtained. This resolution is in agreement with the required dimensions of the smallest structures designed in the first generation.
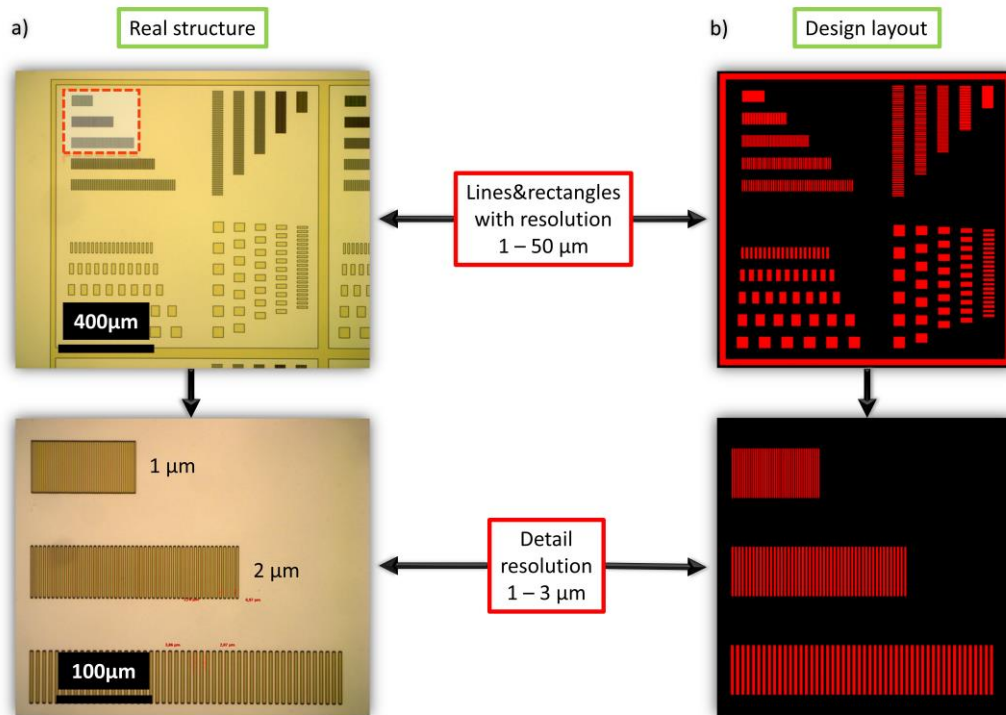
Figure 48. Resolution testing structure for negative photoresist AR-N-4340: a) real structure depicted under an optical microscope, b) design layout.

Then, the optimal conditions for DWL exposure are described in Table 2.

Table 2. Parameters of DWL exposure settings for negative tone resist AR-N-4340.

AR-N-4340 exposure settings – Heidelberg Ins. – DWL	
Parameter	**Process**
	DWL exposure
Laser power (mW)	70
Intensity (%)	55
Focus (-)	-40
Filter (%)	50

4. Wet etching of Au/NiCr conductive layer

The etching of Au/NiCr conductive layer was carried out using two wet etchants, namely, gold etching solution (Sigma-Aldrich, Gold etchant – nickel compatible), and nichrome etchant (Sigma-Aldrich, Nichrome etchant – standard) for nickel-chromium layer. [149,150] The etching process was performed in immersion bath using standard wet etching procedures, including etching, first rinse (dirty), second rinse (clean), and drying by nitrogen blow. Firstly, most of gold structures were over etched as a result of the high etching rate of the gold etchant. After diluting the gold etchant with DEMI water (ratio 1 : 2), the etching rate of gold layer (80 nm thick) was 10 Å/s^{-1}, and for nickel-chromium layer (20 nm thick) 25 Å/s^{-1}, approximately. At last, a few arrays were electrically tested on a probe station (Cascade Microtech, M150) to find out if there is no residual layer between the faced electrodes.

5. Chip dicing and substrate cleaning

After the etching, the whole wafer was spin-coated with a positive photoresist S1813 (Microposit®), and then intentionally exposed under daylight without a soft bake process. This layer was used as a protecting layer to avoid scratches and impurities during the last step. Thus, a dicing procedure was realized using ohmic trimming laser (Aurel Automation, ALS300) to divide silicon wafer to chip pieces 1x1 cm. In this context, on the substrate surface remained grooves, which then help to break the wafer along the crystallographic planes.

Finally, the wafer was cleaned from resists residual with organic compounds using PG Remover solution (Microchem) in the immersion bath heated up to 80 °C and enhanced by sonication for more than 30 minutes. To achieve maximum cleaning effect and to prevent the redeposition of resist residues, this process was repeated twice (clean and dirty solution). Then, the silicon wafer was two times rinsed in the shower with deionized water and dried with nitrogen.

3.1.4 Nanowires redeposition and integration process using dielectrophoresis

The redeposition process was carried out using a contact-angle measurement station (SEO, Phoenix 300), which is equipped with a high-resolution camera (Z-axis imaging) and automatically controlled liquid drop volume with minimum adjustment of 1 µl. An additional digital microscope (Dino-lite, digital microscope - premier) was used to imaging the chip from the top side, which allows precise placement of the droplet in a particular area (a specific array), and thus X, Y-axis positioning, respectively. Figure 49a describes individual parts of the station for NWs redeposition.

As stated in 3.1.1, WO_3 NWs were removed from the basic substrate. DEMI water containing suspended NWs was put into the syringe (shown in Figure 49a). 5 µl drop was applied on a surface of the first chip generation. Figure 49a displays the process of redeposition, in which the drop was spread over the electrode array. Also, it is seen, as already mentioned in 3.1.2, that gold retains the drop from further motion to the pads due to its hydrophobic properties.
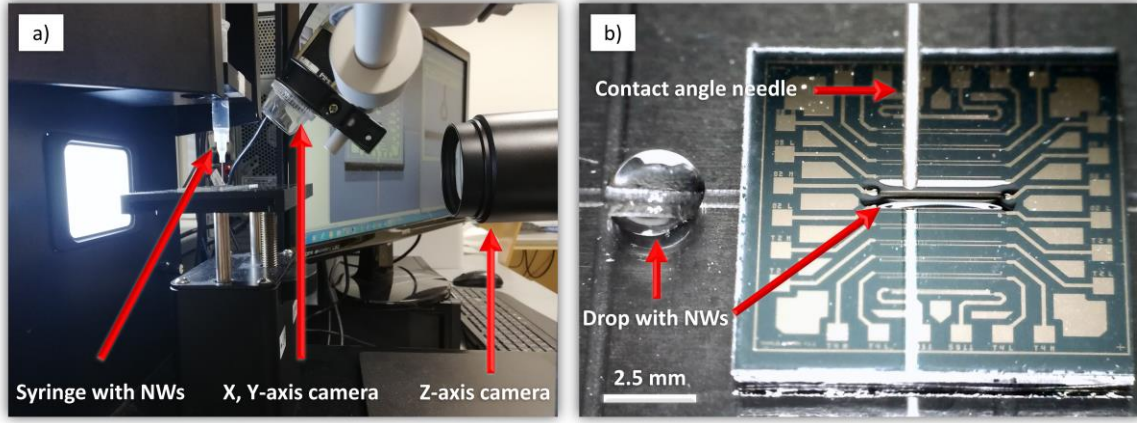
Figure 49. Nanowires redeposition process using contact angle station: a) contact angle station equipped with an additional camera (X, Y-axis), b) drop with NWs applying process (redeposition).

Consequently, the chip with a drop on it was electrically interconnected via probes (100 µm tip diameter) using the probe station (Cascade Microtech, MPS150). An alternating voltage for DEP tests was provided by a signal generator (Agilent, 33220A, 20 MHz function/arbitrary waveform generator) connected to the probe station. Thus, optimal parameters of DEP were carried out experimentally by setting different voltage and frequency values, for instance, voltage values were from 1 to 10V (peak-to-peak), frequency from 3 to 15 MHz, respectively.

3.2 Results and discussion

In this section are presented the results obtained in the fabrication of the first chip generation designed to prove the concept of using an alternating electric field for NWs alignment in parallel microelectrode arrays. The protocols developed for the removal, redeposition, and integration of NWs are also discussed.

3.2.1 Fabricated test chips with microelectrode arrays for NWs alignment

Several 4-inch silicon wafers were consumed for the fabrication of the first chip, mainly, in order to optimize lithography with negative tone resist, and wet etching parameters. Figure 50 shows a chip distribution on the 4-inch wafer, which containing 65 chips in total. The structures of each chip that were placed close to the wafer's edge (12 chips) underwent slight deformation due to a changed light scattering related to different resist thickness on the wafer's edge.
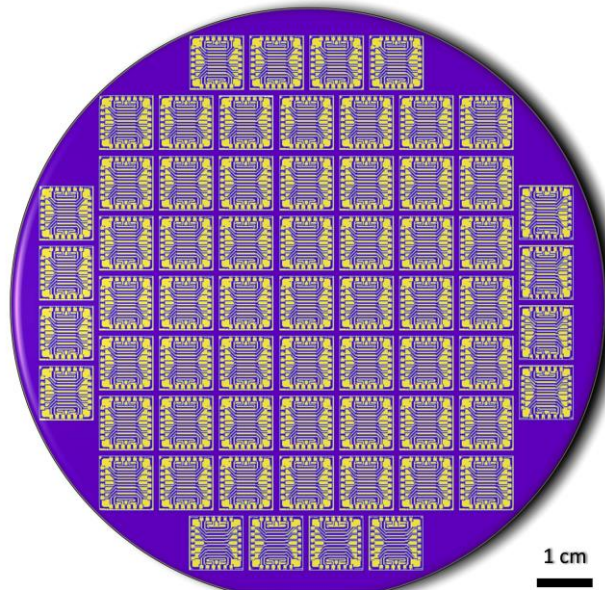
Figure 50. Illustration of 4-inch wafer with structures of the first chip generation.

The fabrication process reveals a few issues, which affect particularly the structures with the lowest resolution, e.g., faced electrodes, resulting in affecting its working ability (i.e., electrical and mechanical parameters). Indeed, the fabrication process has only one lithographic step, but due to the wet etching process and the high etching rate (as stated in 2.6.1 suffers from several drawbacks) the process control was complex, and the samples showed high isotropic etching profile. Therefore, the electrode fingers (structures around 2 µm) were completely removed, and the incoming electrodes were strongly under etched during the first gold layer etching. To improve the process, the etching solution was diluted with water, which led to a decrease in (gold) etchant concentration as well as its etching rate.

Another problem was a poor uniformity of etched structures. Although the etching rate was controlled well, the electrodes showed non-homogenous edges through the entire substrate, see Figure 51a, b. This non-homogeneity may be caused by remaining photoresist after insufficient developing of the pattern, as presented in 2.1.2, that is characteristic for immersion development. Xu, and co-workers [145] found out that electrode shape plays a major role in electric field distribution during DEP. Hence, in order to remove the residual resist, oxygen plasma treatment was performed using plasma resist stripper (Diener, Nano) for 5 minutes (600W, 0.15 mBar) before etching.
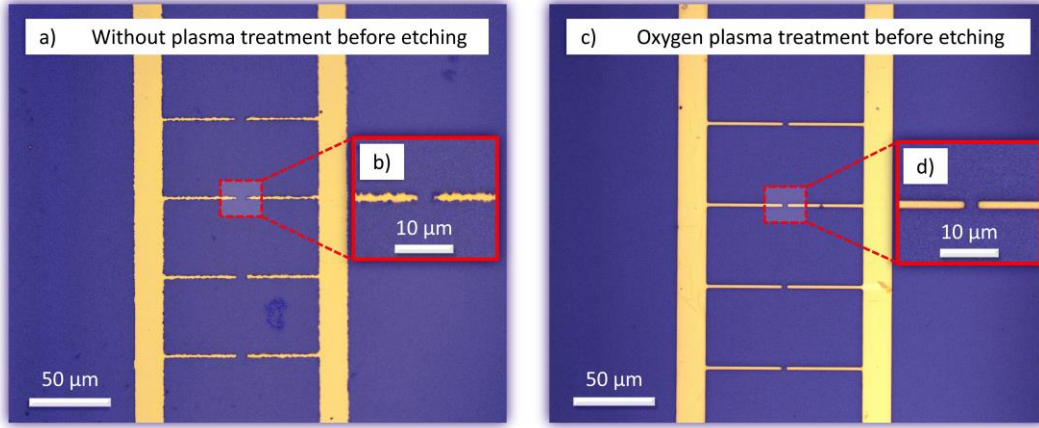
Figure 51. Optical inspection of the array with faced electrodes made by two different fabrication procedures: a) without plasma treatment after resist development (1.exposure, 2.bake, 3.development, 4.rinse, 5.wet etching – both layers), b) detail of the faced electrode (without plasma), c) oxygen plasma treatment used after resist development (1.exposure, 2.bake, 3.development, 4.rinse, 5.DESCUM, 6.wet etching – both layers), d) detail of the faced electrode (plasma-treated).

Effect of additional plasma treatment used in the fabrication process is depicted in Figure 51c, d, showing a comparison of the same microelectrode array as was presented in Figure 51a, b. Faced electrodes depicted in Figure 51d are well-shaped (uniform), as opposed to those shown in Figure 51b detail. Also, the surface treated with plasma is cleaner than that without plasma treatment. In Figure 52 it is shown an illustration of fabricated arrays with different dimensions (spacing between electrodes) and shapes (round and spike end) of faced electrode ends, which can be used for NWs integration process.
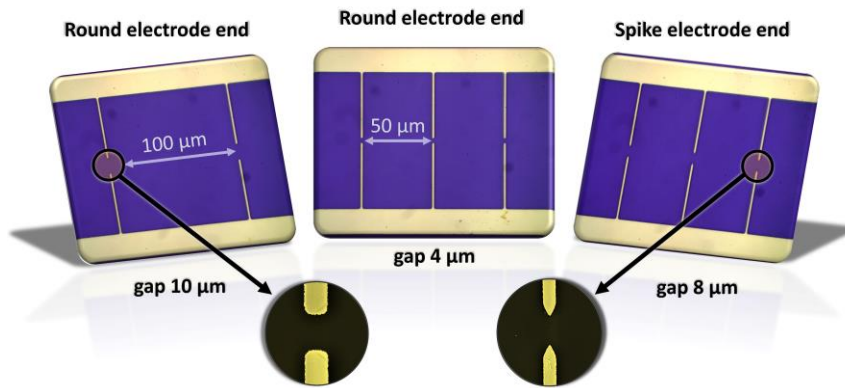
Figure 52. Illustration using optical and SEM inspection to show fabricated microelectrode arrays with faced electrodes with various dimensions and shapes.

3.2.2 Optimization of nanowires removal, redeposition and integration process

The success of the whole NWs integration process by using DEP as an aligning technique to assembly the NWs on the fabricated electrode arrays is dependent on several operations (steps). In general, there are three main procedures which were optimized (experimentally) by testing the influence of various parameters, including the influence of the sonication intensity on NWs removal process, density of dispersed NWs in a drop, or electrical parameters setting of AC signal onto NWs alignment properties. Due to the nanoscopic dimensions of NWs, results of all procedures were evaluated using SEM. The DEP process was carried out using the probe station equipped with optical microscope, which was used to observe the behavior of NWs in

the drop during applied DEP forces. Especially visible was NWs burning effect that appeared as a result of high current (applied voltage), as described further.

Thus, a first alignment procedure was done in order to find out an assembly ability of NWs using the straight electrodes with 5, 9, and 11 μm gap, as shown in Figure 53. The signal parameters were a sinusoidal peak-to-peak voltage of 2.5 V and frequency of 10 MHz. These conditions, for the first DEP experiment, were inspired by publications, in which the same liquid medium (DEMI water), as a transport and storage medium for dispersed NWs, was used. [142,151] Figure 53a shows the first DEP results obtained in which it is visible that the electrode edges are fully covered with NWs captured from the droplet. This result proves that (1) the maximum of the electric field is concentrated at the edge of electrodes (electrode (Au) – dielectric (SiO_2) interface), so-called fringing-field as described in [152], and most importantly (2) the NWs alignment process is working.

In Figure 53b is seen that the NWs alignment process yields various types of NWs interconnection (e.g., multiple NWs, single NWs, or bundles of NWs) assembled between the straight electrodes. Based on these results, it was noticed that the deposited solution (droplet) contains a high density of dispersed NWs, which, in turn, causes the drop to be filled with NWs of different dimensions (diameter, length), as observed in Figure 53b. Indeed, this is not desired, for instance, due to NWs with different dimensions, such as diameter, have different properties (electrical), which also affect their ability to move in the applied electric field (electro hydrodynamical). To avoid such numbers of dispersed NWs and their dimensions dispersion, the DEP process was adjusted further.
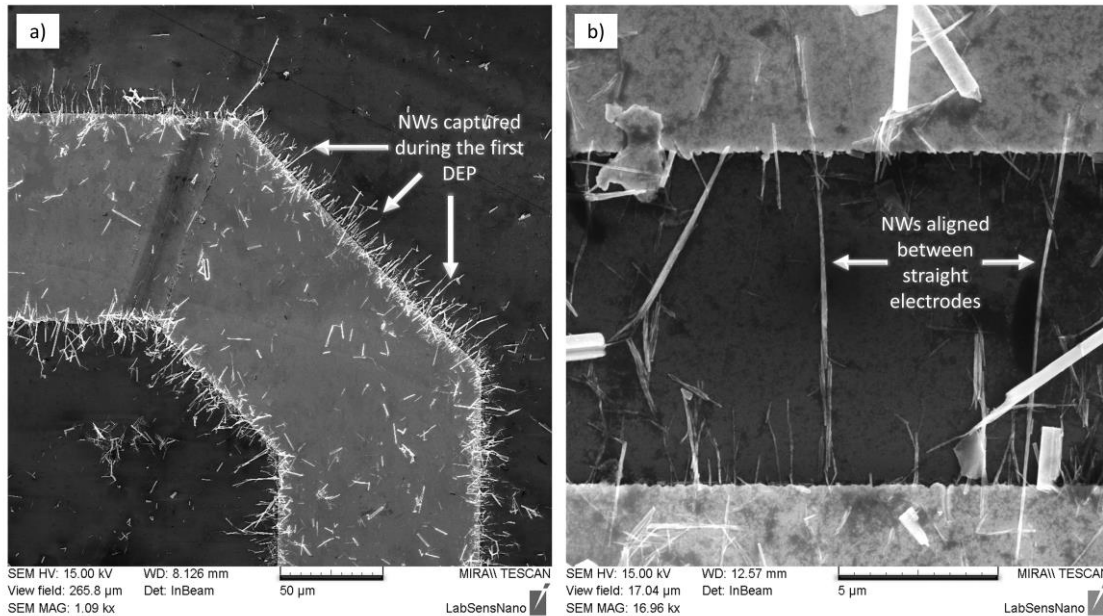
Figure 53. SEM inspection shows the results of first DEP: a) NWs captured on edges of incoming electrodes, b) NWs aligned between (5911) straight electrodes showing the gap of 11 μm.

Firstly, WO_3 NWs removal process from a basic substrate was optimized by finding an optimal intensity of the sonication in order to prevent damage of the structures, particularly avoiding the shortening of their length. To this end, several periods (2, 5, 10, and 15 seconds)

and power intensities (10, 20, 50, and 100 %) were investigated. Figure 54a depicts a surface with redeposited NWs from the solution, in which the maximum intensity of sonication (100 %) was used for 15 sec. The surface contains a high number of short NWs with length around 2.5 μm, which were most likely broken into pieces due to high sonication intensity (using these conditions there was only few NWs with lengths of 5 μm or more). On the contrary, Figure 54b shows that the optimal conditions for this process, which were found at 10 % of power intensity (35 kHz) for 5 seconds. These conditions allow the separation of NWs with maximum lengths of 10 μm approximately, consistent with the electrode gaps of fabricated electrodes.
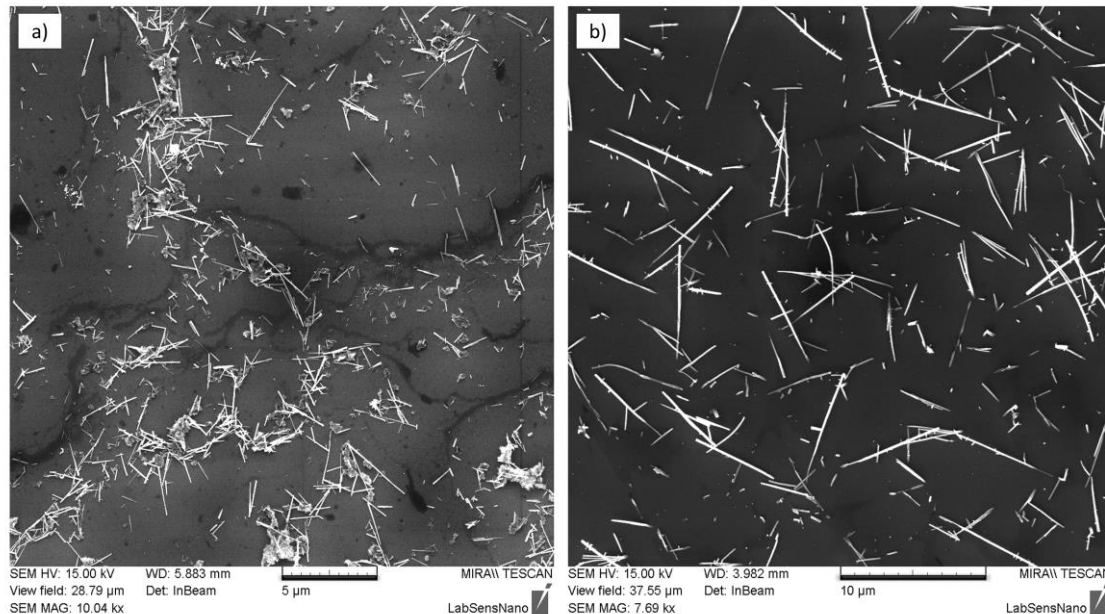
Figure 54. SEM inspection depicts WO₃ nanowires redeposited on small silicon test tiles for the evaluation of NWs removal process using various parameters: a) power = 100 % for 15 seconds, b) power = 10 % for 5 seconds.

Although the removal process was producing less NW damage after optimization, the concentration of dispersed NWs in the solution was still very high. Therefore, the removal solution, as was described in 3.1.1, was diluted with an additional 1 ml of DEMI water. Also, it was found that the basic substrate is not covered uniformly with as-deposited NWs, but the NWs with compliant dimensions (10 μm length, 100 nm diameter) are situated in the middle, and the rest of the substrate is deposited with large clusters, or other microstructures, as shown in Figure 55. To solve this issue, the substrate was cut into small pieces (1x1 mm), which also contribute to reducing the number of possibly removed NWs.
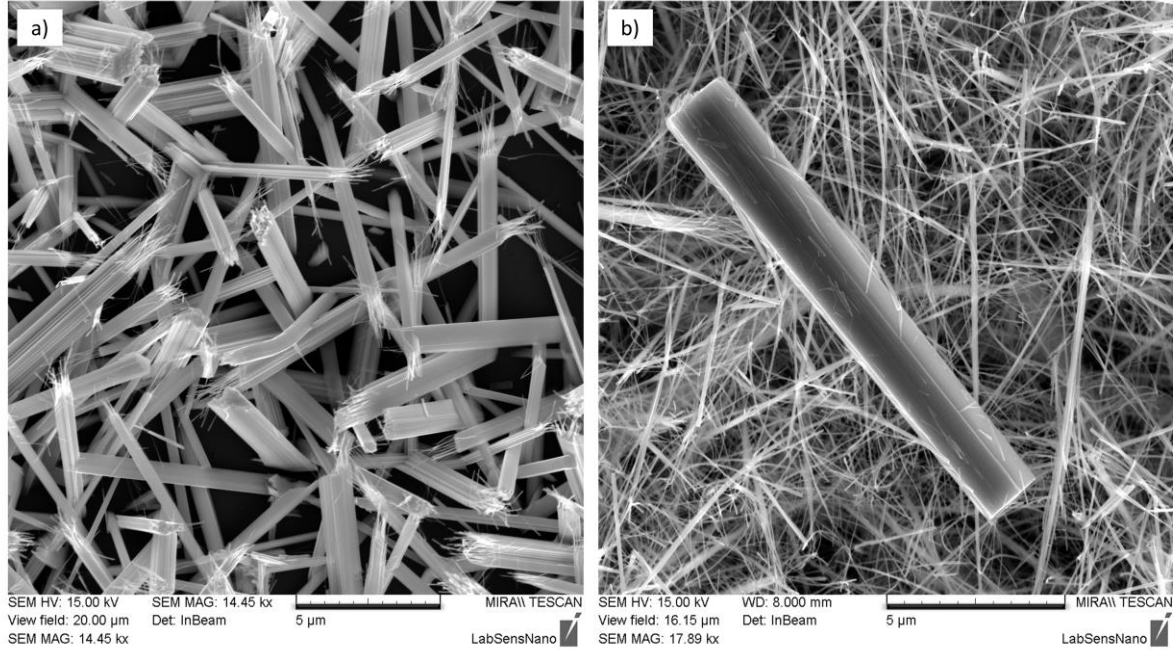
Figure 55. SEM inspection of the basic substrate (1x1 cm) containing other WO₃ structure then as-deposited NWs: a) large clusters, b) detail of large wire with microscale dimensions.

After the optimization of NWs removal, which aims to reduce the number of wires and keep their quality (dimensional parameters), the optimization of the DEP process was performed. As stated in 3.1.4, the parameters were set variable from 1 to 10 V (peak-to-peak) and frequency from 3 to 15 MHz. The DEP process was kept running at least for 2 minutes depending on the evaporation rate of the applied water drop. The results from the optimization process are presented in Table 3, in which the successful conditions for the alignment of NWs is marked by colors as well as by additional comments.

Table 3. Parameters of the DEP optimization process.

DEP optimization process – NWs alignment ability						
Parameter	**Frequency (f), sine wave (MHz)**					
Voltage, V_{pp} (V)	3 MHz	5 MHz	7 MHz	10 MHz	12 MHz	15 MHz
1	very poor	very poor	very poor	very poor	very poor	very poor
2	poor	poor	poor	poor	poor	poor
3	fair	fair	good	good	good	good
5	good	good	excellent	excellent	good	good
7	fair/critical	fair/critical	good/critical	good/critical	fair/critical	fair/critical
10	critical	critical	critical	critical	critical	critical
*(very poor: few NWs captured on electrodes, **poor**: more NWs captured (low alignment ability), **fair**: few M-NWs aligned between faced electrodes, **good**: mostly M-NWs, **excellent**: M-NWs and few S-NWs, **critical**: NWs burned); ****(S-NW** – single NWs, **M-NW** – multiple NWs)						

For example, **"*very poor*"** NWs alignment ability was observed at 1 V through a whole tested frequency range (red color), where only a few NWs were captured mostly on large electrodes (incoming electrodes), or electrode fingers, but none of them was aligned between the faced electrodes. Whereas **"*good*"** alignment (light green color) ability was monitored between 3 and 5 V almost over the entire frequency range (see in Figure 56).
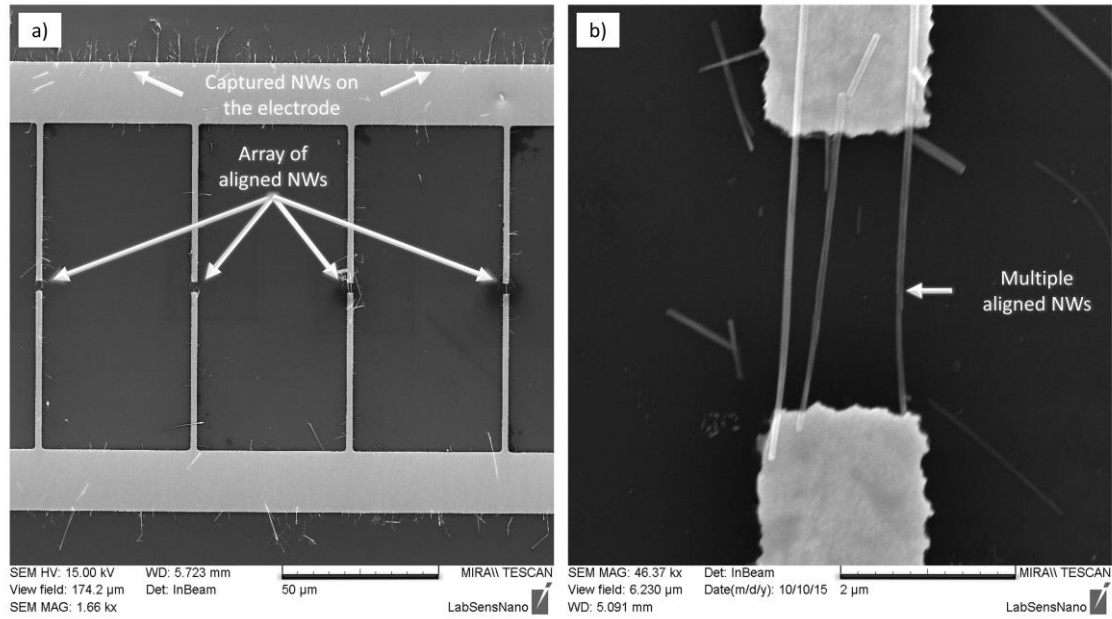
Figure 56. SEM inspection of microelectrode array with parallel aligned NWs: a) microelectrode array from a distance, b) detail of faced electrodes end with multiple aligned NWs.

On the contrary, when the voltage exceeds 5 V, most of NWs started to burn due to a higher current that results in their damage, disruption accompanied by melting, respectively. Figure 57a presents a closer view of multiple NWs interconnection together with the burnt NW (or NWs) that apparently melted (see in Figure 57c). As stated, the NWs burning effect was visible under the microscope during the DEP process, which was manifested by small bubbles in the drop between the faced electrodes. The highest applied voltage (10 V) was **"*critical*"** for the alignment process.

Figure 56a depicts a microelectrode array consisting of the parallel interconnection of multiple aligned NWs, which was achieved during the optimizing process. The detail view of multiple aligned NWs (M-NWs) is shown in Figure 56b. Despite the removal process optimization, the solution was still containing some of the broken NWs, as seen in Figure 56b and Figure 57b, which means that the process should be optimized further. Figure 57b shows an example of the NWs response to the applied electric field (3 V, 5 MHz), where NWs follow the lines of the field established between faced electrodes during the DEP.
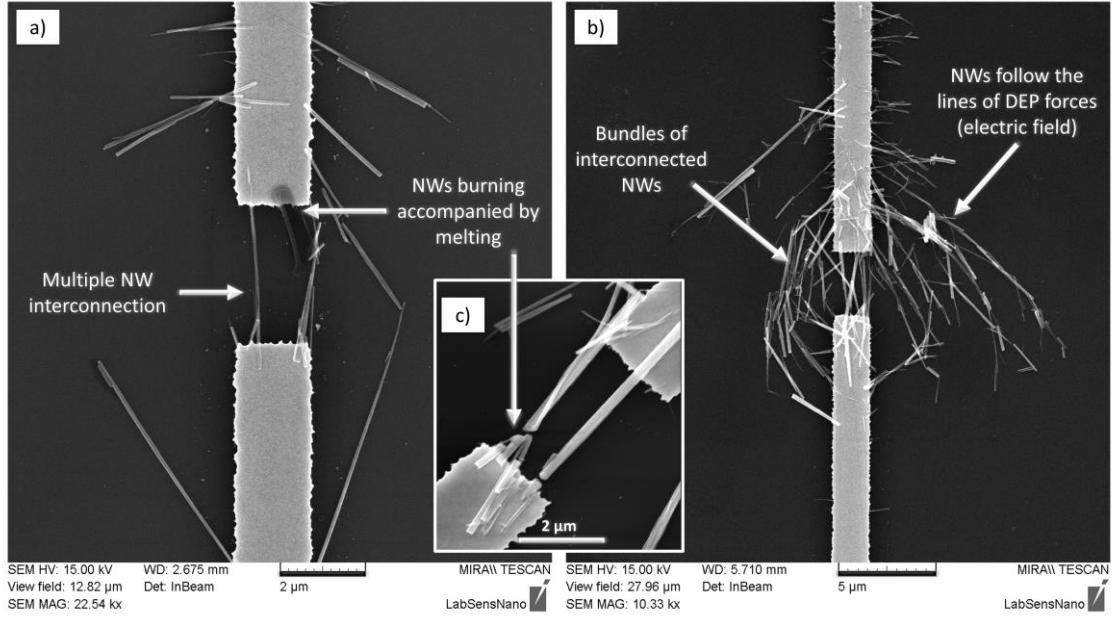
Figure 57. SEM inspection of faced electrodes after DEP process: a) multiple NWs interconnection and burned NW, b) NWs response to an applied electric field resulting in the creation of bundles of interconnected NWs, c) detail view of burned NWs.

The bundles (NWs agglomeration) mostly formed due to droplet evaporation before a nitrogen blow. It was observed that most of NWs occurred on the edge of the drop, so when the drop began to dry all NWs were pulled to the faced electrodes, where they created this agglomeration. Despite these issues, single NWs interconnections were also observed. Figure 58 presents single NWs aligned across 3 μm gap between the faced electrodes. According to Table 3, this **"excellent"** alignment ability was observed at 5 V and 7 MHz, 10 MHz respectively. Therefore, more tests were carried out in order to find out accurate frequency, which was found around 9 MHz for the WO_3 NWs.
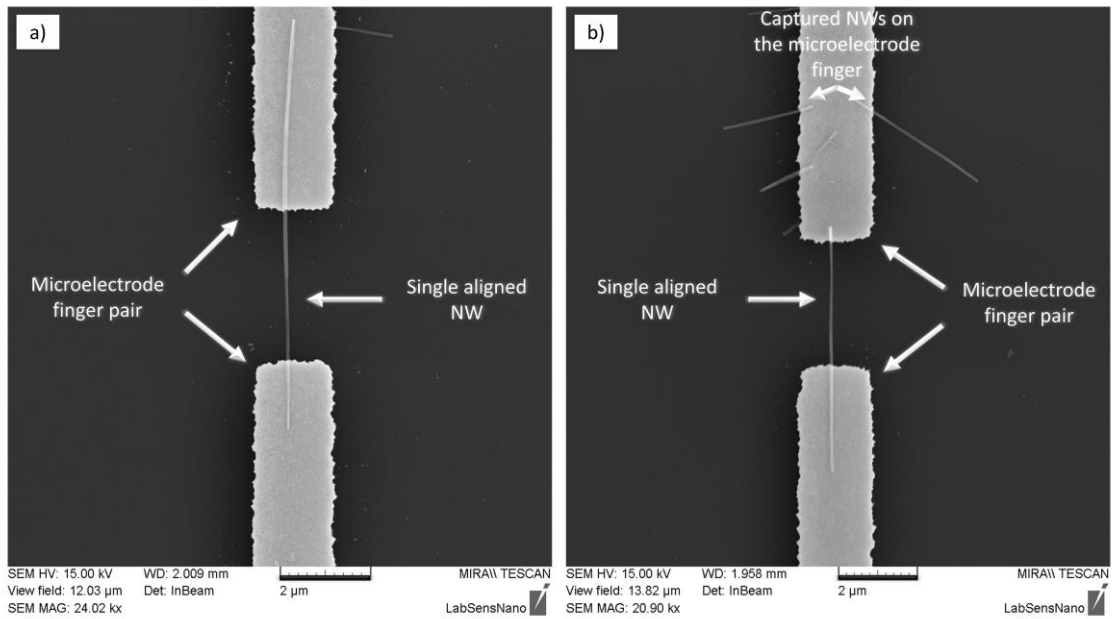
Figure 58. SEM inspection of faced electrodes with single NW interconnection: a) S-NW assembled across 3 μm gap, b) S-NW aligned across the gap with other captured NWs.

In sum, it was realized that the density of the NWs generally increased with the increase of the applied voltage potential as well as with decrease the gap distance between the faced electrodes. The increased frequency caused straighter, tighter, and more uniform NWs alignment, which is consistent with the theory described in 2.8.3. The more uniform alignment was observed when the spike shape of electrodes end was used, as opposed to the round shape, in which the capture of the NWs at the electrode side was typical. Additionally, more single-NW interconnections were achieved using the spike electrodes, unlike the rounded. On the contrary, no difference in the NWs alignment ability in between 50 µm and 100 µm electrode spacing was proven.

The electrical measurements of the faced electrode containing single-NWs and multiple-NWs interconnection were performed using the probe station system (Cascade Microtech, MPS150) connected to parameter analyzer (Keithley, 4200-SCS). The results presented in Figure 59 indicate an asymmetric and non-linear characteristic for the I-V curves. Both curves suggesting that the contact between the NWs and the electrode has a Schottky nature. In gas sensors, the response is defined as the relative changes of electrical resistance before and after exposure to gaseous analytes, and generally, two components contribute to these changes (1) the NW channel and (2) the contact resistance between NW and the electrode. These contacts may have a Schottky or ohmic nature, and although ohmic contacts tend to be more attractive in gas sensors, there is evidence that Schottky contacts are more appropriate for reducing gases enhancing the sensor response, for instance up to four orders of magnitude, as demonstrated previously for carbon monoxide sensors. [153,154]
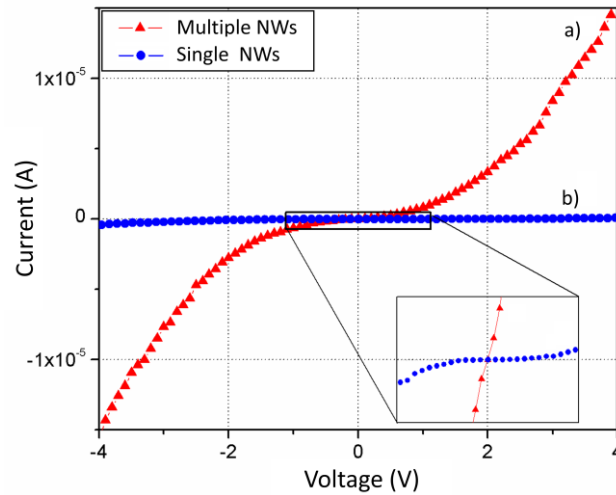
Figure 59. I-V curve measurement of two types of WO$_3$ NWs interconnections aligned in parallel microelectrode array (at RT): a) M-NWs, b) S-NWs.

3.3   Summary

The experiments and results described in this chapter served as a proof of concept to advance on the fabrication of the second chip generation. Briefly, the results indicated that the NWs damage, caused during the removal process of as-deposited WO_3 NWs from the basic substrate carrier, was significantly reduced by decreasing the sonication forces to minimal value (10 % of power) for a relatively short time (5 seconds in a sonication bath). This measure helped to increase the length of removed NWs up to 10 μm approximately. The concentration shows to play an important role in the number of NWs aligned between the electrodes. This was solved by using smaller pieces of the substrate containing the NWs and diluting further the solution in which the NWs were suspended.

The microelectrode array platform (first chip generation) was designed in order to find the optimum DEP parameters for the integration of WO_3 NWs. These chips consisted of ten microelectrode arrays with faced electrodes, two straight electrodes, and other testing structures, which were fabricated on 4-inch silicon wafers with minimal resolution of 2 μm for the smallest electrodes. Additionally, the microelectrode array was made in several modifications, mostly differing in the spacing between faced electrodes and different end shapes. During the fabrication process, it was found that the oxygen plasma treating after the resist development process affects the uniformity of the wet etching process. This process turns out to be one of the key processes for the final shape of the electrodes. The final chip size was 1x1 cm which was sufficient for all undergone operations, such as electrical contacting by probes, or the drop coating.

In conclusion, it was found that 5 μl drop is enough to cover a whole array area of the chip and that the water repellent structures stop the drop from expanding. The most suitable NWs alignment was observed for the microelectrode array with 3 μm gap and spacing 50 μm between the faced electrodes. The faced electrodes with spike end shown better capability for the alignment, as opposed to the round shape. The dielectrophoresis process with an adjusted bias voltage to 5 V and frequency 9 MHz applied for 5 seconds showed excellent alignment results and electrical interconnection of multiple (WO_3) NWs assembled in parallel across the faced electrodes. Several single NW interconnections were also observed under these conditions.

4   Second chip generation: Nanoelectrode arrays platform for parallel alignment of single nanowires using for gas detection

As discussed previously in chapter 4, the first chip generation revealed several unwanted effects which could be prevented by the modification of the chip design and the addition of new fabrication steps. For example, the first chip generation showed that the DEP forces are present all over the electrodes with the same intensity. This causes the NWs to be attached on undesired areas of the electrode, in contrast to the elementary assumption that indicated an exclusive connection between the two faced electrodes. In this context, chapter five presents amongst other improvements the use of an additional layer, which covers the rest of the electrodes and performs electric field shielding, simultaneously. The second chip generation was also intended to connect various single NWs in a parallel array for gas sensing tests. For this reason, various electrode systems were fabricated to unfold the ideal modification with the aim to (1) achieve good signal-to-noise (S/N) ratio, (2) enhance the measured gas sensing response, (3) provide only single NW interconnection.

Generally, the electrodes in the second chip generation were carried out using the combination of EBL and DWL techniques. The first approach included the use of a lift-off fabrication process with direct deposition of Ti/Au conductive layer over a pre-patterned mask to achieve the electrode structures. The second approach included the so-called etch-back process with both deposition and etching process. These approaches required the use of advanced dry etching tools, particularly, in the case of nanoelectrodes etching, where the achieved resolution is usually in the order of nanometers and preferable anisotropic. Both approaches have their advantages and disadvantages that are discussed further in this chapter. [115]

As described in 1.2.1, a basic prerequisite for the measurement of gas sensing properties of MOX gas sensors is the presence of gas-solid interactions, which usually occur at high temperature and thus need of heating element (heater) able to provide optimal temperature conditions to the gas sensitive material. Therefore, in order to facilitate the fabrication of the second chip generation and further gas sensing tests, an external heater was integrated between the package and backface of the chip (as a single unit). The external heaters were fabricated using thick film technology based on the screen-printing process of several functional layers on alumina (Al_2O_3) substrate [155] to reach temperatures of 250 ºC.

Overall, the second chip generation shows the fabrication of electrode array systems, which can be loaded with different types of sensitive material in the form of NWs. The work proves the integration of various types of NWs on a single chip with independent electrode arrays and the possibility to exploit them on the fabrication of selective gas sensing elements.

4.1 Experimental and methods – part I.

In the first part of the experimental, the fabrication process of the second chip generation is presented. Two lift-off processes were used to make a test structure that serves to prove a design concept for single NWs arrays.

4.1.1 Fabrication of nanoelectrode array test structure on 2x2 cm substrate using lift-off process

The individual steps of the fabrication process of the second chip generation by lift-off approach is described below.

1. The design proposal of the test structure

The layout of the second chip generation test structure for the fabrication using the lift-off process is depicted in Figure 60. The second chip generation has a quarter (5x5 mm) of the size set for the first chip generation. This new chip has four arrays with various modification of the electrode system. Figure 60a shows separation stripes (gold) that work as hydrophobic traps keeping the drop with suspended NWs in the selected array (violet color). Thus, several additional electrodes around the general electrodes array may help to eliminate the amount of NWs in the area of nanoelectrodes (green color). During the DEP process, the voltage potential applied to these electrodes causes that some NWs get attracted to them as well as to the nanoelectrode array. The other electrodes with pads serve for further electrical characterization; if needed (red color).

The design of the electrode array is illustrated in Figure 60b, where a red frame highlights the write field area (100x100 μm) for the precise stitching of the nanoelectrode pattern. Apart from resistive topology, the test design consists of another two topologies that may be used to enhance the gas sensing properties of the sensor (FET topology with the third electrode) or the resistive measurement setup with 4-wire electrodes arrangement, as it is shown in Figure 60c and in the detailed view in Figure 60d, respectively. More information about the description of all structures placed on the chip is presented in chapter 4.3.1.
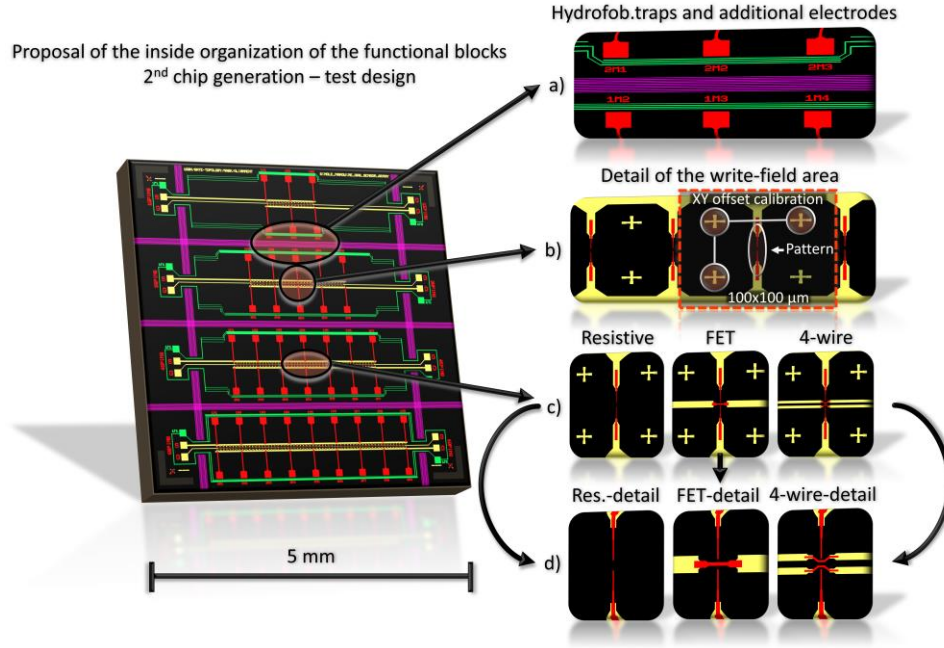
Figure 60. The design proposal of the organization of the functional blocks for the second test chip generation (colors: yellow – alignment electrodes, red – electrodes for measurement, and EBL design of nanoelectrodes, violet – water repellent structures (hydrophobic traps), green - additional electrodes, black – thermal oxide layer (SiO_2)): a) hydrophobic traps and other structure, b) detail of the write-field area, c) electrode array modifications (resistive, FET, 4-wire), d) detail of electrode array modification displaying EBL nanoelectrodes and microelectrodes processed by DWL.

2. Substrate processing before a lithography

In order to eliminate the charging effect of the SiO_2 dielectric layer, 4-inch silicon substrate (525 μm thick wafer) with thermally grown oxide about 300 nm was used as a basic substrate in this fabrication process, instead of 500 nm thick SiO_2 layer. The charging effect can occur during the EBL and brings unwanted problems during the EBL, but also in following procedures (e.g., SEM inspection of aligned NWs). Thus, the wafer was covered by positive tone optical resist (AR-P-3540) to protect the surface from mechanical damage and various impurities produced within the dicing procedure. Subsequently, the trimming laser Aurel ALS300 was used to perform cut-lines over the wafer surface, deep enough (tens of μm at least) to effectively break the wafer into 2x2 cm pieces. The whole 4-inch wafer with marked laser cuts is illustrated in Figure 61.
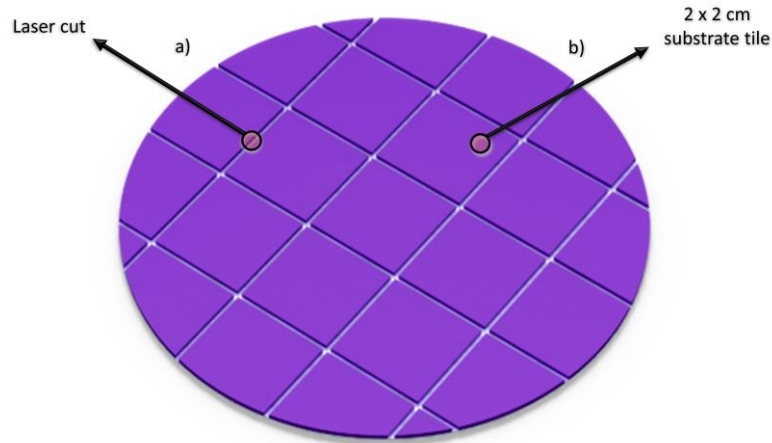
Figure 61. Illustration of a <u>4-inch</u> wafer cut on 2x2 cm pieces.

Afterward, individual substrate tiles were cleaned in NMP-based solvent stripper bath (Microchem, PG Remover) warmed up to 80 °C and enhanced by sonication for 30 min. However, to avoid any organic impurities and to increase the adhesion of the resist, each substrate was treated in oxygen plasma before spin-coating. During the plasma processes, substrates were always cooled at 20 °C from the bottom side. Parameters of the plasma cleaning procedure are listed in Table 4.

Table 4. Parameters of the plasma cleaning procedure.

Plasma cleaning procedure – DIENER Nano – plasma resist stripper	
Parameter	**Process**
	Plasma cleaning
Power (W)	600
Process Pressure (mbar)	$1 \cdot 10^{-1}$
O_2 flow (sccm)	7
Time (min)	60

3. Photoresist processing, lithography, and development (1st lithography)

After plasma cleaning, the substrate was coated with an adhesion promoter (AR-300-80) using spin-coater (Labspin) with rotation speed 4000 rpm that corresponds to a thickness of about 15 nm. Thus, the substrate was coated with photoresist (AR-N-4340), exposed by DWL and developed in an immersion bath with the developer (AR-300-475). For this process, it was applied the same process conditions used previously in the fabrication of the first chip generation. Figure 62 shows the photoresist mask (electrode arrays and other structures) prepared for the fourth fabrication step.
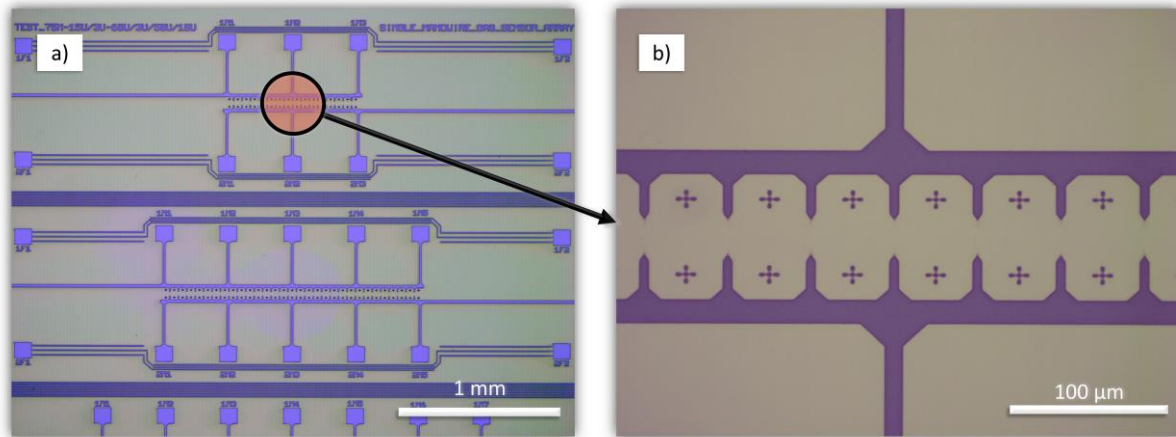
Figure 62. Optical inspection of arrays after photoresist development: a) 5x mag (objective), b) 20x mag (objective) detail.

4. Optimization of the resist development using plasma ashing process (DESCUM)

The DESCUM process was carried out using plasma resist stripper (Diener, Nano) in order to remove undeveloped resist residuals remained on the substrate in developed areas. Concerning the principle of the lift-off fabrication process, in which the pattern is created by deposition over the resist (mask), the DESCUM process is crucial fabrication step that can provide better adhesion of deposited layer with the substrate surface, as described in 2.1.2 or 3.2.1. To ash at least 100 nm of the resist layer (this thickness is usually enough to eliminate leftovers from the immersion development), the DESCUM process was optimized by measuring the thickness losses in pattern trenches of the photoresist before and after 15 minutes of applying oxygen plasma under conditions specified in Table 5.

Table 5. Parameters of AR-N-4340 resist ashing procedure for findings of DESCUM conditions.

Photoresist ashing – DIENER Nano – plasma resist stripper	
Parameter	**Process**
	Resist ashing
Power (W)	600
Process Pressure (mbar)	$1.5 \cdot 10^{-1}$
O_2 flow (sccm)	7
Time (min)	15

The thickness measurement was performed using profilometer Dektak XT in standard 2D scan mode in the highest resolution mode "hills & valleys" with a range of 6.5 μm in Z-axis, which is depicted in Figure 63.
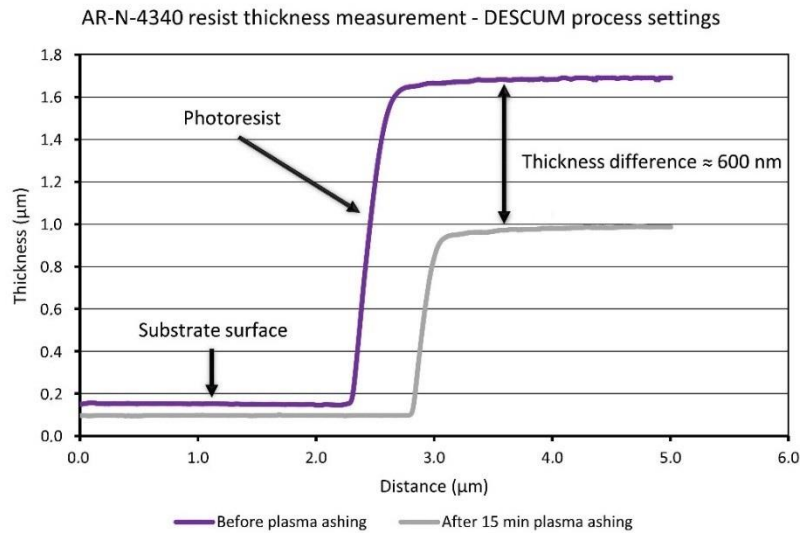
Figure 63. Photoresist thickness measurement using profilometer before and after plasma ashing.

The difference in the thickness of the photoresist after 15 min plasma ashing was approximately 600 nm, which corresponds to the etching rate about 40 nm/min. Thus, the conditions of the DESCUM process for photoresist AR-N-4340 are well known, and the parameters are listed in Table 6.

Table 6. Parameters of the DESCUM process for AR-N-4340 resist.

Plasma DESCUM – DIENER Nano – plasma resist stripper	
Parameter	**Process**
	DESCUM (AR-N-4340)
Power (W)	600
Process Pressure (mbar)	$1.5 \cdot 10^{-1}$
O_2 flow (sccm)	7
Time (min)	2.5
Resist Thickness removed (nm)	100

5. Deposition of Ti/Au conductive layer (1st deposition)

After the DESCUM of 100 nm of the photoresist, the substrate was put into the high vacuum sputtering system (BESTEC – magnetron) to deposit a conductive layer (Ti/Au) of 100 nm thick. The parameters of the deposition are shown in Table 7. Titanium was used as an adhesive layer instead of the nickel-chromium alloy, which showed poor adhesion in our previous experiments. For example, part of the structures using nickel-chromium were removed from the substrate after the cleaning procedure (immersion bath) enhanced with sonication.

Table 7. Parameters of Ti/Au thin film layer deposition using HV sputtering system (magnetron).

PVD deposition – BESTEC – High vacuum sputtering system (magnetron)		
Parameter	**Material**	
	Ti	**Au**
DC Voltage (V)	372	578
DC Current (mA)	405	345
Power (W)	150	200
Initial pressure (mbar)	$4.7 \cdot 10^{-8}$	$4 \cdot 10^{-8}$
Deposition pressure (mbar)	$9 \cdot 10^{-4}$	$9 \cdot 10^{-4}$
Substrate rotation (rpm)	10	10
Deposition rate ($\text{Å} \cdot s^{-1}$)	0.45	1.89
Layer thickness (nm)	5	95
Ar flow (sccm)	15	15

The result of the deposition is shown in Figure 64, where it is seen that the entire surface is covered with Ti/Au conductive layer.
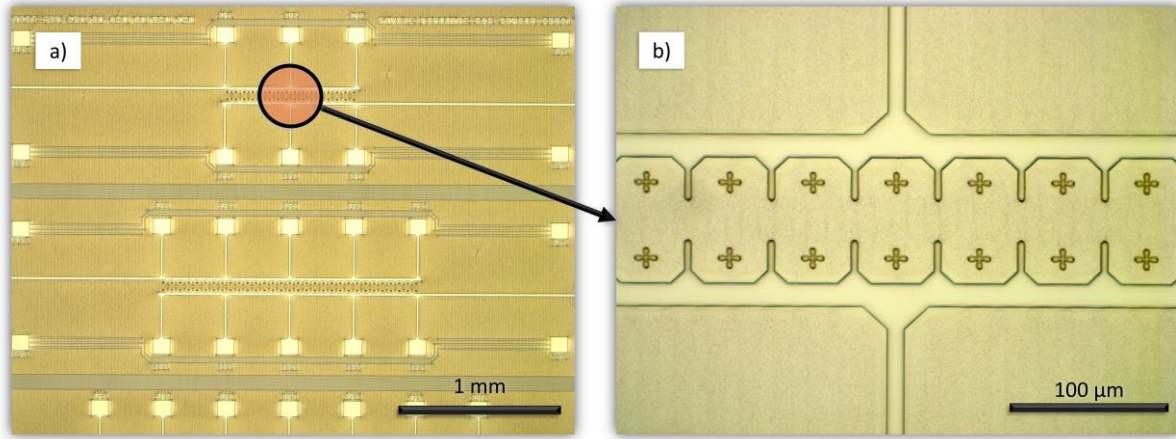
Figure 64. Optical inspection of arrays after the first Ti/Au deposition: a) 5x mag (objective), b) 20x mag (objective) detail.

6. Photoresist lift-off process (1st lift-off)

The substrate with photoresist and deposited layers was subsequently immersed in the bath with PG remover heated up at 80 °C and enhanced with sonication for 1 hour (lift-off process). To prevent the redeposition of removed material, the substrate was attached to the holder that enables to keep the substrate upside down. Hence, the photoresist detaches from the surface with deposited layers easily and does not stay on the substrate but drops to the bottom of the beaker. Then, the substrate was rinsed in two-step IPA solution, DEMI water and dried by nitrogen blow. The final structures made in the first lithographic step by lift-off process are shown in Figure 65. The photoresist is completely removed from the surface.
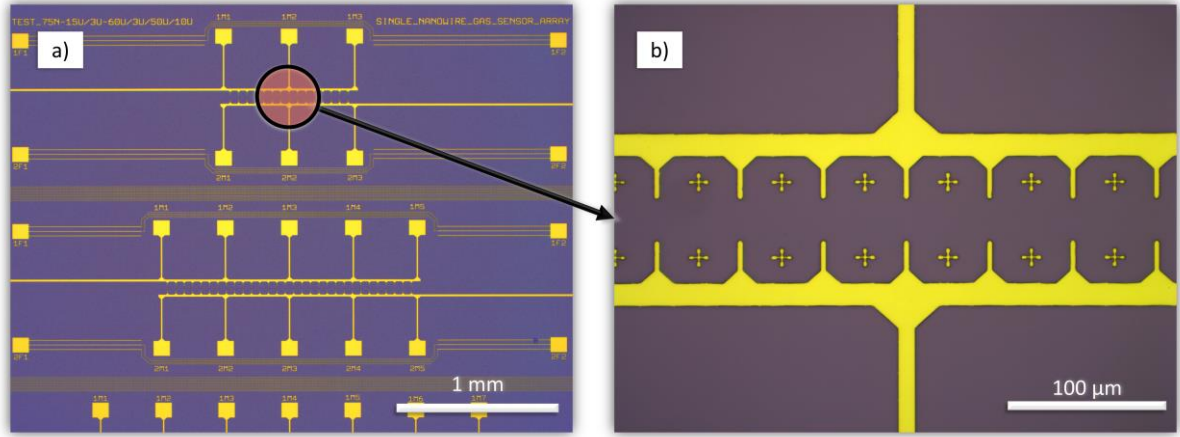
Figure 65. Optical inspection of arrays after the first lift-off process: a) 5x mag (objective), b) 20x mag (objective) detail.

7. Optimization of e-beam resist processing and exposure dose parameters

The e-beam lithography was performed using an adhesion promoter (AR-300-80) and a positive resist (AR-P-6300.13), which is about 400 nm thick after spin coating under the same conditions as those used for the photoresist (i.e., 4000 rpm for 60 s). Before the lithography itself, it was necessary to find out the actual conditions of the EBL process. In principle, the procedure was similar to that in photolithography based on DWL, in which the elementary parameter was a correct dose that was given by laser power and beam focus. In case of EBL (except other parameters as overlap and beam current) the primary parameter influencing the right dose is the dwell time, which is the time that the electron beam stays at a certain position. This parameter is dependent on beam current, which is variable during the cathode lifetime period.

Dose test (DT) was performed with the same substrate as was used for fabrication of test chip (2x2 cm) with deposited Ti/Au layer. The DT layout designed in order to find the correct dose is depicted in Figure 66b. The versatile layout consists of one hundred squares (50x50 µm) ordered in an array with marked rows and columns for better evaluation of the results. Thus, EBL was performed by the e-beam writer (Raith 150 Two) at 20 kV using stitching strategy by 100 µm write field areas as was planned to be used in the fabrication process of nanoelectrode fingers. The dose was distributed from 10 to 60 µC/cm^2, based on datasheet values. [119] The DT was evaluated using profilometer Dektak XT in map scan mode (3D), as can be seen in Figure 66a, whereas the accurate dose appeared between H and J column in a sixth row that corresponds to the dose from 38 to 40 µC/cm^2.
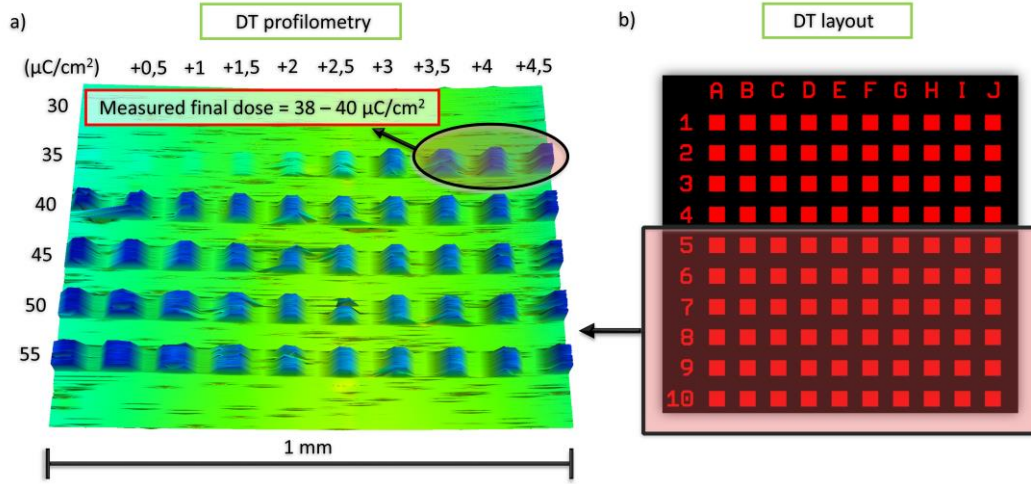
Figure 66. Optimization process of CSAR e-beam resist: a) dose test measured by a profilometer, corresponding to the b) layout for the dose test.

8. E-beam lithography (2nd lithography)

After the DT, the substrate (2x2 cm) with coarse structures down to 1 µm was cleaned using standard plasma cleaning procedure for 1 hour and spin-coated with e-beam resist (AR-P-6200.13) as was described above for the DT. Subsequently, the substrate was loaded into the e-beam writer to produce a mask (nanoelectrode fingers) over the microelectrodes made in previous fabrication step by photolithography and follow-up lift-off process.

Generally speaking, there are two fundamental procedures which were set up before the pattern execution, namely, the objects position information (coordinates) for a pattern generator and the microscope parameters adjustment settings. To the first, it was necessary to create a position list of all write fields (100x100 µm) in the layout in Elphy (Raith software). Then, the "global" coordinates of the designed layout could be attached to the "local" coordinates of the actual position of the structures on the stage holder. Accordingly, for this step, there were incorporated "substrate" position markers in marginal areas of the substrate, and inside "write-field" cross-marks for automatic XY offset calibration prepared in the first lift-off process. In the second procedure, several parameters related to the SEM microscope and the stage were adjusted employing various steps, e.g., calibration of the beam-column spot size, calibration of the X, Y, Z coordinates through entire substrate surface, calibration of actual beam current, and others.

Once the parameters of EBL were set, the pattern was executed using parameters as for the DT with an exposure dose of 39 µC/cm². The substrate was developed in the developer for e-beam resist (AR-600-546) followed by IPA and DEMI water rinse, both for 30 seconds. Then, the substrate was gently dried by nitrogen blow, and the result of the lithography was controlled by optical microscope (see in Figure 67) and SEM (Figure 70a).
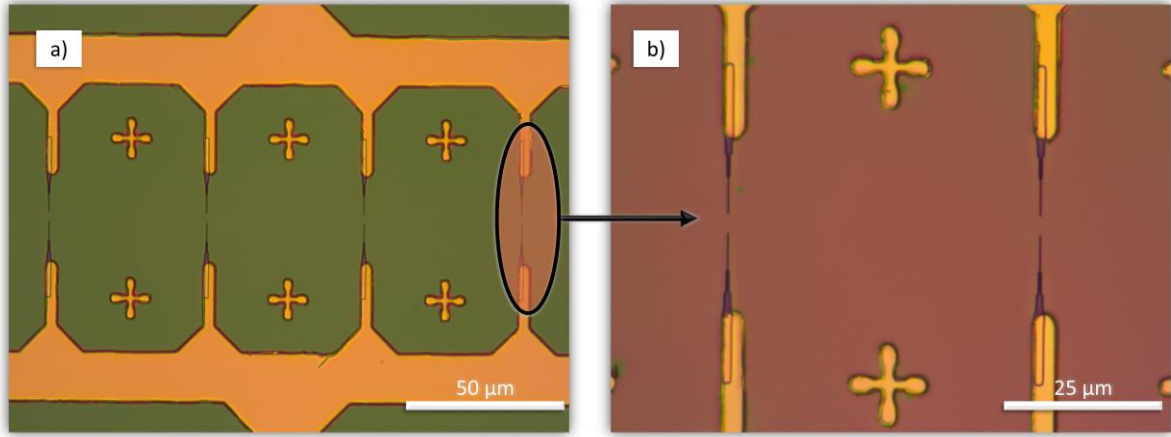
Figure 67. Optical inspection of EBL lift-off follow-up lithography: a) 50x mag (objective), b) 100x mag (objective) detail.

9. Deposition of Au/Ti conductive layer (2nd deposition)

The DESCUM process for e-beam resist (process pressure = 15 mBar, process time = 1 min, other parameters remains unchanged as in Table 6) was performed to ensure good adhesion of the follow-up layer, in which approximately 30 nm of the resist thickness was removed. Accordingly, a conductive layer of Ti/Au (100 nm thick) was deposited on the substrate with e-beam resist mask using HV sputtering system (BESTEC – magnetron). The parameters of the deposition were comparable to those used in the previous deposition. A photograph of the substrate (2x2 cm) after the second deposition is displayed in Figure 68a next to Figure 68b that depicts the structure layout.
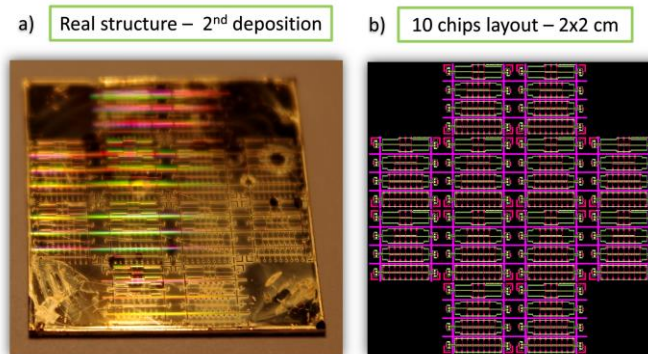
Figure 68. Illustration of the substrate (2x2 cm): a) photograph of the structure after the second deposition, corresponding to the b) layout of ten chips with all lithographic steps.

10. E-beam resist lift-off (2nd lift-off)

In this fabrication step, the substrate was immersed in the bath with e-beam resist remover (AR-600-71). The technique was identical to the one used in previous lift-off process for photoresist, with the difference that the applied sonication power was set to half the power used previously. After one hour, the substrate was rinsed under DEMI water stream and dried by nitrogen. Thus, standard plasma cleaning procedure was engaged for one hour. The result of

the second lift-off process is shown in Figure 69. It is noticed that even at the highest possible magnification, the image does not show the result of all lithographic steps clearly. For that reason, the SEM inspection was also used (see Figure 70).
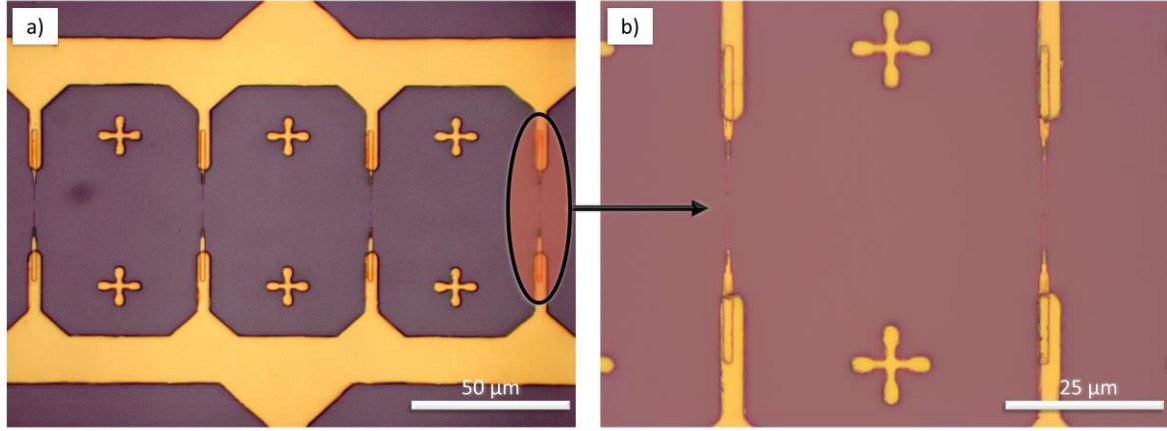
Figure 69. Optical inspection of the array after second lift-off: a) 50x mag (objective), b) 100x mag (objective) detail.

4.2   *Results and discussion – part I.*

SEM inspection depicted in Figure 70 shows the comparison of the nanoelectrode finger in two different fabrication steps. Figure 70a shows the result of the EBL (with resist) in which the developed area of the nanoelectrode finger (trench) is visible even though the quick SEM scan used to avoid charging (electron beam exposure) of the resist. Due to the image resolution, it cannot be well recognized the level of development, for instance, if the exposure dose was accurate (high enough) resulting in no remaining leftovers. On the other hand, Figure 70b illustrates that both structures (microelectrode and nanoelectrode) after the second lift-off process are interconnected. The structure does not show any signs of damage, taking into account that the structure passed through the lift-off process enhanced by sonication.
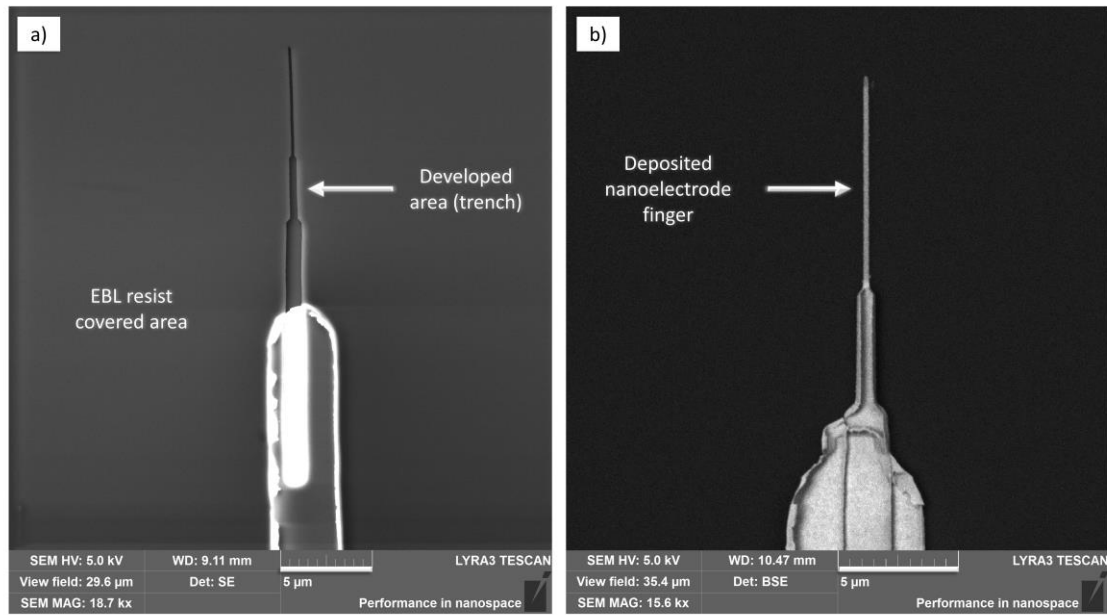
Figure 70. SEM inspection of lift-off process fabrication steps: a) developed area for follow-up Ti/Au deposition, b) deposited nanoelectrode finger after lift-off (interconnection step).

As stated in 2.6, one of the crucial failures of the lift-off process is creating the so-called "fence-like" structures in which the deposited material is redeposited on resist sidewalls. A typical example can be seen in Figure 71, which shows that both lift-off processes have redepositions that remain on the edges of the resist over the entire substrate surface even after the resist stripping process with ultrasonic. In the areas with outer structures (pads or lead electrodes) redeposition would not cause significant problems. However, in the inner areas (electrode fingers) it brings several issues for the follow-up procedures. In particular, a slightly positive edge of the fences made in the first lift-off created a barrier for the deposited material which gives rise to a weak electrical interconnection at the junction between micro and nanoelectrodes. Then, the fences occurred after EBL may complicate the subsequent NWs alignment procedure and cause weak contact between the electrode and NW (see in Figure 71b). Another problem is exhibited in the automatic offset calibration procedure, which does not work well with global cross-marks of the substrate. The EBL pattern for nanoelectrode fingers is aligned with a shift in both *XY*-axis, as can be seen in Figure 71a but also Figure 67b and Figure 69b. In principle, this shift may be caused by several reasons; for instance, the offset calibration procedure works with a design of small crosses that may have a different size from the real structure made in first lift-off (fences), so the pattern generator gets a wrong position results in calibration failure, or the calibration procedure failed.
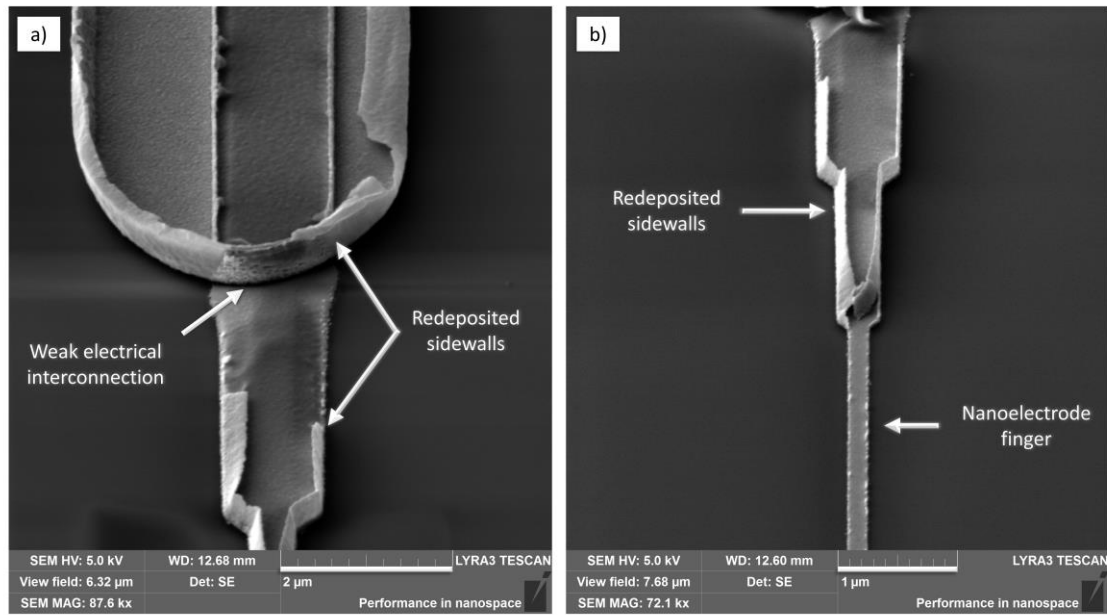
Figure 71. SEM inspection of metallic interconnection (junction) between microelectrode and nanoelectrode finger: a) depicts weak electrical interconnection and redeposition from both lift-off processes, b) nanoelectrode finger in detail.

Concerning the smallest possible structure that is possible to create by the lift-off process, it was found that the e-beam resist with a thickness about 400 nm is sufficient for structures larger than 75 nm, which correspond to the aspect ratio of approximately 5. Figure 72 depicts the measurement of the electrode finger thickness based on the SEM profilometry in which four profiles were measured from the thinnest (thin) to the thickest part (both electrodes). The measurement is illustrated in Figure 72b in which the "thin part" of the electrode has a thickness of about 20 nm that is one-fifth of the required thickness. In this context, considering the thickness, the conductivity of the smallest electrode part can be significantly reduced than in the rest of the electrode. Additionally, the thin layer with such thickness will be prone to electromigration (possible layer cracks as described in [156]), or other types of surface changes which may occur due to DEP forces, and high operating temperatures. Despite this and in order to find out the properties of the current design, several tests, including DEP procedure with WO_3 NWs were carried out using similar conditions to those used in first chip generation. Consequently, the dimensions and parameters of individual functional blocks (pad size for probe tip, size of an area for a droplet with NWs, hydrophobic barriers, and others) were analyzed during the experimental tests of the second chip generation first version. The insights obtained from these tests have been used for the subsequent version of the current generation.
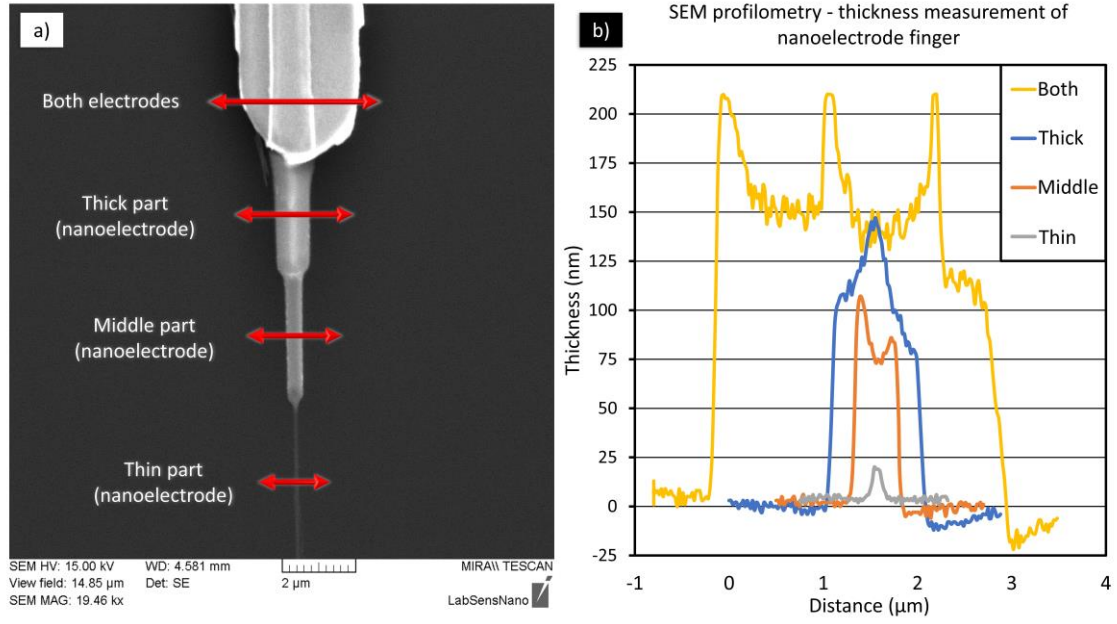
Figure 72. SEM inspection of metallic junction: a) figure with marked profiles area along the electrode, b) graphical illustration of measured thickness.

Figure 73 shows the electrode finger with aligned single NW over the 75 nm (width) nanoelectrode after the DEP. The voltage was lowered to 2.5 V peak-to-peak due to the weak condition of the nanoelectrode finger, but the frequency value stayed unchanged (9 MHz) respect to the conditions used for first chip generation. Even though electrical and mechanical conditions of the nanoelectrode required further optimization, the results after DEP were promising as the NW aligned precisely over the nanoelectrode end. Furthermore, the occurrence of a single NW connection was predominant, as can be seen in Figure 73b.
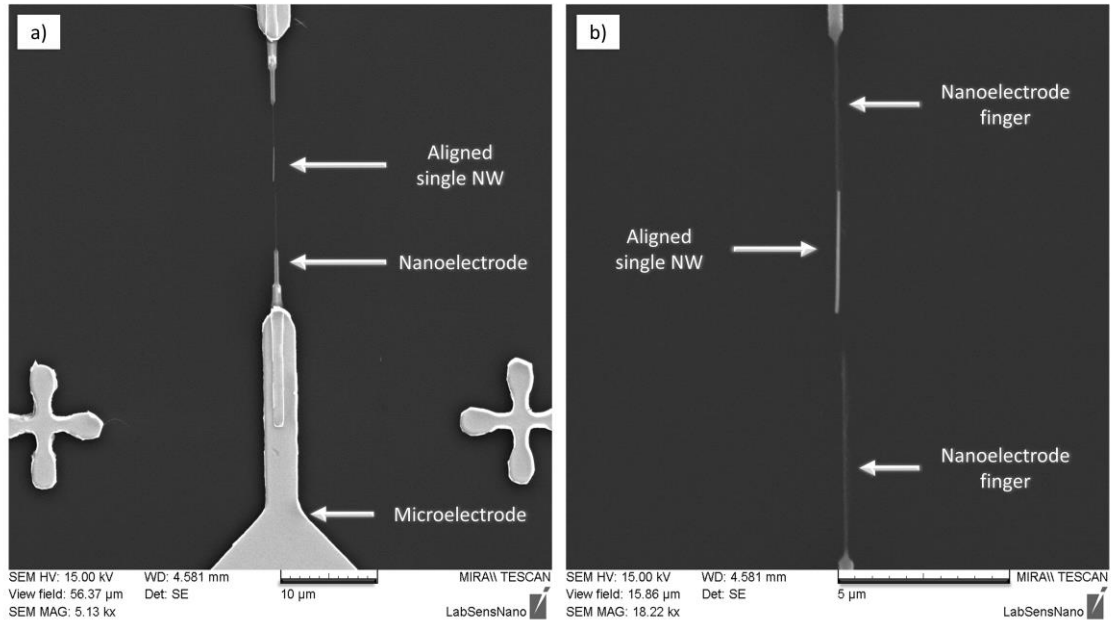
Figure 73. SEM inspection of nanoelectrode after NWs integration by DEP: a) distant view, b) closer view depicts aligned single NW.

The NWs that reached the nanoelectrodes were not long enough to contact both electrodes (electrode pair), as it can be seen in details in Figure 73b and Figure 74b. This could happen

due to several reasons, but the most likely is that the power of sonication was set too high, so the NWs were broken on pieces during the removal procedure. For this reason, the NWs has the same length about 2 μm, approximately. In Figure 74a is depicted interconnected electrode pair by two NWs stick up together.
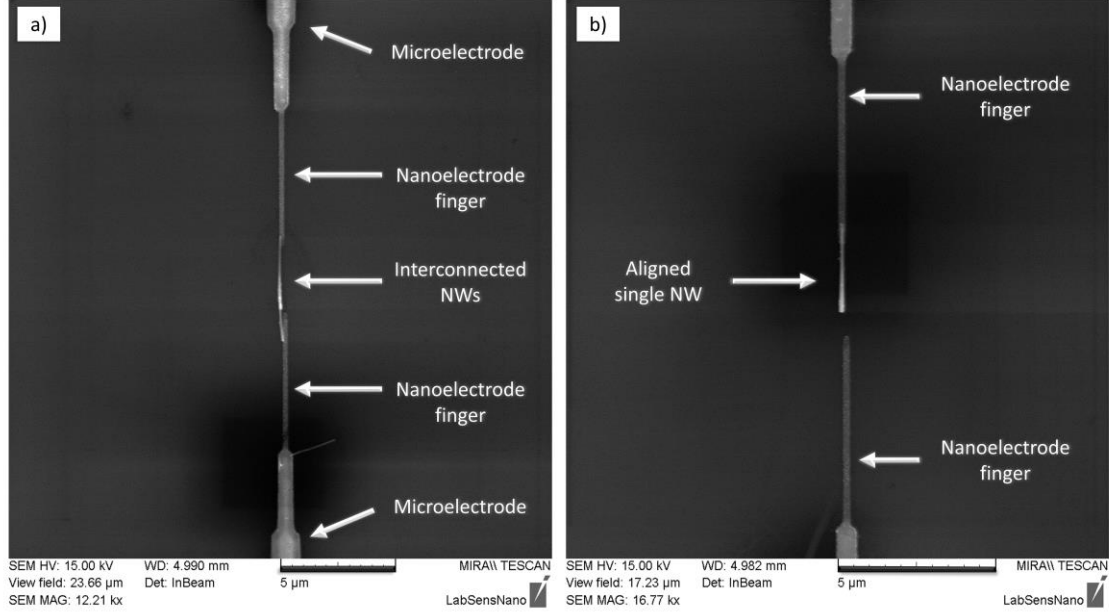
Figure 74. SEM inspection of nanoelectrodes after DEP process: a) aligned and interconnected NWs, b) aligned NW without interconnection of both electrode poles.

The parallel ordering was not as good as expected because only a few parallel connections were observed. A large amount of NWs was connected to the electrode wires (incoming thick leads) and to the additional measuring electrodes (for electrical characterization), in the area outside of the array with nanoelectrodes, respectively. This may be a reason why more NWs could not be aligned in parallel. These results were taken into account for the improvements performed on the new chips described hereafter.

4.3 Experimental and methods – part II.

The second run of experiments considered the results from the prior version and focused on optimizing further the process to fabricate the nanoelectrode arrays. In this section, the design and fabrication of the external heating element are also presented. The assembled sensing element containing the nanoelectrode array and the heating element in the backside was tested to the presence of various gases.

4.3.1 Design concept and specification of the nanoelectrode arrays and other functional blocks on the chip

In the second run of experiments, two topologies of the second chip generation were proposed to develop the gas sensor based on single NWs aligned in arrays. The first topology system, called "resistive", is conceived to work on the principle of measuring resistance changes in NW placed between electrode pairs without any other signal enhancement. The

second topology system, named "FET", consists in the resistive topology system equipped with an additional electrode insulated under the NW to work as the gate of the FET structure. Then, the gas detection signal can be impacted by applying voltage potential on this third (gate) electrode placed under the NW and between two electrodes.

The design of the individual functional blocks placed on a single chip can be divided into general (extended) and inside (detailed) view of the block organization. The extended organization view includes mostly elements for the recognition of the chip modification (topology), electrode arrays layout but also elements required for the finalizing steps of the fabrication process, for example, cut marks for chip dicing procedure, pads and so forth (illustrated in Figure 75), where both resistive and FET topologies are depicted together. To be specific, every chip consists of the following elements:

- *Chip identifiers and chip generation label* are situated in the upper left and upper right corner of the chip (shown in Figure 75a and Figure 75b). It provides an overview of the topology and the width of the nanoelectrode finger end. In details, there are four modifications of the nanoelectrode (will be specified further) and two topologies, i.e., resistive/FET chip with a final electrode width about 300 nm. Then, these labels can be helpful during the DEP process, or in other processes, to easily recognize the current chip modification.

- *Four electrode arrays* divide the chip into four parts, which, in principle have the same design but differing only in the number of electrodes (partly seen in Figure 75c, d). There are 15, 30, 45 and 60 electrodes, which were designed considering the number of possible single NW interconnection in one array. Each array consists of two contacting pads (labeled D and S on the sides, 100x100 μm), wires toward arrays (width 10 μm) and arrays itself. As can be seen in Figure 75c, the FET topology has one additional pad (labeled G) with the same dimensions than D and S.
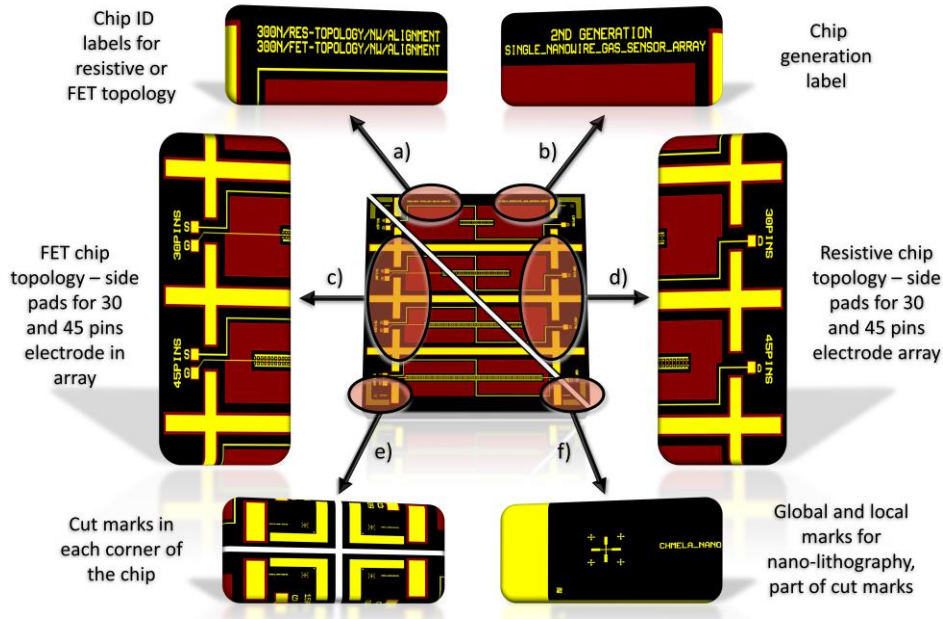
Figure 75. Second chip generation layout – general view of the organization of the structures (colors: yellow – electrodes and other structures (gold layer), red – resist for lift-off of SiO₂ dielectric layer, black – thermal oxide layer (SiO₂)): a) chip topology ID, b) chip generation ID, c) FET topology side organization, d) resistive topology side organization, e) cut marks, f) global and local marks for EBL.

- *Hydrophobic stripes* are designed to separate one electrode array from the others by the hydrophobic barriers (150 μm thick), which keeps the water drop in the middle of the array during the DEP (depicted in Figure 75c and Figure 75d). Additionally, the surface of these stripes is expected to have sufficient or more significant hydrophobic behavior than the surface with water drop to be held.

- *Cut marks with global and local marks* are placed in each corner of the chip (shown in Figure 75e). These cross-marks, with the gap of 200 μm, will be useful for finalizing dicing process, when the wafer is cut into separate chips. Global and local markers (crosses illustrated in Figure 75f) are part of the cut marks and are composed of one big cross (global, 50x50 μm) and four small crosses (local, 12x12 μm). These crosses are used for EBL alignment procedure during nanolithography, in which the chip offset calibration is performed supported by each cross.

As stated previously, the design of the second chip generation is divided into four independent electrode arrays. They are located in the middle of the array surrounded by hydrophobic stripes so that the DEP forces take place right in the center of the drop with dispersed NWs. The inside organization of the functional blocks is shown in Figure 76 that mostly illustrate the electrode array and its neared view. The electrode design was partly adapted from proven structures of the previous generation (Figure 76a). This new design addresses the constraints identified in the previous generation. For instance, the minimum dimension to perform the gate electrode, in the case of FET modification, is 1 μm that is given by maximum resolution of DWL tool. Further description of the electrode array design and its modifications is presented in detail below:

- *Electrode array specification* – the electrode array is made of parallel ordered electrodes (finger pairs) where the distance between individual electrode fingers is 50 µm. This spacing worked well for the first generation, and also it is sufficient for EBL 100x100 µm write-field areas (Figure 76b), which will be used to perform the nanoelectrodes. One finger pair consists of positive and negative faced electrodes with the gap about 4 µm in between. As proposed, they will be used to perform DEP in the first phase, and in the second phase for the measuring of resistance changes. Local cross-marks, created by DWL, serve for automatic *XY*-axis offset calibration procedure during EBL patterning for precise alignment and positioning within one write-field.
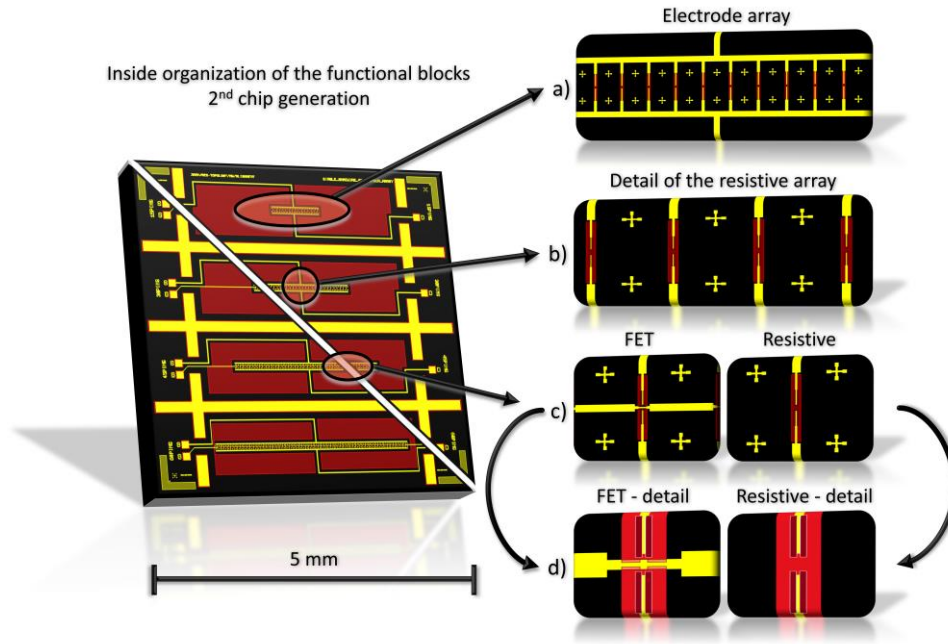
Figure 76. Second chip generation – the inside organization of the functional blocks (colors: yellow – electrodes and other structures (gold layer), red – resist for lift-off of SiO₂ dielectric layer, black – thermal oxide layer (SiO₂)): a) view of the electrode array, b) detail of the write-field area, c) view of the resistive and FET topology, d) detail of the resistive and FET topology nanoelectrodes (colors: yellow – electrodes (gold layer), bright red – resist for lift-off of SiO₂ dielectric layer, dark red – EBL pattern for dry etching).

- *Electrode finger dimensions* – the entire electrode finger, which is 43 µm long in total, can be divided into three parts. The first part is 20 µm long and 5 µm wide, and it is created in the first lithographic process (DWL) together with the second part, that is 23 µm long and 1 µm wide. Thus, the third part, which is called nanoelectrode finger, is fabricated by etching of the second through EBL pattern. The final layout is depicted in detail in Figure 76d, where the dark red color around the electrode (resistive) is the design for EBL, and the bright red color is the design for follow up lithography step, in which the entire electrode system, except the nanoelectrode, is covered by a dielectric layer. This structure is called a dielectric window, and it is more and less identical for both topologies. The thickness of the nanoelectrode is designed in four modification, i.e., 100, 150, 200, and 300 nm.

- *Design of the gate electrode in the junction area with nanoelectrode* – as stated previously, the gate electrode is 1 μm wide. This element is realized by DWL in the same lithographic step as the rest of the functional blocks (shown in Figure 76d). Additionally, the gate electrode must be covered with a dielectric layer to avoid short circuit during the gas sensing measurement. Whereas the gate is not designed as a buried electrode to reduce fabrication steps, the gate is covered in the last fabrication step. Last fabrication step is the deposition SiO_2 dielectric layer (dielectric window) with a thickness about 250 nm, in which appreciate adjustment of the optical lithography that can reduce the thickness of the deposited layer must be developed.

4.3.2 Fabrication of optimized nanoelectrode array structure using etch-back process (preferred process)

The individual steps of the fabrication process of the second chip generation by etch-back approach is described below.

1. Substrate processing

The fabrication of modified design was performed on 2-inch silicon substrates (380 μm thick) with thermally grown oxide (300 nm thick). The substrate was cleaned under DEMI water stream, dried by nitrogen blow and heated up to 180 °C for 5 minutes, to evaporate the rest of water and adsorbed humidity. Subsequently, the plasma cleaning procedure was performed for 1 hour; procedure parameters are listed in Table 4.

2. Deposition of Ti/Au conducting layer (1st deposition)

Three 2-inch substrates were mounted to 5-inch holder of HV sputtering system (BESTEC – magnetron) to deposit 100 nm thick conductive layer (Ti/Au) under the conditions shown in Table 7.

3. Photolithography – coarse structures and microelectrode fingers (1st lithography)

After the deposition of the conductive layer, the substrate was coated with an adhesion promoter (AR-300-80) and photoresist (AR-N-4340) using spin-coater with the rotation speed of 4000 rpm; this layer has a total thickness of about 1.4 μm. The pattern with all structures (coarse structures with microelectrodes) was exposed under DWL condition for this resist type obtained in the previous process. Then, the substrate was developed in an immersion bath with the developer (AR-300-475).

4. Ion-beam etching – coarse structures and microelectrode fingers (1st etching)

Before the etching, plasma DESCUM process (see in Table 6) was performed to remove resist residues. Then, the substrate was loaded to the IBE chamber to etch the Au/Ti layer by accelerated argon ions. The parameters are listed in Table 8.

Table 8. Parameters of Au/Ti thin film layer etching using ion-beam etching tool (SCIA).

Ion-beam etching – SCIA – coat/mill 200 system	
Parameter	**Material**
	Au/Ti
Beam Voltage (V)	400
Acceleration Voltage (V)	400
Beam Current (mA)	~213
Accelerator current (mA)	~5
Neutralization parameters	800mA, 55W 48/30V
Power (W)	280
Process pressure (mbar)	$8 \cdot 10^{-4}$
Substrate rotation (rpm)	20
Substrate Angle from handling pos. (°)	90
Etching rate ($\text{Å} \cdot \text{s}^{-1}$)	2/0.4
Layer thickness (nm)	95/5
Source Gasflow Ar (sccm)	18
Neutralization Gasflow Ar (sccm)	6
Endpoint detection	SIMS (Ti drop)

The substrate was cooled from the backside by helium gas to prevent thermal stress of the deposited layer. The etching process was stopped at the layer boundaries (Ti/SiO$_2$) using SIMS (Secondary Ion Mass Detection) spectroscopy (material detection) when a visible drop of the etched titanium was detected, respectively.

Then, the substrate was removed in the bath with PG remover (NMP-based solution) heated up at 80 °C and enhanced with sonication for 1 hour. Subsequently, the substrate was rinsed in two-step IPA solution, DEMI water and dried by nitrogen blow. At last, the oxygen plasma cleaning procedure was used to remove remained residues for 1 hour.

5. E-beam lithography – nanoelectrode fingers (2nd lithography)

This fabrication step was performed using the same parameters described in previous EBL process (see in 4.1.1). To reach a precise pattern alignment, the local cross-marks, which were fabricated in the first lithography step, were employed for the automatic *XY*-axis offset calibration procedure, as can be seen in Figure 77.

6. Ion-beam etching – nanoelectrode fingers (2nd etching)

The second IBE process was performed with the same conditions as in the previous first etching.

7. Photolithography – dielectric windows (3rd lithography)

Accordingly to the design, the pattern for dielectric windows was produced using negative photoresist (AR-N-4340), employing various fabrication steps, including spin-coating, DWL exposure, resist development, and DESCUM process. In contrast with previous lithography steps (etch-back process), this last lithography serves as a mask of microelectrodes ends inside the array (nanoelectrodes) and outside the array (pads, hydrophobic barriers, and so forth) for the following lift-off process (from 4.1), as is shown in Figure 77. Concerning the

results of previous lift-off process, in which deposited material stuck on the sidewalls of the photoresist, the development process was extended by 10 seconds in order to get undercut profile to prevent fence-like structures.
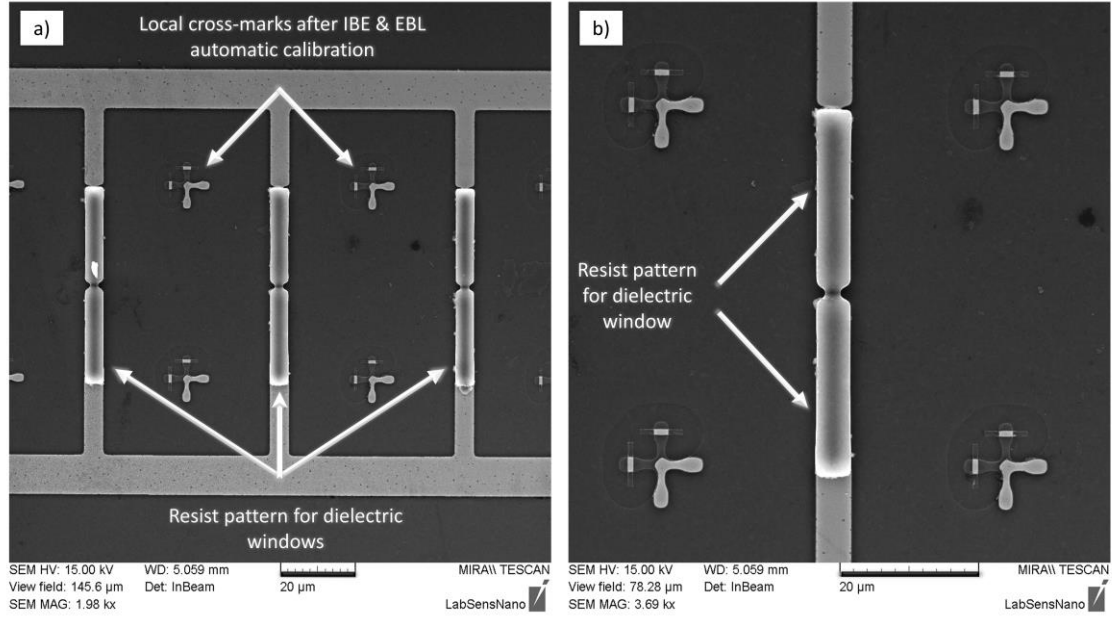
Figure 77. SEM inspection of the electrode array with resist mask for SiO₂ deposition: a) three electrodes, b) electrode finger detail.

8. Deposition of SiO₂ dielectric layer (2nd deposition)

Consequently, the entire surface of the wafer, except those covered in the previous step, basically the whole electrode path used for DEP, was covered by 250 nm silicon dioxide dielectric layer. The layer was sputtered using HV sputtering system (BESTEC – magnetron). The deposition parameters are presented in Table 9. In contrast to the other deposition using magnetron sputtering, the deposition time of the SiO_2 layer was quite long (approximately 3.5 hours). Unfortunately, this was the reason why the deposition was very unstable, and the process was repeated several times to be finished.

Table 9. Parameters of the SiO₂ dielectric layer deposition using HV sputtering system (magnetron).

PVD deposition – BESTEC – High vacuum sputtering system (magnetron)	
Parameter	**Material**
	SiO₂
Bias Voltage (V)	~458
Forward/Reflected Power (W)	112/8
Initial pressure (mbar)	$4 \cdot 10^{-7}$
Deposition pressure (mbar)	$1 \cdot 10^{-3}$
Substrate rotation (rpm)	10
Deposition rate (Å·s⁻¹)	~0.2
Layer thickness (nm)	~250
Ar flow (sccm)	15

9. Photoresist lift-off process (1st lift-off)

In the last fabrication step, the photoresist was removed using the procedure described in 4.1.1. This procedure includes immersion bath PG remover enhanced by sonication and plasma cleaning procedure. The result is shown in Figure 78, where the array with three electrodes is depicted in Figure 78a and the single electrode finger describing the individual electrode parts in Figure 78b.
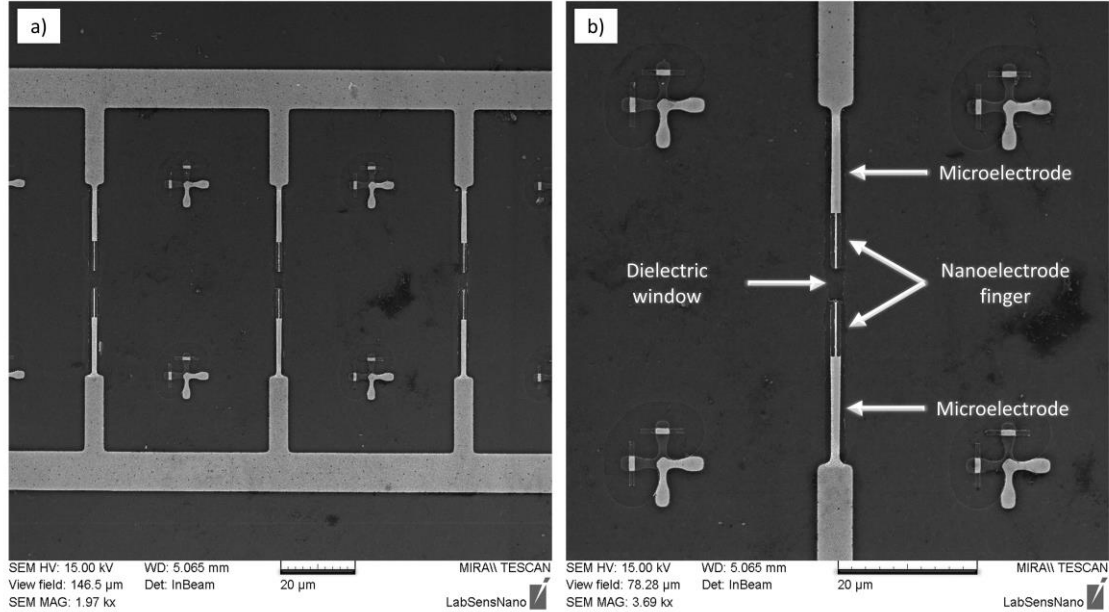
Figure 78. SEM inspection of the array after lift-off: a) three-faced electrodes, b) detailed view of a pair of faced electrodes.

After the entire chip fabrication process, the wafers were cut into the chip pieces 5x5 mm using compact laser dicer (Oxford Lasers, A-series).

4.3.3 Design and fabrication of heating elements for gas testing

Here it is presented the design and fabrication process of the heating element attached to the sensing platforms. These elements were integrated with the sensing platforms described in the previous section to provide the minimum thermal activation required to encourage the interaction between the nanowires and the target gas analytes.

1. Design and specification of the (external) heating element

Corundum ceramic (alumina, Al_2O_3) is commonly used as a substrate carrier in microelectronic, in particular, the realization of hybrid integrated circuits based on thick-film layers from which may be created basic electronic elements such as a resistor, capacitor, and so forth. In principle, the heating element is designed as a simple square printed resistor made of a thick-film resistive layer, in which the temperature is controlled by an applied voltage, or current respectively.

The aim was to create the heating element suitable for integration into the standard TO-8 package to fix it mechanically and contact it electrically. The design printed on a substrate with dimensions 5x5 cm, is shown in Figure 79. This design consists of 16 heater elements in total. All technological steps, including three lithographies and one dicing procedure, are depicted in Figure 79e, as well as a single heater in Figure 79f. In the first lithography, the conductive layer performs the electrical interconnection between the package pins and resistive layer (shown in Figure 79a), in which the contact area for soldering (pin to the heater) is 2 mm in diameter and contacts for the resistive layer are 0.7 mm wide and 7 mm long. The second lithography (Figure 79b), as stated, is placed between the contacts with dimensions 6x6 mm. The third (Figure 79c), isolation layer that covers both resistive and conductive layer with dimensions 8x8 mm. The alignment marks of each layer are illustrated in Figure 79d.

In the last technological step is generated file comprising the coordinates for laser dicer to make holes and cut lines in order to separate single heater from the others, as is depicted in Figure 79e, f.
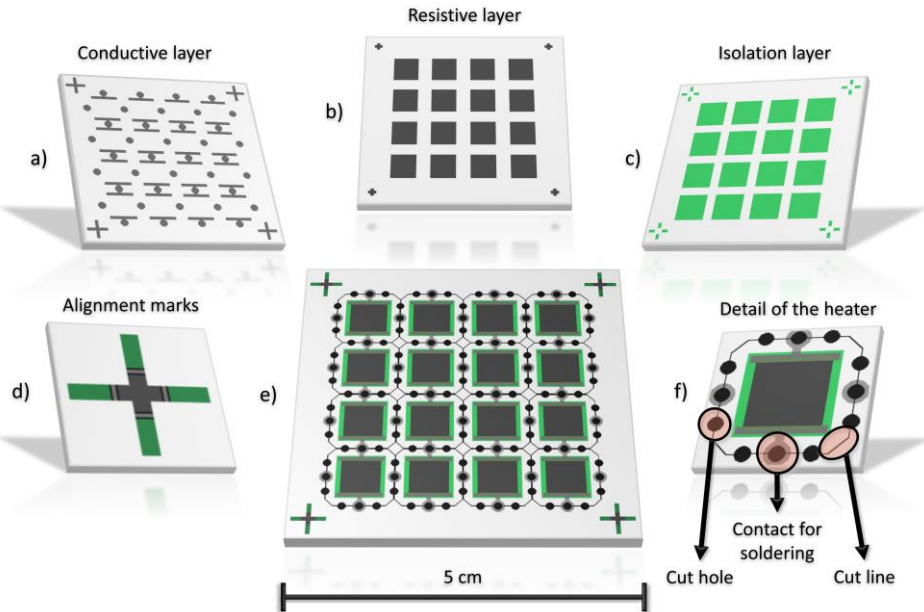
Figure 79. Design of the heater's layers: a) conductive layer, b) resistive layer, c) isolation layer, d) alignment marks, e) the entire substrate with 16 heaters, f) technology layers of the single heater in detail.

2. Heater fabrication

As stated above, several ceramic substrates (5x5 cm, 250 μm thick) were used for small prototype production of the heaters. Before screen-printing, the pattern for the lithography that was prepared on a plastic foil was transferred to the three woven mesh using negative foil photoresist (MacDermid Autotype, Capillex CP). After lithography procedure, the first mesh was used as a mask (conductive layer pattern) to deposit a conductive layer (cermet silver and conductive palladium paste, ESL Electroscience, type 9695-G) using screen-printing station (Aurel Automation, C880 screen printer). Then, printed ceramic substrates were leveled for 10 minutes in the air and left in a drier (Memmert, UF 75 Plus) at 125 °C for 15 minutes to

evaporate solvents and other components of the paste. Subsequently, the process was repeated for the resistive layer (ruthenium resistive paste, ESL Electroscience, type 3911-J) and both layers were fired in industry furnace (BTU International, BUCR-1) at 850 °C for one hour cycle, with conveyor speed 2 m/hour, respectively.

Subsequently, the isolation layer (dielectric SiO_2 paste, ESL Electroscience, type 4771-P1) was printed. To ensure better dielectric parameters of the layer, the printing step was repeated once again to achieve a double layer thickness. Then, the substrates were leveled in air, dried and fired in industry furnace at 550 °C for 20 minutes, 6 m/hour respectively. The whole substrate with heaters was divided into pieces using compact laser dicer (Oxford Lasers, A-series).

3. Heater support substrate – mechanical and thermal stabilization

The heater is isolated by an interlevel alumina layer which serves primarily to eliminate thermal losses through the TO-8 package body. The additional alumina layer (250 µm thick) was cut by laser dicer (Oxford Lasers, A-series) and was made of two thin pieces following the shape of the heater and package (see in Figure 80). Consequently, between the heater and package was formed space filled with air, which causes that most of the heat flow via small areas of support resulting in reducing of thermal losses. Despite thermal losses, the support substrate provides mechanical stabilization, which is especially important when soldering the heater contacts.
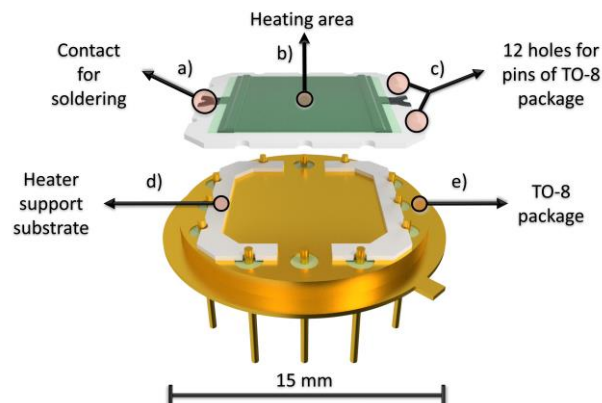
Figure 80. Illustration of the individual parts of the heating element: a) contact for soldering, b) heating area, c) holes for pins, d) heater support substrate, e) TO-8 package.

4. Heater contacts soldering – electrical interconnection

(Kovohute Pribram, in the composition of Pb92 % Sn5.5 % Ag2.5 %), with producer guaranteed melting point about 280 to 301 °C. After soldering, heaters were cleaned from soldering flux residues in the immersion bath (VIGON® SC200, Zestron) enhanced by sonication for 30 minutes. Then, TO-8 packages with heaters were cleaned by IPA and dried.

5. Heater characterization – temperature tests

Several heaters were characterized in order to find out maximal operation temperature. The measurement was performed by setting constant current using source measure unit (SMU) (Keithley 2401) that can measure other electrical properties (voltage or resistance) at the same time. Thus, the temperature was measured by a temperature sensor (Pt100) that was attached to the heater by silver glue (RS Pro, type 186-3593) and additional polyimide tape, which provided mechanical strength and kept them together. The electrical properties between 200 and 300 °C were measured in more details as this is the range at which the NWs are expected to respond better to various gaseous analytes.

4.3.4 Nanowires integration and sensor assembly procedure

NWs removal, integration, and alignment processes were carried out using the procedures described in 3.1.4 for the first chip generation. Two types of NWs were used to verify the possibility of creating a selective sensor; namely, WO_3 (NWs) and WO_3 (NWs) functionalized with Pt (NPs), which were described in [11]. Their surface (SEM) inspection and elemental composition (EDX) characterization are shown in Figure 81.
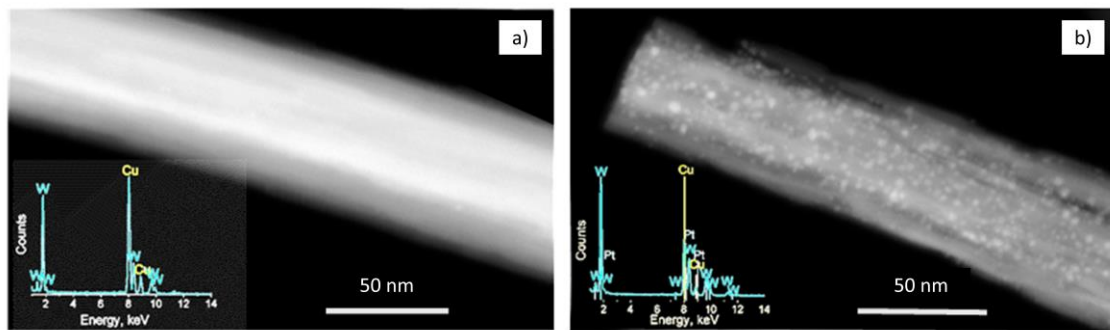
Figure 81. SEM and EDX inspection of NWs used as a sensing element: a) pristine WO_3 (non-functionalized), b) WO_3 functionalized with Pt NPs.

Silver glue (RS Pro, type 186-3593) was used to attach the chip to the package already containing the heating element. After 30 minutes of drying at room temperature, the chips were electrically interconnected to the TO-8 package pins by gold wires using wire bonder (TPT, HB16).

4.3.5 Nanoelectrode arrays with single aligned NWs in parallel gas tests

The gas tests characterization of the gas sensor based on nanoelectrode arrays with single aligned NWs in parallel (second chip generation) were carried out at the University of Barcelona (doctoral internship supported by Erasmus program). The gas measurements were performed in a gas station equipped by mass-flow controllers for precise gas flow adjustment connected via pipeline to a gas chamber adapted to various package types, including TO-8 package. The gas chamber is depicted in Figure 82. The parameters of the measurement (electrical settings, gas flow and so forth) were controlled by PC software created in LabVIEW

(National Instruments®) using SMU (Keithley 2401) for the sensor and programmable DC source (Keithley 2200) for heater settings.

The sensors were exposed to various gases and concentrations, including oxidizing gas, e.g., nitrogen dioxide (NO_2), and reducing gases, e.g., ethanol (C_2H_5OH), ammonia (NH_3) and carbon oxide (CO). The gas responses of the sensors were determined out by monitoring the electrical resistance changes of the NWs while applying different currents (in the order of nano amperes) under various temperatures. The measurement was in continuous gas flow mode (200 sccm) in which the initial baseline (stationary state) resistance was achieved by purging synthetic air into the chamber. Thus, by the mixing of the synthetic air with gaseous analyte provided by mass-flow controllers, the sensor response to the specific analyte concentration was measured (response state). Subsequently, the sensor was recovered by synthetic air at a full flow rate (recovery state).
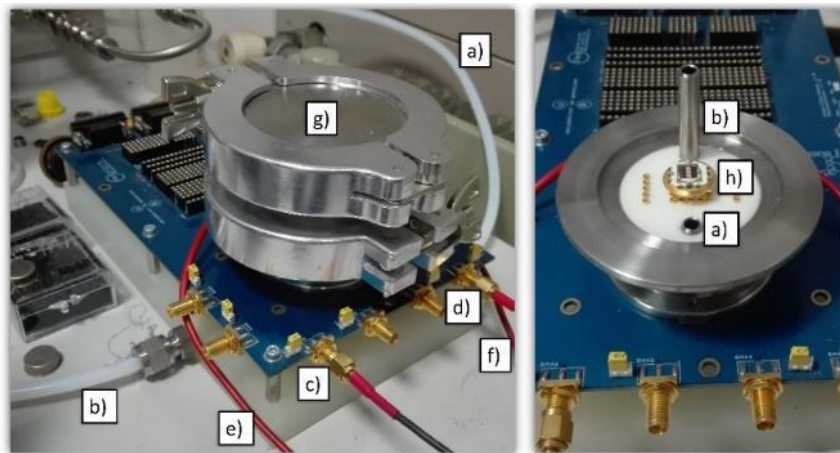
Figure 82. Description of the gas chamber parts at University of Barcelona (UB chamber): a) gas inlet, b) gas outlet, c) sensor +, d) sensor -, e) heater +, f) heater -, g) chamber cap, h) measured sensor.

4.4   Results and discussion – part II.

This section is dedicated to discussing the results obtained in the optimized fabrication process using etch-back approach. This section also describes the fabrication, and characterization of the external heater, and the gas testing of the nanoelectrode arrays with parallel aligned NWs.

4.4.1   The optimized fabrication process of nanoelectrode arrays on 2-inch wafers for gas sensing applications

Figure 83 shows one 2-inch wafer consisting of 56 chips in total. The structure of the chips situated close to the edge of the wafer were affected due to the poor light scattering during the lithography process. Concerning the etch-back process, several wafers were fabricated in order to use them for the fabrication process optimization to avoid any delay in the event that a parameter needed to be changed in a specific fabrication step (for instance, parameters of the automatic offset calibration (EBL), IBE and so forth). For this reason, each wafer was labeled with a unique wafer identification number (WID number).

Also, the wafer was divided into four segments in which three are dedicated to the resistive topology (42 chips) and one to FET topology with the third electrode (14 chips).
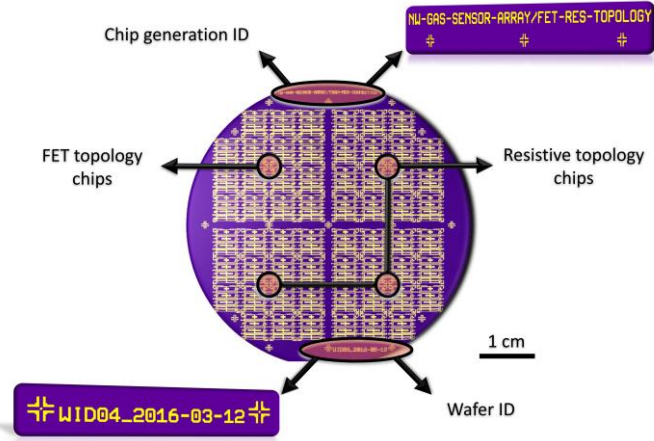
Figure 83. Illustration of a 2-inch wafer with structures of the second chip generation.

The final second chip generation with four nanoelectrode arrays for gas sensing applications is depicted in Figure 84a. This figure shows a close view of a microelectrode array with 15 electrode finger pairs (Figure 84b), and one nanoelectrode finger pair (Figure 84c).
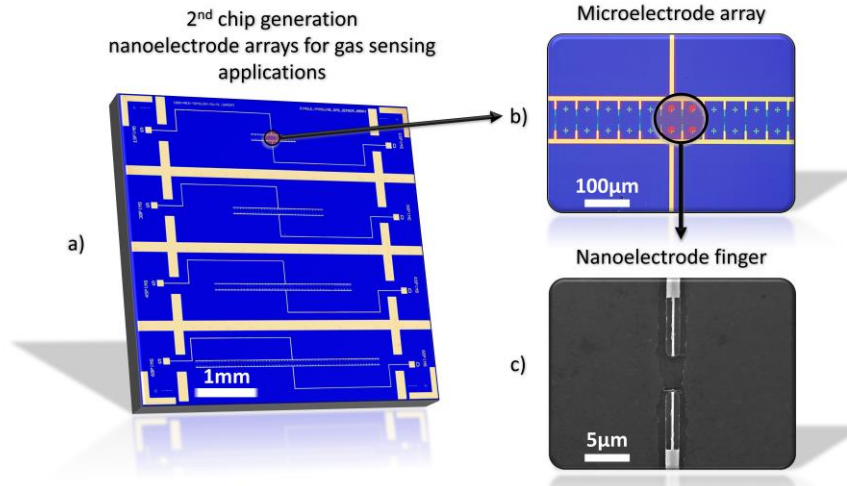
Figure 84. Illustration of the second chip generation: a) entire chip, b) microelectrode array with 15 electrodes – optical inspection, c) nanoelectrode finger – SEM inspection.

A detail of the nanoelectrode finger pair with a dielectric window made by lift-off is visible under SEM inspection in Figure 85. The nanoelectrode finger was fabricated in four modifications, which differ by the width (100, 150, 200, and 300 nm) of the end-side of the electrode. Figure 85b shows an example of the 300 nm wide nanoelectrode finger pair in detail.
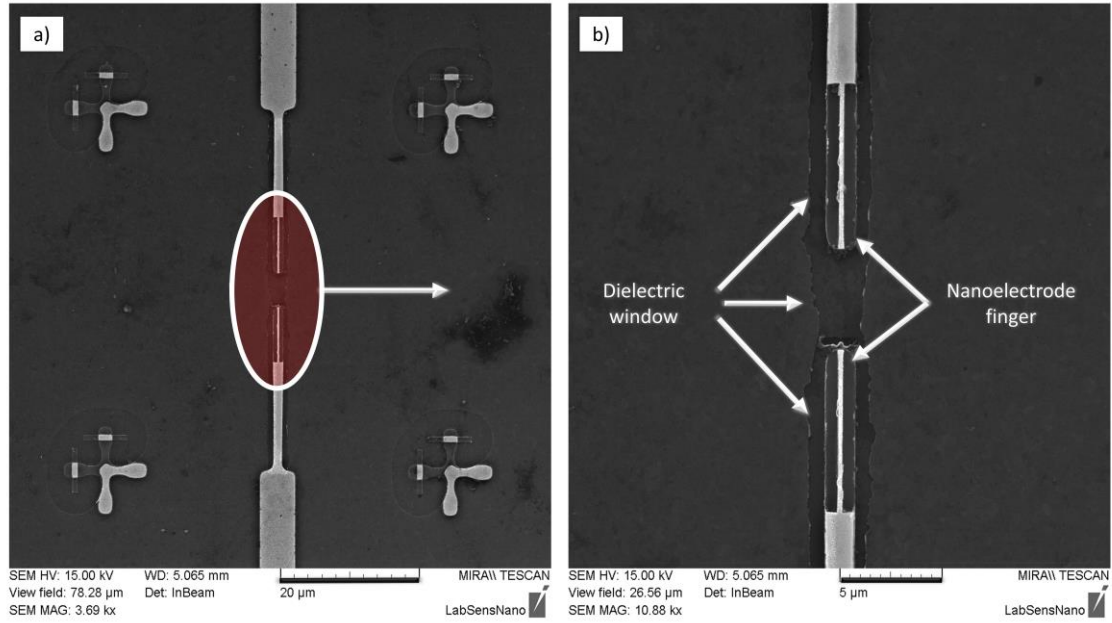
Figure 85. SEM inspection of the nanoelectrode: a) distant view of the electrode, b) closer view.

After the DEP, the results showed that the NWs were precisely aligned over the nanoelectrode pair, as is demonstrated in Figure 86. This result proved the hypothesis that the width of the electrode close to the NWs diameter could be a key factor for successful single NW alignment (see Figure 86b).

Relating to the result of the fabrication process, it was noticed that during the IBE process, redeposition (fence-like structures) are still formed at the edges of the electrode system. This may pose a problem for aligned NWs (visible in Figure 86b) due to poor electrical contact, non-homogeneous dielectric forces, or others. The redeposited structures can be caused by a perpendicular angle (90° from a handling position) of the ion stream to the substrate during the etching step. Also, the shape of the dielectric windows is not uniform after the lift-off, which was evoked by extending the development time (10 seconds), which give rise to the non-uniform shape of the windows.
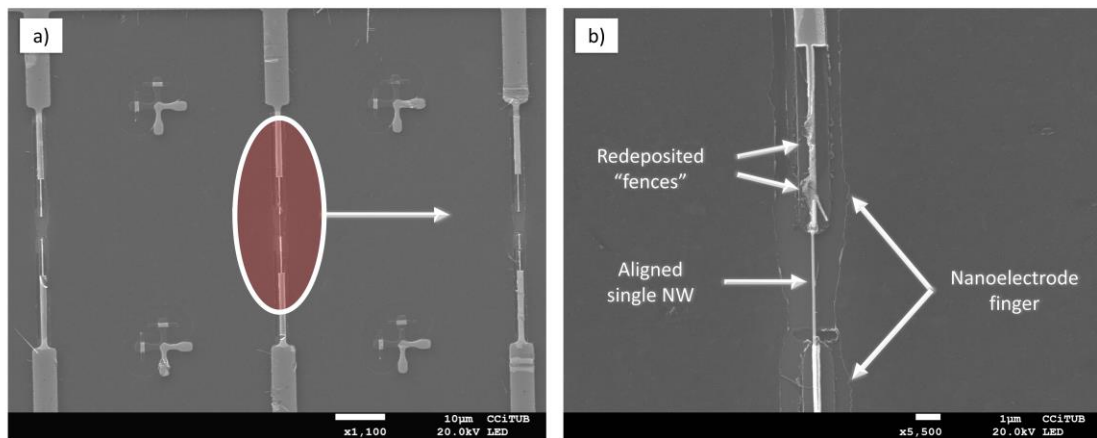
Figure 86. SEM inspection of an aligned single NW over the faced nanoelectrode: a) distant view, b) closer view.

Several wafers did not pass through all fabrication steps due to a fabrication process fails. Despite this, a few "unfinished" chips were used for DEP testing. For instance, the FET topology that is depicted in Figure 87 does not have the shielding dielectric layer because the EBL and follow-up IBE process were not successful. In this case, a wrong development caused that the remained e-beam resist prevent the effects of accelerated argon ions from the etching of the Ti/Au layer (see Figure 87b). However, despite the connection of various NWs to the electrodes, the parallel alignment of single NWs in the array was reached.
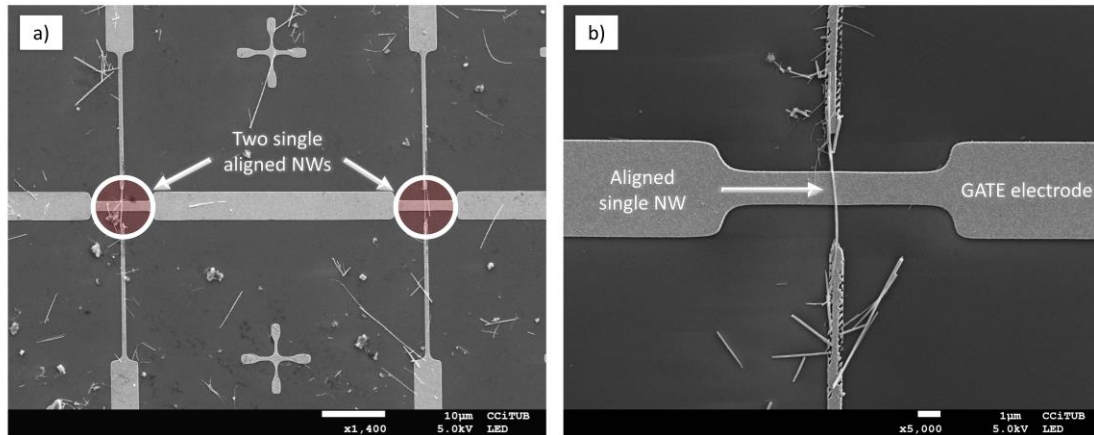
Figure 87. SEM inspection of two single NWs aligned in the FET topology array: a) distant view, b) closer view.

At last, an optimized fabrication procedure for the fabrication of nanoelectrode arrays was developed, as a result of the experience gained during the fabrication process of the second chip generation. The difference between the optimized fabrication and currently used process lies basically in the order of the lithographic steps, as illustrated in Figure 88. The first lithography used was EBL, in which the faced nanoelectrodes pattern was made as first (see in Figure 88e, f). Then, all faced nanoelectrodes were protected with (optical) resist after the following lithography, and the rest of the structures were linked together (Figure 88g).

The optimization of these processing steps solved several issues introduced during EBL process that finally increased the resolution of the final pattern and provided the better shape of the faced nanoelectrodes end. Such issues included, mainly, the pattern distortion artifacts, which can occur due to several reasons. For example, the fabricated structures (e.g., electrode fingers) creates a rough surface, which influences the flatness of the applied e-beam resist (400 nm thick) leading to the irregular shape of the EBL pattern. Also, it is well known that EBL suffers from charging effects (often results in the formation of strong electrostatic fields at the sample surface), which usually appears due to usage of electrically insulating substrates, and/or dielectric layers. Consequently, it causes a significant reduction in resolution, as opposed to the grounded and/or conductive substrates, which can effectively help with charge dissipation. [157]
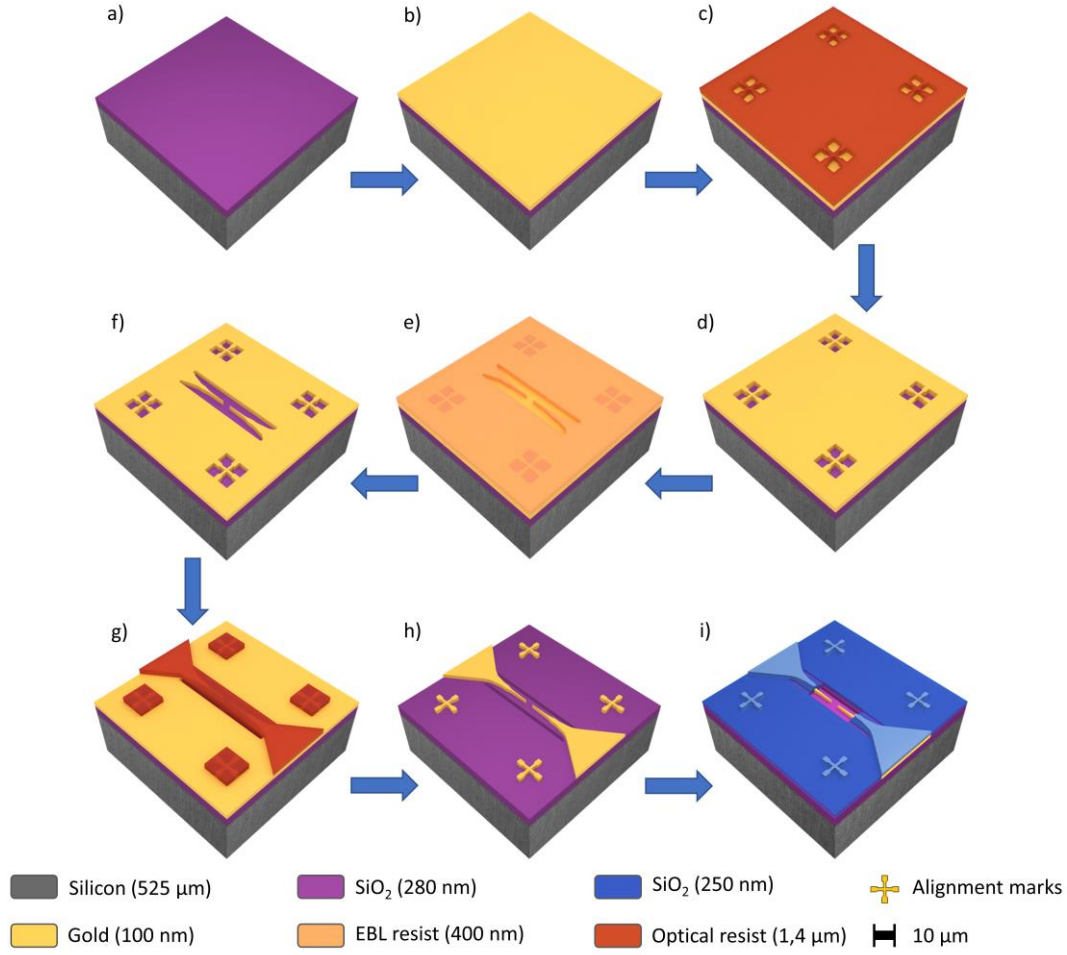
Figure 88. Schematic view of an optimized fabrication procedure developed to improve the fabrication of the nanoelectrode arrays: a) silicon substrate with SiO₂ layer, b) Ti/Au layer sputtering, c) pattern for marks used for the EBL automatic calibration, d) Au/Ti layer etching (IBE), e) pattern in EBL resist for faced nanoelectrodes, f) faced nanoelectrodes after Au/Ti etching (IBE), g) pattern for covering of faced nanoelectrodes, h) final electrode finger pair after Au/Ti etching (IBE), i) deposition of SiO₂ layer (dielectric windows).

4.4.2   Heater electrical and temperature characterization

Each heater was characterized in order to find their electrical and temperature parameters for the gas sensor characterization. The tests were addressed to determine the behavior of the entire system (heater and package) as a working heating element and in particular, the maximal operating temperature that the system could reliably reach.

During the tests, it was found out that the critical part of the heater, which has a main influence on the maximal operating temperature, was the solder joint between the pin and heater's contacts. This is related to the melting point of the solder, which is about 280 to 301 °C, according to the producer. The measurement showed that when the temperature approached 290 °C, then it evoked irreversible changes. These changes are in the form of structural distortion, which affects the electrical contact of solder joints (resistance change). Thus, the heater loses its characteristic parameters and are deteriorated. After further tests, it was concluded that the system had a reliable operation for a maximal operating temperature of 270 °C.

The theoretical heater resistance was designed to 10 Ω, that is given by resistance of ruthenium resistive paste (10 Ω/square, datasheet value), and in an area of 6x6 mm ≈ 1 square. As it is shown in Table 10, the theoretical value does not match with real values that vary by tens of percent. These deviations are mainly due to differences in processing parameters and used fabrication tools, in particular, parameters that influence the final layer thickness such as mesh type (holes per inch), resist thickness or pressure. Table 10 shows measured temperatures of three heaters which are dependent on set current/voltage values. Also, the calculation of the maximal power consumption (at 270 °C) and the temperature coefficient of resistance (TCR) are listed in the table.

Table 10. Heater characterization – temperature dependence on electrical properties.

Heater characterization – temperature dependence on electrical properties									
Parameter	Heater 1			Heater 2			Heater 3		
Temp	Voltage	Current	Resistance	Voltage	Current	Resistance	Voltage	Current	Resistance
(°C)	(V)	(A)	(Ω)	(V)	(A)	(Ω)	(V)	(A)	(Ω)
25	N/A	N/A	14.29	N/A	N/A	13.94	N/A	N/A	14.65
200	4.66	0.32	14.57	4.76	0.33	14.23	4.69	0.31	14.93
210	4.85	0.33	14.59	4.94	0.35	14.24	4.85	0.32	14.94
220	5.00	0.34	14.60	5.10	0.36	14.25	5.02	0.34	14.95
230	5.16	0.35	14.62	5.25	0.37	14.25	5.21	0.35	14.96
240	5.30	0.36	14.62	5.40	0.38	14.27	5.34	0.36	14.97
250	5.50	0.38	14.65	5.57	0.39	14.27	5.50	0.37	14.99
260	5.70	0.39	14.65	5.73	0.40	14.29	5.66	0.38	15.00
270	5.86	0.40	14.66	5.88	0.41	14.29	5.82	0.39	15.00
Power Consumption (270°C) (W)	2.34			2.42			2.26		
TCR (ppm/°C)	1.02·10⁻⁴			1.03·10⁻⁴			1.02·10⁻⁴		

The parameter TCR is one of the often-used parameters to characterize a resistor that is associated with the relative changes in resistance due to changes in temperature of the material under a given electric field. The TCR calculation for Heater1 is obtained according to the following Equation (4.1) described below [158]:

$$TCR = \frac{1}{R_{ref}} \cdot \frac{\Delta R}{\Delta T} = \frac{1}{R_{ref}} \cdot \frac{(R_{Tmax} - R_{ref})}{(T_{max} - T_{ref})} = \frac{1}{14.29} \cdot \frac{(14.66 - 14.29)}{(270 - 25)} = 1.02 \cdot 10^{-4} \, ppm/°C \qquad (4.1)$$

Considering the thickness of the resistive layer (several μm, thick layer), the value of TCR parameter should stay the same for each heater which can be potentially used for a precise calculation of desired temperature, if it is taken into account that the increase of the resistance is linear and their slopes are identical in the temperature range of interest. Figure 89 shows the electrical and temperature parameters of six measured heaters.
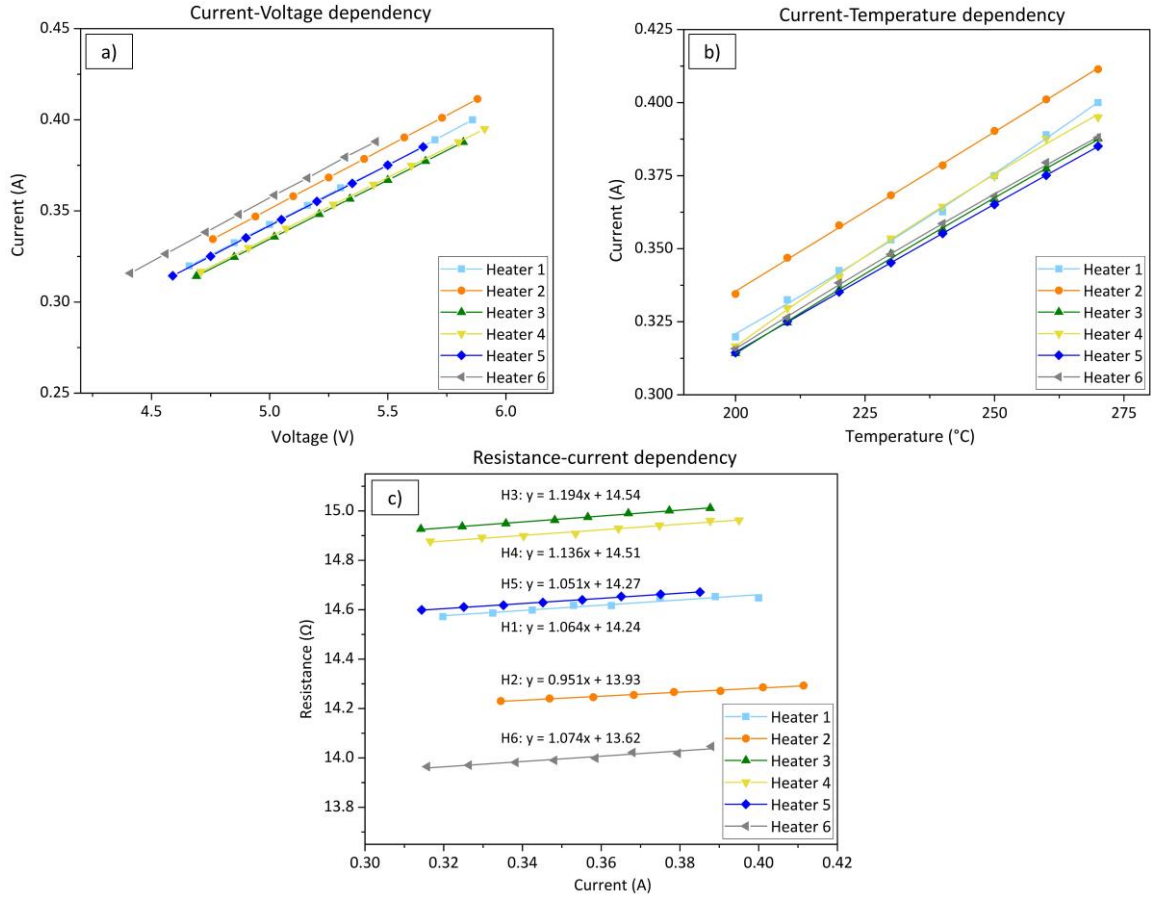
Figure 89. Electrical and temperature parameters characterization of heaters (1-6): a) current-voltage dependency, b) current-temperature dependency, c) resistance-current dependency.

The graphs show that the highest deviations of values are for heater2, which was measured the first. It could be due to a poor temperature sensor (thermocouple) attachment to the heater surface; this issue was solved for the next measurement by using a special holder with a tip to ensure the adhesion. Thus, except heater2, the values of the slope range between 1.05 and 1.20, which is quite a big difference to be used as a generalized method to set the temperature of the heater. Additionally, the slope values should be rounded-off, and that is not appropriate, especially in the case, where the calculation uses the equation that contains temperature-dependent resistance values, in which the difference between the lowest resistance (at RT) and highest resistance (at 270 °C) is only about 0.35 Ω. This would introduce a significant measurement error into the further measurement. For this reason, the temperature characterization of each heater was provided based on the measurement, in which the standard temperature calibration procedure, including measuring of stabilized temperature using Pt100 sensor, was used for every heater characterization.

4.4.3   Gas sensing tests

As was stated previously, two types of NWs were integrated into the separated arrays of faced nanoelectrodes using DEP process. Several sensors (TO-8 package with the external heater, and the chip with four separated electrode arrays) were prepared for gas sensing tests. These sensors were employed to perform essential tests, e.g., findings of the accurate current value with acceptable S/N ratio, receptor baseline resistance at different temperatures (from RT

to 250 °C), or sensor maximal response related to the actual temperature, and so forth. The real picture of the test device with all fabricated parts is displayed in Figure 90.
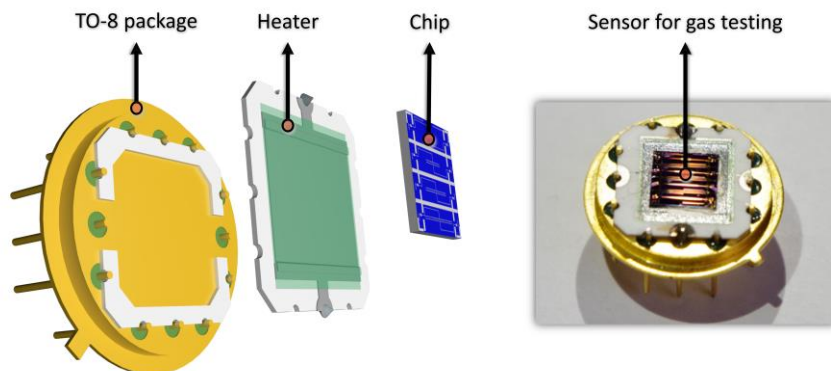
Figure 90. Sensor for gas testing - TO-8 package with heater and chip.

Generally, the integration of single-NWs into the nanoelectrode arrays (15 pairs) proved a success rate of approximately 33 %. Thus, each measured sensor employed in this work consisted of arrays of up to 5 single-NWs (non-functionalized or Pt-functionalized) as receptors. In principle, a slight deviation in numbers of connected NWs may raise deviations in data evaluation when comparing the responses of these two materials to the various gas species. For this reason, the gas sensing characteristics, mentioned further, were performed with structures that have parameters as close as possible, particularly, heater parameters and numbers of single connected NWs.

Effect of gas exposure on measured sensor resistance

Gas sensing tests of the nanoelectrode arrays based sensors with non-functionalized and Pt-functionalized tungsten oxide NWs were carried out applying current from 10 to 100 nA. The maximum sensor responses to nitrogen dioxide (NO_2) and ethanol (C_2H_5OH or EtOH) were found when using a constant current of 50 nA and temperature about 250 °C. For these conditions, the sensors showed changes in the electrical resistance after exposure to various concentrations of NO_2 or EtOH consistently, as is shown in the recorded measurements below.

Additionally, the parameters of gas sensing procedure for NO_2 are displayed in Figure 91, in which Figure 91a represents the responses for the non-functionalized NWs and Figure 91b for functionalized NWs with Pt NPs. One gas sequence consists of three replicated for each gas concentrations, but the exposure time remains the same. The lowest concentration measured includes the stabilization for 15 minutes (baseline resistance) with synthetic air (SA) followed by three peaks of NO_2 (0.2 ppm), one introduced every 5 minutes. The concentration of NO_2 is different only in the last sequence, in which the concentration is 2.5 ppm for non-functionalized NWs, 5 ppm for functionalized NWs with Pt NPs, to show the better sensitivity of the non-functionalized NWs to NO_2.
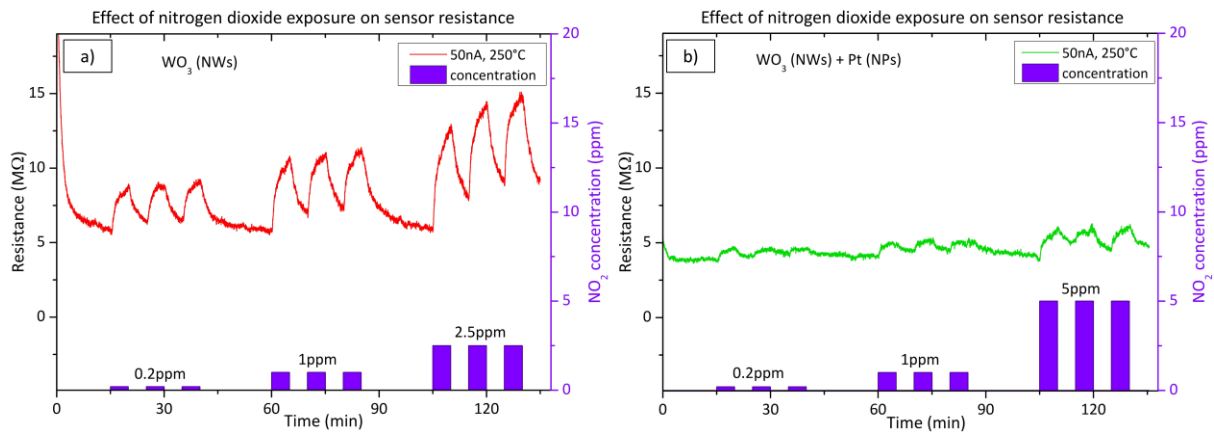
Figure 91. Effect of increasing concentration of nitrogen dioxide exposure (multiple) peaks (3x0.2 – 3x1 – 3x2.5 (5) ppm) on sensor resistance: a) non-functionalized WO_3 (NWs), b) functionalized WO_3 (NWs) with Pt (NPs).

Generally, the measured signal curve for the non-functionalized NWs showed a more intense reaction to NO_2 species than functionalized, accompanied with clear, stable, and repeatable behavior of the sensor response.

A similar procedure was repeated for EtOH, which unlike the previous sequence for NO_2, the lowest concentration with possible concentration error (given by the calibrated gas cylinders and by gas station system, MFC range) was 2.5 ppm and the maximum possible concentration 100 ppm (see in Figure 92).
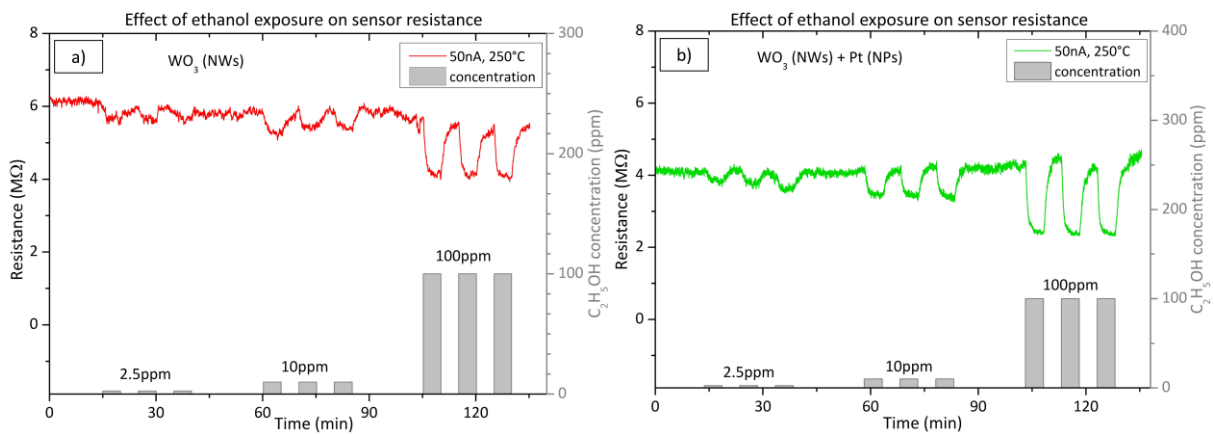
Figure 92. Effect of increasing concentration of ethanol exposure (multiple) peaks (3x2.5 – 3x10 – 3x100 ppm) on sensor resistance: a) non-functionalized WO_3 (NWs), b) functionalized WO_3 (NWs) with Pt (NPs).

The gas sensors showed consistently an increase or decrease of the electrical resistance after exposure to NO_2 (Figure 91) or EtOH (Figure 92), respectively, as noticed previously for other n-type MOX (including tungsten oxide) when exposed to oxidizing or reducing species [159]. These electrical resistance changes were proportional to the gas concentration (Figure 95) and reproducible, displaying similar characteristics (e.g., magnitude of the electrical resistance change and time of response and recovery) for the same gas concentration, as shown in Figure 91 and Figure 92.

After the gas sensing procedure including sequence of multiple peaks with increasing concentration, further measurements were performed in order to find out the ability of the gas

sensor to detect increasing and decreasing concentration that come after each other. Thus, another gas sequence for NO_2 is displayed in Figure 93, in which the stabilization of sensor resistance (SA) is 20 minutes, and the gas exposure time was prolonged from 5 to 10 minutes.
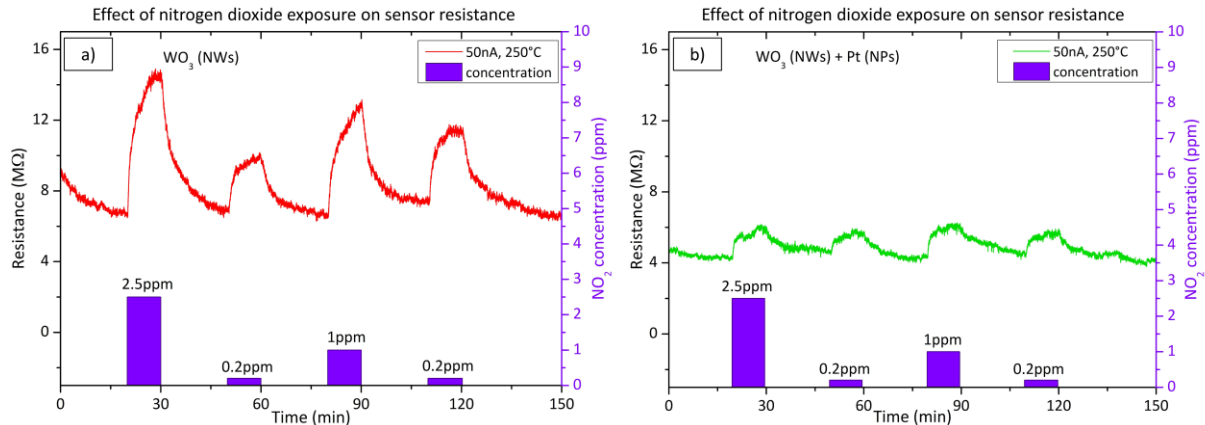
Figure 93. Effect of increasing-decreasing concentration of nitrogen dioxide exposure (single) peak (2.5 – 0.2 – 1 – 0.2 ppm) on sensor resistance: a) non-functionalized WO_3 (NWs), b) functionalized WO_3 (NWs) with Pt (NPs).

These results showed similar behavior of the resistance as in previous procedure for NO_2 (see Figure 93a) for non-functionalized NWs. The value differences between the first measured response to 0.2 ppm concentration and the second to the same concentration (0.2 ppm) are mostly caused by non-desorbed NO_2 species bounded in previous peaks. For this reason, the gas sensor needs longer recovery times to reach the baseline resistance, which fluctuates around 6 MΩ for the non-functionalized NWs. This is likely related to the need for higher thermal energy for desorption of NO_2 at the surface, which could not be performed due to the heater features. This also applies for the sensor with functionalized NWs (Figure 93b) in which the measured resistance during recovery time could not reach the baseline resistance that is about 4 MΩ.

Further, similar gas sensing procedure (sequence) was repeated for ethanol. These results are displayed in Figure 94.
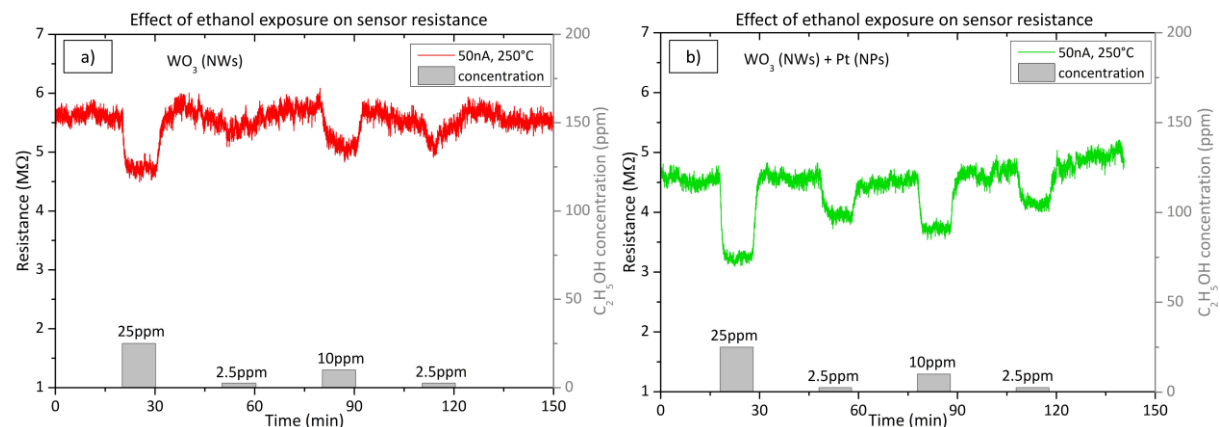
Figure 94. Effect of increasing-decreasing concentration of ethanol exposure (single) peak (25 – 2.5 – 10 – 2.5 ppm) on sensor resistance: a) non-functionalized WO_3 (NWs), b) functionalized WO_3 (NWs) with Pt (NPs).

The response and recovery of the gas sensor (based on non-functionalized or Pt-functionalized NWs) proved slower toward NO_2, as opposed to C_2H_5OH, particularly at a high NO_2 concentration (i.e., 2.5 ppm). Also, the recovery and response time of the non-functionalized NWs is longer compared to functionalized, which is consistent with the literature (described in detail in 1.2.5), which states the acceleration of chemisorption in metal oxide as a result of the addition of catalytic active sites, such as Pt NPs.

Summary of gas sensors response – material diversity role

The sensor response was defined as (R_{air}-R_{gas}/R_{gas}) for ethanol (reducing gas) and (R_{gas}-R_{air}/R_{air}) for nitrogen dioxide (oxidizing gas), where R_{air} is the sensor resistance in air at the stationary state and R_{gas} the sensor resistance after a defined time of analyte exposure. The sensor response toward NO_2 (oxidizing gas) and EtOH (reducing gas) for both non-functionalized and functionalized NWs are depicted in Figure 95.
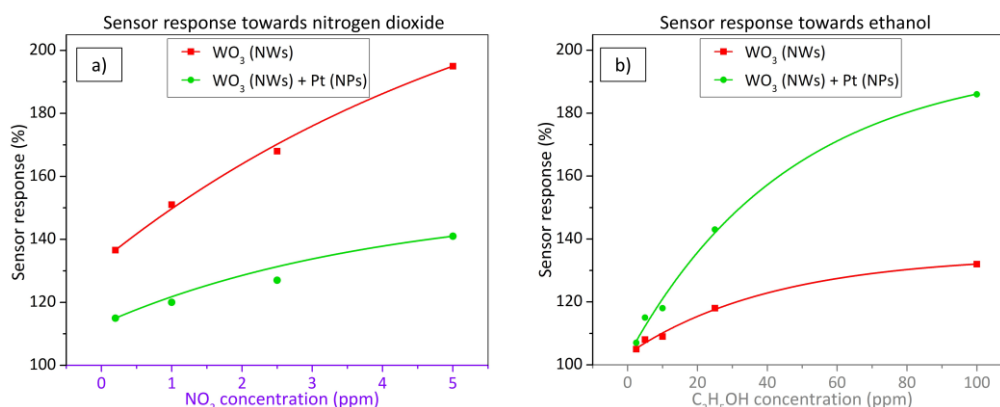
Figure 95. Sensor response vs. concentration curves of the sensor with non-functionalized and Pt-functionalized NWs toward: a) NO₂, b) EtOH.

Overall, the electrical resistance recorded on the sensors with non-functionalized NWs showed larger changes toward NO_2, as opposed to the sensors with Pt-functionalized NWs, which showed larger changes toward C_2H_5OH. For instance the sensor response toward 2.5 ppm NO_2 registered a value of approximately 168 % for the non-functionalized NWs and 130 % for those functionalized with Pt NPs, whereas the sensor response toward 100 ppm of C_2H_5OH, registered a value of approximately 132 % and 186 % for the non-functionalized and Pt-functionalized NWs, respectively (Figure 95). These results indicate better sensitivity to NO_2 for the sensors with non-functionalized NWs, in contrast to the Pt-functionalized NWs, showing consistency with the literature, which previously demonstrated that non-modified tungsten oxide in various forms (e.g., thin films, [160] nanoparticles, nanolamellas, [161] or nanofibers [162]) is more sensitive to oxidative species than reductive species, [159] even at low concentrations (e.g., 1 ppm [163]) and in the range of operating temperatures studied in this work. Similarly, these results show better sensitivity to C_2H_5OH for the Pt-functionalized sensors compared to those without functionalization, which is also consistent with previous reports in the literature that demonstrated the enhancement of sensitivity in n-type MOX

modified with Pt NPs (e.g., Pt@WO₃,[164-166] Pt@ZnO,[164] or Pt@TiO₂[167]) toward reductive species, including C_2H_5OH.

Further, a comparative table showing the sensor responses recorded in this work and the literature for other single-wire and multiple randomly connected wire systems toward NO_2 and C_2H_5OH is displayed in Table 11. This table is meant to provide a general idea of the properties of our sensors. Despite the complexity behind the comparison of the sensor outputs, which depend strongly on the fabrication and test set-up employed in each work. It is worth noting that Table 11 takes into account only the optimum condition reported in each work toward NO_2 or C_2H_5OH. Also, that the use of tungsten oxide for single-wire sensors is not frequent in literature, which is particularly focused on other MOX wires such as SnO_2, [168,169] In_2O_3 [19,111] or ZnO. [170] Based on this literature search, it is noticed that the developed sensors show better or similar responses than other single-NW systems reported previously (considering the gas concentrations tested).

The table also shows that the responses of single NW-based sensors have lower magnitudes compared to sensors based on multiple wires. This is attributed to the broader exposed surface area in multiple wires (as opposed to a single or few NWs), which allows for a higher number of gas molecules to impinge the surface and in turn amplifies the electrical output signal, as demonstrated previously when comparing the gas sensing performance of thin films and single-NW systems. [171]

Table 11. Summary of the sensor responses recorded in this work and the literature for sensors based on single and multiple nanowires toward NO_2 and C_2H_5OH.

Summary of the sensor responses – comparison of this work vs. literature						
Type	**Material**	**Features (nm)**	**SR (%)**	**Gas**	**ppm**	**Ref**
S-NWA	WO_3	$100^{\varnothing} 10000^{L}$	151	NO_2	1	This work
S-NW	SnO_2	$90^{\varnothing} 15000^{L}$	25	NO_2	0.5	[168,169]
S-NW	SnO_2	$78^{\varnothing}$	100	NO_2	100	[172]
M-NWs	WO_{3-x}	$50^{\varnothing}$	1560	NO_2	1	[173]
M-NWs	$W_{18}O_{49}$	$90^{\varnothing} 1000^{L}$	1304	NO_2	1	[174]
M-NWs	$W_{18}O_{49}$	$1000^{\varnothing}$	335	NO_2	1	[175]
M-NWs	WO_{3-x}	N/A	500	NO_2	5	[176]
S-NWA	$Pt@WO_{3-x}$	$5^{\varnothing NPs} 100^{\varnothing} 10000^{L}$	188	C_2H_5OH	100	This work
S-NW	In_2O_3	$220^{\varnothing} 5000^{L}$	47	C_2H_5OH	100	[177]
S-NW	CP	$220^{\varnothing} 6000^{L}$	0.15	C_2H_5OH	2000	[178]
M-NWs	WO_{3-x}	$100^{\varnothing} 10000^{L}$	300	C_2H_5OH	10	[179]
M-NWs	$Pt@WO_{3-x}$	$5^{\varnothing NPs} 100^{\varnothing} 10000^{L}$	450	C_2H_5OH	10	[179]
M-NWs	$Au@WO_{3-x}$	$30^{\varnothing NPs} 200^{\varnothing} 2000^{L}$	98	C_2H_5OH	4	[180]
S-NWA: single NW array, S-NW: single NW, M-NWs: multiple NWs (wire-based films), CP: conductive polymer, $^{\varnothing}$: wire diameter, ^{L}: wire length, SR: response ($\Delta R/R_0$)						

Further tests of the sensors toward other analytes including carbon monoxide (CO) and ammonia (NH_3) showed typical n-type semiconducting behavior during gas exposure (Figure S1 and S3). Generally, the responses to CO were negligible and the response to NH_3 registered lower cross-response (ΔSR) to C_2H_5OH and NO_2 for the Pt-functionalized nanosensors (ΔSR for C_2H_5OH 85 %, NO_2 85 %) as compared to the non-functionalized nanosensors (ΔSR for

C_2H_5OH 110 %, NO_2 79 %). A global view of the results (Figure 96), however, suggest better selectivity for the non-functionalized nanosensors to NO_2 respect to the reductive gases (C_2H_5OH, NH_3 or CO), as opposed to the Pt-functionalized nanosensors, which indicate poor selectivity to C_2H_5OH due to the strong interference with NO_2, although better selectivity for the reductive gases.
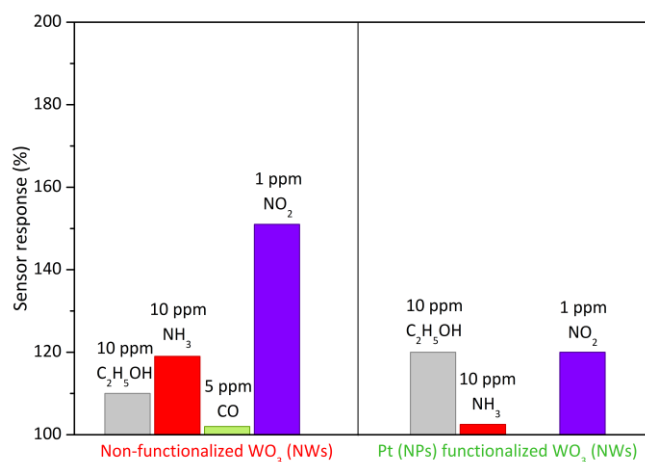
Figure 96. Summary of the sensor response toward various analytes including C_2H_5OH, NH_3, CO (reducing gases) and NO_2 (oxidizing gas) showing the possible cross-responses among them.

Gas sensing mechanism

The sensing results can be understood on the basis of the mechanism of chemical sensing on MOX surfaces, in which the pre-adsorbed oxygen species at the MOX react with gaseous analytes producing electrical changes in the MOX. Thus, when non-functionalized NWs are exposed to air, they adsorb oxygen molecules at their surface leading to the formation of different chemisorbed oxygen species (O_2^- at temperatures lower than 130 ºC, O^- at temperatures between 130 – 300 ºC and O^{2-} at temperatures higher than 300 ºC) [181-184] by capturing electrons from the conduction band that corresponds to the four equations described in receptor function in 1.2.2 (Equations (1.1), (1.2), (1.3), and (1.4)).

This, in turn, produces a depletion layer and an increase in the resistance of the tungsten oxide NWs, as illustrated in Figure 97a and Figure 97b. Similar mechanism works for the Pt-functionalized NWs (Figure 97c), although, due to the large difference in the work function of Pt (5.12 – 5.93 eV) [185] and bandgap of tungsten oxide (2.5 – 3.5 eV), [186] nano-Schottky barriers are formed at the interface of the Pt NPs and the tungsten oxide NW. This induces to an accumulation of electrons on the Pt NPs and the formation of holes on the tungsten oxide NWs, [167] thus resulting in an enlargement of the tungsten oxide depletion layer at the surroundings of the Pt NPs. Simultaneously, the catalytic Pt NPs also activate the dissociation of molecular oxygen and their distribution onto the surface of the NW. This effect, known as "spillover", described in 1.2.5, strongly increases the quantity of adsorbed oxygen species on the tungsten oxide surface (Figure 97d).
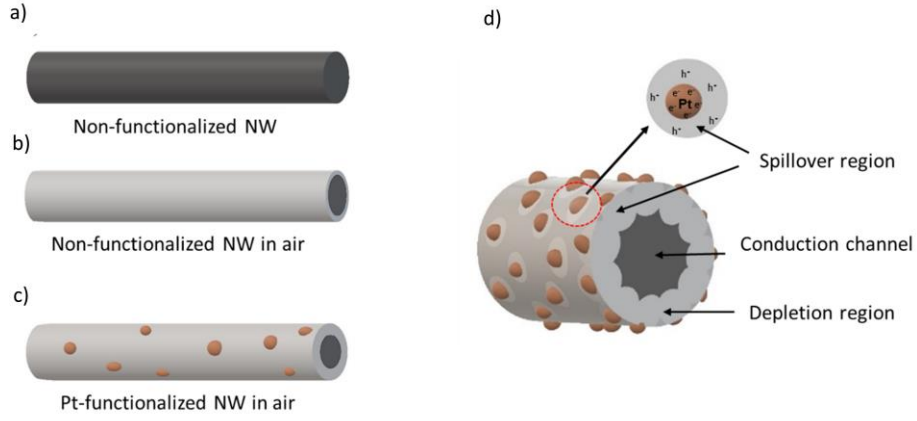
Figure 97. Illustration of gas sensing mechanism in single NW: a) fully conducting tungsten oxide NW, b) formation of depletion region around the NW when exposed to air, c) increase of the depletion region due to the Pt functionalization (NPs), d) formation of Schottky barriers at interface (NW – NP) leading to the spill-over effect and the enlargement of the depletion region in air.

After the exposure of the sensors to ethanol at 250 ºC, the following reaction paths are likely to occur at the surface dominated by pre-adsorbed O$^-$ [187-190]:

$$C_2H_5OH_{(gas)} \rightarrow C_2H_5O^-_{(ads)} + H^+_{(ads)} \tag{4.2}$$

$$2H^+_{(ads)} + O^-_{(ads)} \rightarrow H_2O_{(vapor)} \tag{4.3}$$

$$C_2H_5O^-_{(ads)} + H^+_{(ads)} \rightarrow C_2H_{4\,(vapor)} + H_2O_{(vapor)} \tag{4.4}$$

$$C_2H_{4\,(vapor)} + 6O^-_{(ads)} \rightarrow 2CO_{2(gas)} + 2H_2O_{(vapor)} + 6e^- \tag{4.5}$$

$$C_2H_5OH_{(gas)} + O^-_{(ads)} \rightarrow C_2H_4O_{(ads)} + H_2O_{(vapor)} + e^- \tag{4.6}$$

$$C_2H_4O_{(ads)} + O^-_{(lattice)} \rightarrow CH_3COOH_{(vapor)} + V_O \tag{4.7}$$
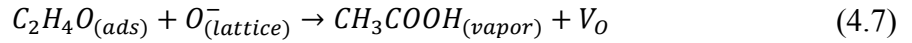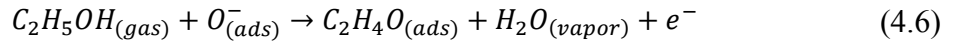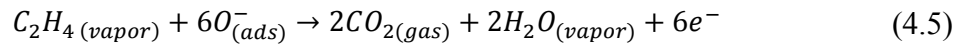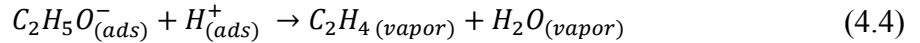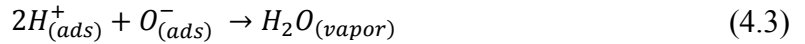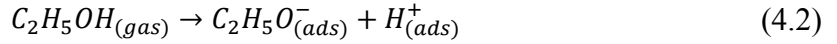
Generally, C$_2$H$_5$OH molecules are adsorbed on the surface of tungsten oxide via the oxygen atoms of the hydroxyl groups (Equation (4.2)), and the resultant H$^+$ ions react with O$^-$ ions (Equation (4.3)) to form water molecules, which are then desorbed. At elevated temperatures (>200 °C), the adsorbed ethoxy groups can also be decomposed into ethylene and water that later are desorbed from the surface (Equation (4.4) and (4.5)). EtOH can also be decomposed to acetaldehyde by reaction with the lattice oxygen with subsequent desorption of vapor of acetic acid and the release of electrons toward tungsten oxide due to the formation of oxygen vacancies (V$_O$) (Equation (4.6) and (4.7)). [187] In sum, the C$_2$H$_5$OH molecules adsorb at the non-functionalized tungsten oxide surface, providing electrons to reduce the adsorbed ionic oxygen and release the free electrons back to the tungsten oxide conduction band. This process reduces the width of the depletion region and increases the conduction of the tungsten oxide NWs.

A similar mechanism occurs for Pt-functionalized tungsten oxide during C$_2$H$_5$OH sensing, however with significant improvements in response to C$_2$H$_5$OH. First, due to the increment of pre-adsorbed oxygen as a result of the trap and accumulation of oxygen species at the Pt NPs and/or spill of these species over the NW surface. Second, due to the promotion and acceleration of the reactions described above at the Pt NPs, unlike the mechanism occurring at

the non-functionalized tungsten oxide surface. [191] Hence, in contrast to the non-functionalized NWs, the Pt-functionalized surface (that is covered with a higher amount of pre-adsorbed oxygen species) promotes the release of more electrons into the tungsten oxide conduction band during C_2H_5OH adsorption, consequently, the record of larger resistance changes in the Pt-functionalized nanosensors toward C_2H_5OH.

On the other hand, when the NWs are exposed to NO_2, the NO_2 molecules are adsorbed as NO_2^- (Equation (4.8)) capturing electrons from the tungsten oxide conduction band and reacting further with the adsorbed ionic oxygen (Equation (4.9)) to form nitric oxide and O^{2-} [192]:

$$NO_{2(gas)} + e^- \rightarrow NO_{2(ads)}^- \qquad (4.8)$$

$$NO_{2(ads)}^- + O_{(ads)}^- + 2e^- \rightarrow NO_{(gas)} + 2O_{(ads)}^{2-} \qquad (4.9)$$
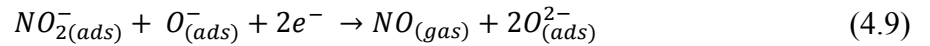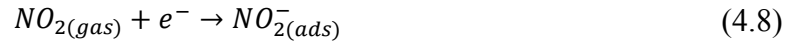
These reactions take electrons from the conduction band of the tungsten oxide NWs producing a wider depletion layer than that formed during the pre-adsorption of oxygen, which results in a further increase of the resistance along the non-functionalized wire. As for the Pt-functionalized NWs, due to these structures are more depleted of electrons after the pre-adsorption of oxygen, the NO_2 molecules exposed to this surface find fewer electrons in the tungsten oxide conduction band to be accepted and to form NO_2^- adsorbents, making the Pt-functionalized NW less sensitive to NO_2 than to C_2H_5OH, as noticed in the functional tests of these systems.

Obstacles overcame during gas tests

During the gas tests, there were several issues which either brought errors into the measurements or caused that the setup (e.g., current) could not be reproduced with the same conditions again. During the first stage of gas tests, the setup was adjusted to study the influence of current in the system in order to define the state in which the S/N ratio was acceptable. Also, to avoid the self-heating effect of the wires not to affect the operating temperature and the chemisorption. The effect of the current is displayed in Figure 98a, where the sensor response is significantly reduced due to an excessive current load (100 nA) flowing through NWs or present highly noisy signal for low currents (1 nA). This effect was minimized when using an intermediate current, for instance, 10 nA as shown in Figure 97a. The higher current through NWs could also create additional heating (Joule heating effect). This self-heating behavior is an effective feature to avoid the use of external heating system and/or reduce operational power. However, for the characterization of the sensor response, or NWs in use, without previous calibration, the self-heating could bring temperature errors. Thus, to avoid this effect the use of high currents during the measurements were avoided.
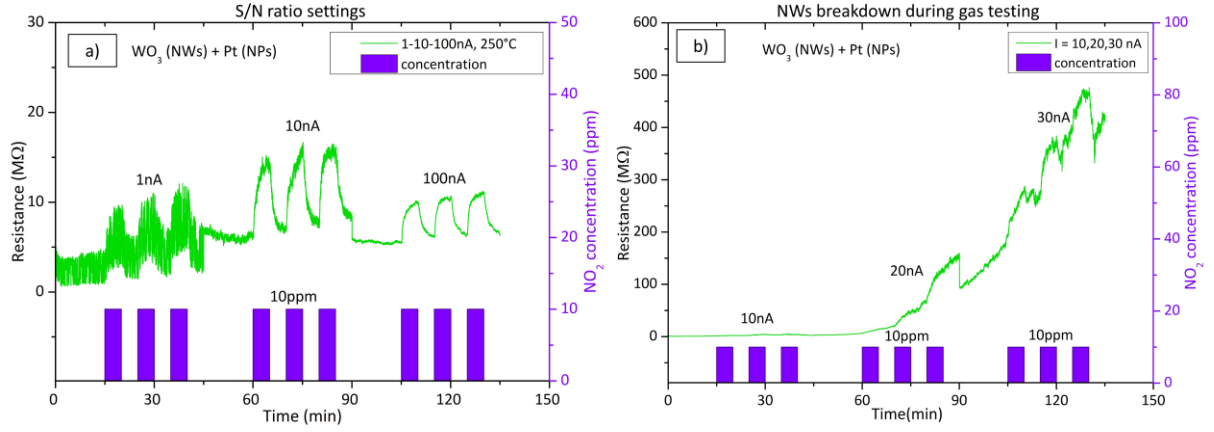
Figure 98. Recorded measurements from gas testing with nitrogen dioxide: a) S/N ration setting, b) NW breakdown.

Another issue to overcome during the tests was the burn out of the wires. Notice that the NW interconnection with faced nanoelectrodes tended to burn out due to the applied current mostly in poorly etched structures in structures with misalignment of the NWs as shown in Figure 99. Figure 99a displays the results from a system aged, in which part of the NW from the array were burned out, and thus the electrical resistance increased with them until near loss the measured signal at relatively low current (30 nA), as opposed to previous observations in Figure 99a. The relatively fast aging of these sensors prevented their use for further gas sensing tests.
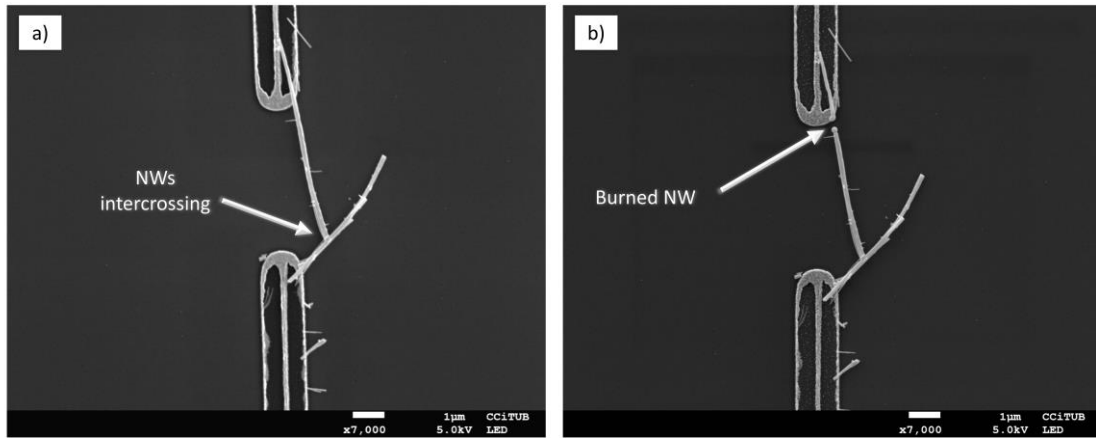
Figure 99. SEM inspection of burned NW: a) before gas testing, b) after gas testing.

Further characterization of the aged structure showed structural degradation of the Au/Ti electrodes layer, as is shown in Figure 100, which apart from the signal loss also brought additional signal noise into the measurement. According to the literature [193], the degradation of the electrodes could be connected with a diffusion phenomenon occurring at temperatures ranging from 200 to 400 °C in polycrystalline Au/Ti layers. It is worth notice that this issue was identified only on one processed wafer, in which the e-beam lithography and followed fabrication steps (e.g., IBE) could be considered unsuccessfully executed, taking into account the state of the nanoelectrode (see in Figure 100b). In this context, the layer exhibits signs of the mechanical erosion, which could have made during the sonication, but also by applied current (electromigration) and/or as a result of many factors related to chosen deposition

technique (magnetron), for instance, deposition rate, initial/deposition pressure and so forth. [194]
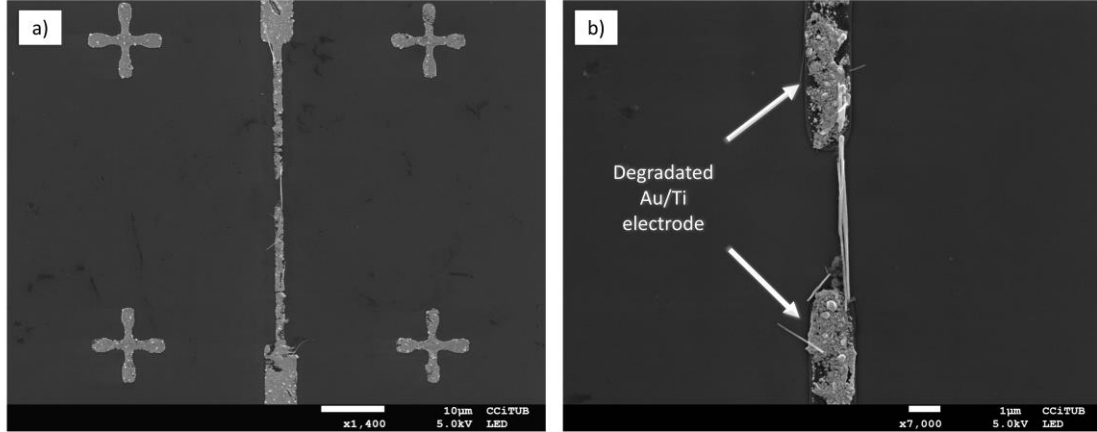
Figure 100. SEM inspection of degraded Au/Ti electrode: a) distant view, b) closer view.

4.5 Summary

This chapter discussed the processing steps and results of the second chip generation, which consist of nanoelectrode array systems with the thickness of the electrode comparable to the diameter of NW. These systems contributed to: (1) selective integration of various kind of NWs, (2) single NWs alignment in parallel using DEP, and (3) characterization of its gas sensing properties. Generally, the second chip generation includes two nanoelectrode arrays platforms, both with size 5x5 mm, made by two different fabrication approaches: (1) lift-off process that uses only depositions over a pattern, and (2) etch-back process using combinations of deposition and (dry) etching techniques.

The design of the chip fabricated by lift-off approach consisting of a variety modification of the nanoelectrode array, since this design was a basic proposal (design test chip) of the second generation made in order to adjust several fabrication procedures. Each chip contains four nanoelectrode arrays (resistive topology) with a different number of faced electrodes ordered in parallel (15, 30, 45, and 60), and with a minimum width of the electrode end 75 nm. Two other topologies were designed, namely, FET topology with one additional electrode, and 4-wire topology that add two more measurement electrodes passing through the center between faced electrodes. The fabrication process of these chips was performed using small square (2x2 cm) silicon substrates, which were cut from 4-inch wafers. Thus, two lift-off processes, including pattern of the microelectrodes made by DWL, pattern of the nanoelectrode fingers (EBL), and two conductive layer depositions over the pattern, were employed to create nanoelectrode arrays with metallic interconnection (junction). Although the fabricated electrodes comprised fence-like structures (redeposited material on resist sidewalls), results demonstrated the ability of selective integration of single NWs into the array with nanoelectrodes.

The design of the chip using the etch-back process for the fabrication is a revised version based on previous design, in which four nanoelectrode arrays were preserved and their design underwent only minor changes (optimized design chip). For example, the nanoelectrode fingers were made in four modifications with electrode width 100, 150, 200, and 300 nm. Also, some of the measurement electrodes and other structures were removed from the final design. Then, the optimized design, including resistive and FET electrodes topology, was fabricated using 2-inch wafer technology with several fabrication processes, in which the nanoelectrode fingers were made by dry etching of the microelectrodes through EBL pattern. Whole electrode system, except for nanoelectrode fingers, was deposited by 250 nm additional dielectric layer (SiO_2) to protect the microelectrodes from NWs capturing during the DEP process.

Subsequently, the gas sensing elements were fabricated using optimized design chip and backside ceramic heater assembled on TO-8 package. The heating element reaches a maximal operating temperature between 270 and 280 °C, and it is based on thick-film technology with designed heating area 6x6 mm. Generally, the nanoelectrode arrays employed in the gas sensing characterization consisted up to 5 single NWs (WO_3 NWs non-functionalized or Pt-functionalized) aligned in parallel, and results proved the integration process success rate of approximately 33 % in the arrays with 15 faced electrodes. Characterization of these sensing elements proved a reproducible behavior with the Pt-functionalized NWs, showing a better response to ethanol (C_2H_5OH), compared to the non-functionalized NWs systems, which responded better to nitrogen dioxide (NO_2). Summary of recorded sensor responses compared with that recorded for other sensing elements based on similar systems (single and multiple NWs) toward NO_2 and C_2H_5OH, was presented in Table 11. Further tests of the systems toward other analytes including carbon monoxide (CO) and ammonia (NH_3) showed typical n-type semiconducting behavior during gas exposure. Generally, the response of the samples to CO were negligible and the response to NH_3 registered lower cross-response (ΔSR) to C_2H_5OH and NO_2 for the Pt-functionalized systems (ΔSR for C_2H_5OH 85 %, NO_2 85 %) as compared to the non-functionalized systems (ΔSR for C_2H_5OH 110 %, NO_2 79 %). Summary of the sensor response toward various analytes and their cross-responses is presented in Figure 96.

A global view of the results suggests better selectivity for the non-functionalized NWs to NO_2 respect to the reductive gases (C_2H_5OH, NH_3 or CO), as opposed to the Pt-functionalized NWs, which indicate poor selectivity to C_2H_5OH, although better selectivity for the reductive gases in general. In conclusion, the gas sensing tests of the second chip generation validated the functionality of the fabricated system.

5 Third chip generation: Advanced nanoelectrode array platform for enhancing of gas sensing properties based on three electrodes configuration

Similarly to the first chip generation, the tests of the second chip generation unfolded several deficiencies, which were amended in the third chip generation. For instance, in the second chip generation, the alignment of single NWs was practically feasible only in arrays with 15 faced electrodes; the other arrays were too large, and so the evaporation of the drop caused NWs agglomeration (presented in 3.2.2), mostly on the outer faced electrodes. To eliminate the fast evaporation during the integration process, it was determined that more water needed to be added on the array's area, so more NWs were aligned. This, however, increased the probability of getting multiple NWs interconnection, or bundles of interconnected NWs. Therefore, the proposed solution for the third chip generation includes the (1) shortening of the electrode arrays, and (2) the change of shape of the hydrophobic barriers, which keep the drop in the middle of the array during the DEP. Other improvements of the new design also include the reduction of the area of the dielectric windows to increase the probability of aligning only a single NWs between the faced electrodes.

In sum, the third chip generation was designed primarily to improve the integration of single NWs via DEP and enhance the gas sensing properties of the systems using the FET (field-effect transistor) arrangement enabled by the third electrode. Thus, the third generation chip consists of bottom (buried) gate electrode, as opposed to other systems with a top gate electrode, which their usage would require the change of the sensor assembly process together with developed fabrication procedure, as described in [195,196]. The new design was developed almost from the beginning keeping only some of the design parameters used for the second generation, such as spacing between faced nanoelectrodes and the electrode gap. Due to a buried electrode the fabrication process required many more steps than in the second generation, for example, the creation of a gate channel for the gate electrode, deposition of the gate electrode, or opening windows for pads covered by gate dielectric layer. For this reason, optimization of a multi-step nanofabrication process was necessary. In other words, the low series fabrication process was turned into the advanced fabrication process, in which more silicon wafers were employed in the individual procedures, in order to ensure higher throughput and reliability of the fabrication.

The gas sensing characterizations were performed in a new test chamber developed in the frame of this thesis for low-current measurement. The new chamber was addressed to reduce the dead volume (that is basically the empty space around the gas sensing elements in the chamber) and thereby to improve undesirable processes, which could influence negatively the ongoing sensor characterization. For instance, (1) small exchange rate, (2) poor spreading of the gas, or (3) high adsorption on the surface chamber walls. Therefore, the chamber fabrication process was divided into two independent device forming fabrication processes, namely, the fabrication of chamber body and its inside structures (mechanical part), and the fabrication of

PCB for the electrical interconnection with measuring devices (electrical part). Design, fabrication, and interconnection of this chamber with gas station system are presented in detail in this chapter.

The tests of the third chip generation were performed using non-functionalized (pristine) WO_3 NWs, which were integrated into the advanced nanoelectrode array platform for operation providing NWs channel modulation. The gas sensing system was fabricated using the same heating elements than for the second chip generation. Reducing and oxidizing gas was used to characterize the gas sensing responses performed with FET arrangement, although only resistive measurements were also carried out to validate initially the structures. In sum, the tests were focused on the effect of the gate voltage potential (negative or positive) on sensor performance (section 1.3.3.2).

To sum up, the third chip generation implements the improvements required in the previous two generations showing the experience acquired in the thesis. The third generation chip provides electrode arrays for single NWs alignment in parallel and gas sensing in FET arrangement. Thanks to the optimization processes, this nanoelectrode platform is ready to integrate various types of NWs, which in the combination with sensing channel modulation by gate voltage, could be able to create highly sensitive and selective gas sensing systems.

5.1 Experimental and methods

This section presents the design and fabrication of three-electrode systems based on the concepts developed in previous chip designs, including faced nanoelectrodes in arrays with buried third electrode passing through its center. The third chip generation of assembled sensing elements was tested in the presence of reducing and oxidizing gas as previous generation. The work related to the third chip generation sensor also includes the design and fabrication of a new TO-8 gas chamber for low-current measurement installed at the FEEC laboratory of LabSensNano scientific group.

5.1.1 Design concept and specification of the advanced nanoelectrode arrays and other functional blocks on the chip

The design concept of the third chip generation is based on elements previously used in the second generation, i.e., nanoelectrode arrays for single NW alignment procedure, hydrophobic elements, fabrication marks, labels and so forth. The size of the chip is 5x5 mm as it was in the case of the second generation. As stated previously, the third generation is designed primarily for the enhanced resistive (gas) measurement with an additional third electrode (FET topology). The third electrode is buried under the SiO_2 layer in the first steps of the fabrication process, unlike the second chip generation design in which the third additional electrode was made in the same fabrication step as other structures, such as pads, and electrodes. As in the previous generation, the design of the individual blocks are described in Figure 101 and Figure 102 below:

- *Chip generation and wafer identification labels* are situated in upper and lower parts of the chip (shown in Figure 101a and b). Besides chip generation identifier, some labels give an overview about the current chip number and wafer number identification which are helpful to recognize the modification, the current state of the individual layers, or their manipulation in different processes such as NWs alignment, wire bonding or gas sensing.

- *Four electrode arrays* divide the chip into four parts. Each array is an independent electrode system which is identical with other arrays. Four doubled pads on sides are parts of the array that are used for wire bonding (labeled D, S, G, H, 300x300 µm, see in Figure 101d). There are only small differences in the inside areas that are described further.

- *Measurement structure for characterization of thin-film layer properties* is located on the left side of each chip (shown in Figure 101c). This structure (so-called Van der Pauw) was designed to measure the resistivity of thin layers by van der Pauw method, which is an analogy to the four-point measurement technique. A standard measurement structure is extended by four additional pads and two wires with different width (designed to be about hundreds of nm) for further usage as a temperature sensor during gas measurement.

- *Cut marks with global and local marks* for the third generation remain the same than the second generation as described in 4.3.1 (depicted in Figure 101e, f). They are placed in each corner of the chip.
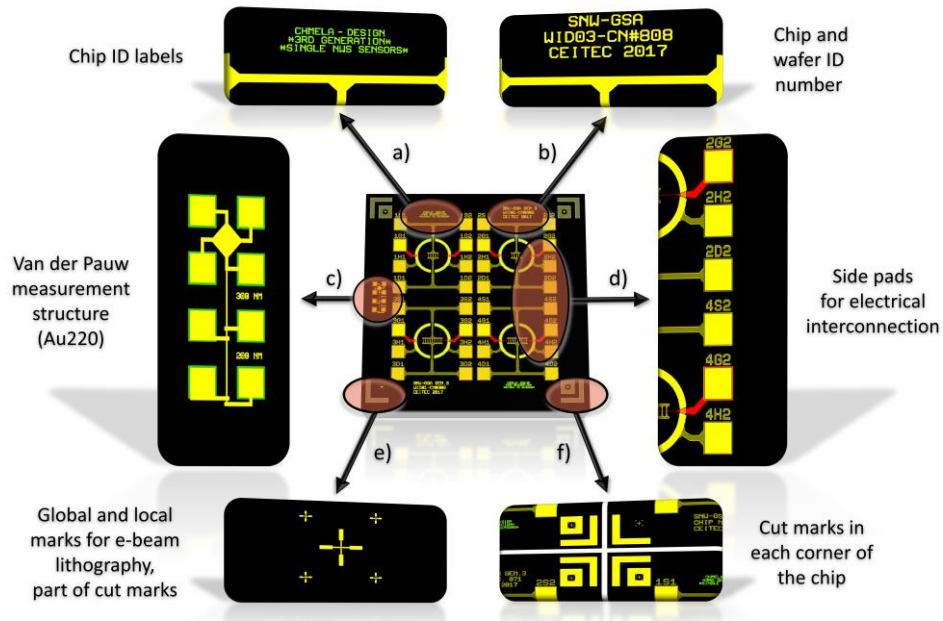
Figure 101. Third chip generation layout – general view of side structures organization (colors: yellow – electrodes (gold layer), red – gate electrode, green – open windows pattern, black – thermal oxide layer (SiO$_2$)): a) chip generation ID, b) wafer ID and chip number, c) Van der Pauw structure (Au220), d) side pads organization, e) global and local marks for EBL, f) cut marks.

The design of the third chip generation is more unified and contains only a few topology modifications in contrast to the second generation. The design of the individual structures (e.g., specification of the nanoelectrode finger or the number of parallel electrodes in the array) is described closely below:

- *Electrode array specification* – the electrode array is made of the same parallel ordered electrodes (finger pairs) which were used in the second generation, but the number of the electrodes is five in the upper part of the chip, and nine electrodes in the lower part (depicted in Figure 102a, e). The spacing between the parallel electrodes remains 50 μm, and the gap between faced nanoelectrodes is 3.5 μm. The local cross-marks, which were used for automatic XY offset calibration procedure (EBL), were excluded from the design inside of the write-fields. Instead, the global marks (part of the cut mark) are used for this purpose. Width of wires toward the array (incoming wires) connected to pads was enlarged, inside the hydrophobic ring to 25 μm and outside of this area to 50 μm.

- *Hydrophobic rings* are designed to keep a water drop with NWs placed on the electrode array during the DEP. The drop size fits better and covers a whole array area due to the circular shape that is closer to the natural shape of the drop after the contact with a wafer surface. The circle diameter is 700 μm, and the width of the ring line is 50 μm for the Ti/Au layer (shown in Figure 102b), 70 μm for the opening windows (fabrication Step 9 in section 5.1.2) into the SiO_2 dielectric layer covering the gold layer, respectively.
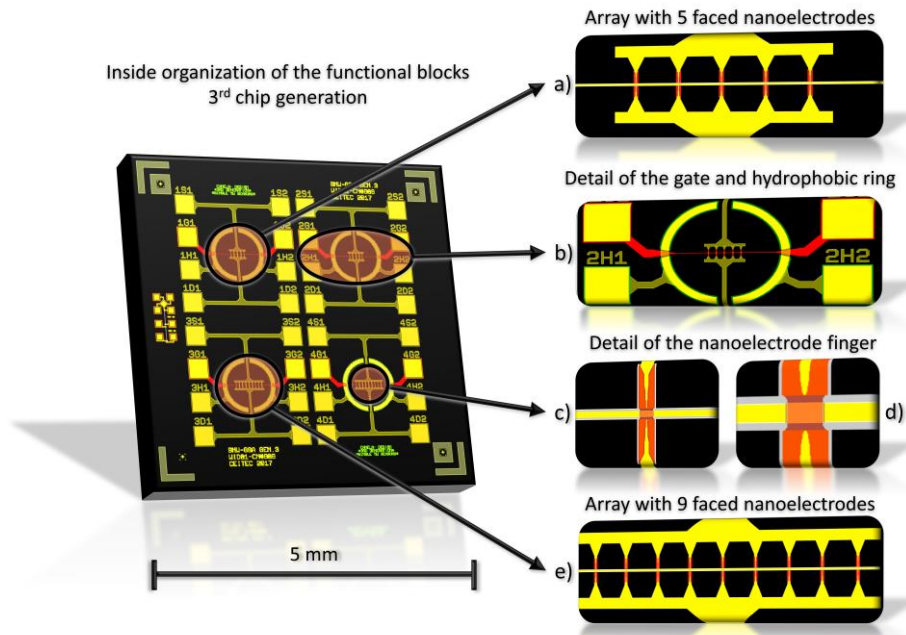
Figure 102. Third chip generation – the inside organization of the functional blocks (colors: yellow – electrodes (gold layer), red – gate channel, orange – EBL pattern, green – open windows pattern, black – thermal oxide layer (SiO_2)): a) array with 5 faced nanoelectrodes, b) detail of the gate and hydrophobic ring, c) detail of the nanoelectrode finger (colors: yellow – electrodes, red – EBL pattern), d) detail of the gate electrode at the crossings with nanoelectrodes (colors: yellow – electrodes, red – EBL pattern, grey – gate channel), e) array with 9 faced nanoelectrodes.

- *Electrode finger dimensions* – the entire electrode finger is 48 μm long in total. It is divided into three parts that start with triangular shape part from incoming electrodes followed by a small part of the middle electrode and nanoelectrode, which ends at the gate channel (trench) boundary. Nanoelectrode arrays are created as a first part by EBL and following etching procedure and its design resembles the shape of a clothes peg (shown in Figure 102c and the closer view is presented further in the fabrication), where

the red color represents the EBL pattern, and the yellow color is the remaining nanoelectrode ends. The nanoelectrode finger is made in two modifications; namely, two left arrays have a width of the ends 200 nm and two right arrays 300 nm.

- ***Design of buried gate electrode*** is depicted in Figure 102b in a distant view of the electrode (red color) which begins on the side pads, continues under the hydrophobic ring and ends with microelectrode in the middle of the array. Generally, the gate electrode is located in the gate channel (trench), which is designed about 2.5 μm thicker than the electrode, unlike the smallest part passing between the nanoelectrode array. In this area, the channel is 3.5 μm thick, and the thickness of the gate electrode is 1.5 μm (see in Figure 102d), where the gray color is the gate channel (trench in SiO_2 dielectric layer), and yellow is the gate electrode itself.

5.1.2 Fabrication of advanced nanoelectrode array structure with a buried gate electrode using high throughput techniques

As described in the section dedicated to the design, the fabrication of the third chip generation comprises a buried electrode which, in turn, requires several additional fabrication steps, for example, the formation of a gate channel for the gate electrode, or opening windows for pads covered by gate dielectric layer. In other words, due to the advanced fabrication process, which contains several fabrication steps (e.g., lithography, etching and deposition), some of the fabrication processes were changed in order to ensure higher throughput and reliability of the fabrication process. Similarly to the previous generation, some of the fabrication processes and their parameters, which were already described in the experimental part of previous chips, are only referenced in this section. The new processes (fabrication steps which were not used before) are described below in detail.

Fabrication procedure of third chip generation

1. **Substrate processing**

The fabrication of the third chip generation was performed on 4-inch silicon wafers equipped with 300 nm thick thermally grown silicon dioxide layer. The substrate was cleaned by the same cleaning procedure as was used for the second generation, i.e., wet cleaning, evaporation, and oxygen plasma.

2. **Optimization of throughput technologies usage – lithography and development of a positive tone photoresist**

As was stated previously, in order to reach a higher throughput of the fabrication process, the direct-write lithography technique was changed to the through-mask lithography. DWL was used to transfer the pattern onto 5-inch chrome photomasks coated with 500 nm photosensitive layer (MicroChem, S1805®) with which were performed a multi-step lithography production

by Süss MicroTec mask-aligner MA8 in both contact mode (vacuum contact, structures around 1 µm) and proximity mode (exposure gap, bigger structures above 2 µm).

The positive tone photoresist AR-P-3540 coating and developing procedures were optimized using Süss MicroTec RCD-8 semi-automatic programmable station. This station provides homogenous resist coatings. The coating procedure comprises a backside rinsing process as well as edge rinsing, which is an important step to remove the resist from the wafer's edge. DWL technique has no problem with thicker resist layer on edge caused during applying the photoresist which is drying while the wafer rotates, but for the through-mask technique this can be a problem (in a vacuum, or hard contact mode) resulting in wafer breakage, or worse, photomask damage. The developing process was realized with RCD-8 development system in puddle regime. AR-300-47 was used as developer mixed with DEMI water in 1:1 ratio.

In Figure 103b is depicted the layout of the testing structure for the optimization of the positive photoresist. As was stated in 2.1.3, AR-P-3540 is a highly sensitive and high-resolution resist that was required in some lithography steps and allows the possibility to reach 1 µm detail, e.g., for the local marks or gate electrode fabrication. A real structure of the testing pattern showing a positive and negative pattern of rounds and squared lines with resolution from 1 µm to 10 µm is shown in Figure 103a. The parameters of the exposure were set from datasheet values (120 mJ/cm^2).
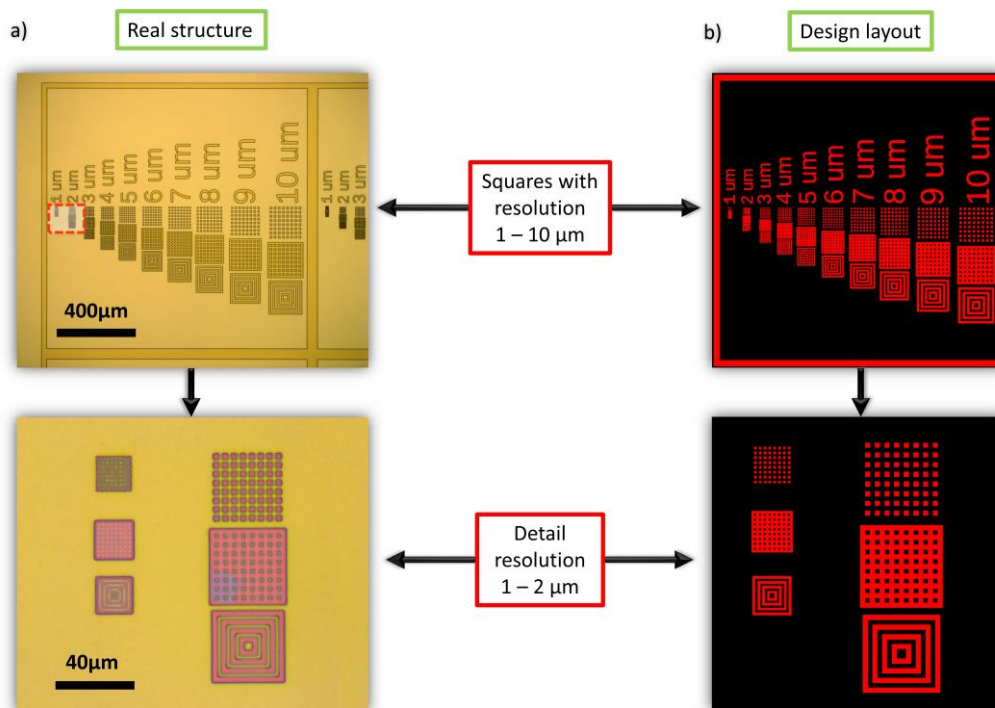
Figure 103. Resolution testing structure for positive photoresist AR-P-3540: a) real structure depicted under an optical microscope, b) design layout.

3. Etching of gate channel trench - channel for buried gate electrode (1st photolithography, 1st etching)

In a first step (Step 1), the wafer was coated with the adhesion promoter, a photoresist (AR-P-3540) using RCD-8 tool as a spin-coater. The process was carried out with the same parameters (rotation speed, time of coating and rotation and so forth) as with the simple Labspin6 coater in the second generation. After that, the pattern of the first layout was transferred to the coated wafers that were exposed through a mask with a first layout (see in Figure 104a) using Süss MicroTec mask-aligner MA8 in hard contact mode and conditions evaluated in the previous step. Then, the substrates were developed in puddle mode procedure with the developer (AR-300-44) that was performed by using RCD-8 tool (in developer mode). The DESCUM process was done under the same conditions as referenced in Table 6, but to remove resist residues about 100 nm thick, the process took the double of time (i.e., 5 min). The result of the process is depicted in Figure 104b, where the purple color is the exposed pattern, an uncovered area (SiO_2) that is prepared for etching, respectively.
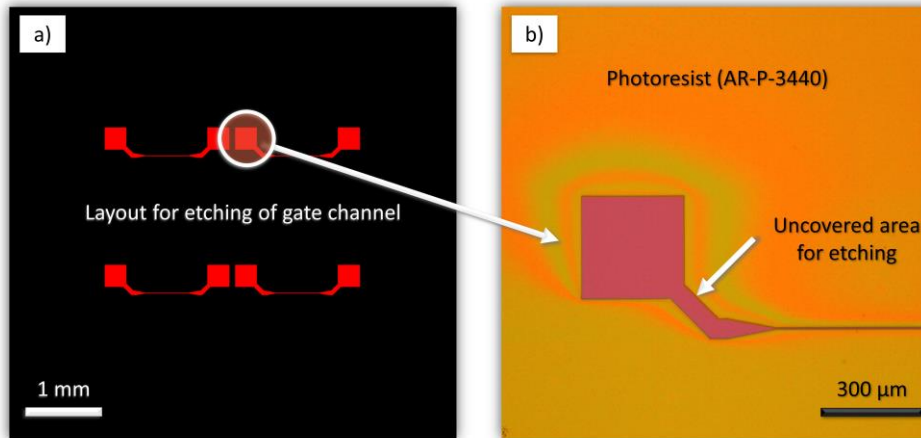
Figure 104. Illustration of Step 1 – preparing of the channel for buried gate electrode: a) one chip design layout (red color – current lithography pattern), b) prepared resist pattern with uncovered area for etching of the gate channel.

The channel for the gate electrode was performed using Oxford Plasma – NGP-80 Reactive-ion etching system (RIE) which was used in fluorine mode, with the presence of CHF_3 gas, respectively. An individual parameters setting of silicon dioxide etching process were provided from Oxford Plasma recipes, but in order to find the exact etching rate, the etched depth on the pad of the prepared channel for gate electrode was carried out using profilometry, as it is depicted in Figure 105.
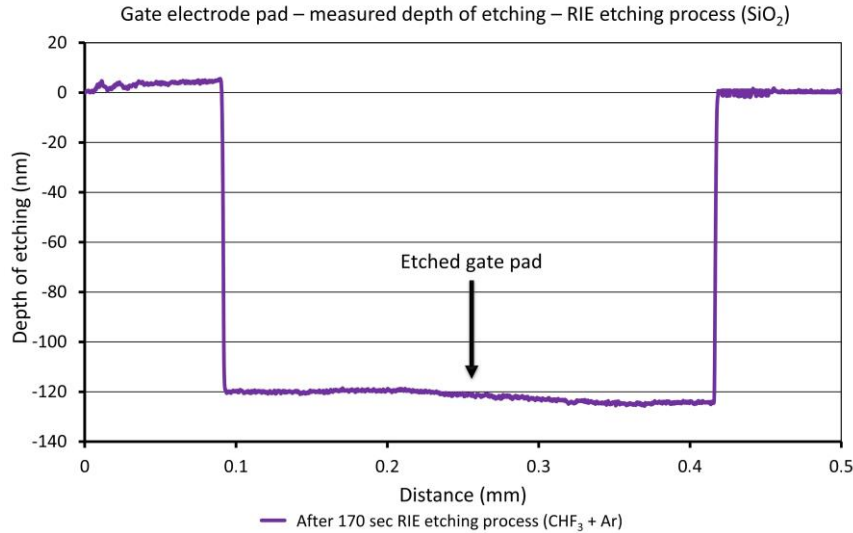
Figure 105. Profilometry measurement of the channel on the gate pad after the RIE process.

Unlike the IBE process, in which the redeposited fences (as it was described in 4.4.1) occurs at the edges of structures, the RIE process avoids these unwanted remains. This is confirmed in Figure 105 above, where no fences are visible after the silicon dioxide etching, and the measured profile is sharp and straight. The parameters of the process are listed in Table 12. The etching rate was counted by time of the process and the thickness of the removed layer. Thus, when the process conditions were known, the channel about 100 nm depth was etched into the silicon dioxide layer of the prepared wafers.

Table 12. Parameters of SiO₂ dielectric layer etching using reactive-ion etching system (RIE).

Reactive-ion etching – Oxford Plasma – NGP-80 (RIE)	
Parameter	**Material**
	SiO$_2$
DC Bias Voltage (V)	100
Forward/Reflected Power (W)	200/0
Strike pressure (mbar)	90
Etching pressure (mbar)	40
Ar flow (sccm)	38
CHF$_3$ flow (sccm)	12
He backing flow (sccm)	5
Etching rate (Å·s^{-1})	7.35

4. Deposition of Ti/Au conducting layer into the channel – gate electrode (2nd photolithography, 1st deposition)

The conditions of the lift-off process used in the fabrication of the second chip generation required improvements to avoid the redeposition of resist on the sidewalls, and thus prevent unwanted effect such as fence-like structures (hundreds of nanometers height), which are particularly undesirable in the area between the electrodes, under the single NW, respectively. As a result, two key processes in the fabrication procedure were modified in the third chip generation and changed to another more appropriate techniques. These changes are described below.

Firstly, for the fabrication of the temporary mask, it was used double-stack resist (two layers system) with a transparent bottom resist not light sensitive and positive (or negative) top resist which is exposed during lithography. This system is advantageous as it avoids the formation of fence-like structures. Its usage, however, lowers the resolution of the photolithography, which is a disadvantage of this system. For this reason, AR-BR-5480, which is approximately only 0.5 μm thick, was used as the bottom resist to ensure minimal resolution for the top resist around 1.5 μm. This resolution is necessary to reach because of the width of the gate electrode.

The second technique, which was changed in the fabrication procedure of the lift-off process is the deposition technique. Generally, the deposition of thin-film layers by using magnetron or IBAD systems has its advantages. However, for the realization of the pattern using lift-off process evaporation technique is preferable. The rationale of this is connected with the lower energy and direction of moving particles toward the substrate. By this technique, the deposited particles have a lower probability of being stuck at the walls of the resist and form fences (see Figure 40b). The parameters of the deposition using ultra-high vacuum e-beam evaporation system are listed in Table 13.

Table 13. Parameters of Ti/Au thin film layer deposition using UHV evaporation system (E-beam evap.).

PVD deposition – BESTEC – UHV evaporation system (E-beam evap.)		
Parameter	**Material**	
	Ti	**Au**
Beam Voltage (kV)	8	8
Emission Current (mA)	100	375
Initial pressure (mbar)	$2.5 \cdot 10^{-8}$	$8 \cdot 10^{-8}$
Deposition pressure (mbar)	$3 \cdot 10^{-7}$	$6 \cdot 10^{-7}$
Substrate rotation (rpm)	10	10
Deposition rate ($\text{Å} \cdot \text{s}^{-1}$)	1.2	3.5
Layer thickness (nm)	3	97

After the deposition of Ti/Au conductive layer of 100 nm thick in total, the wafer was immersed in the PG remover bath with structures upside-down and left for 1 hour in the bath enhanced by sonication. Subsequently, the wafer was immersed in two IPA baths (dirty/clean), rinsed under DEMI water stream and dried by nitrogen (lift-off process). Then, the plasma cleaning procedure was performed for 1 hour (see in Table 4). The result of the first lift-off process is depicted in Figure 106b, and the detail that depicts a precise alignment of the 1.5 μm gate electrode into 3.5 μm gate channel is seen in Figure 106c.
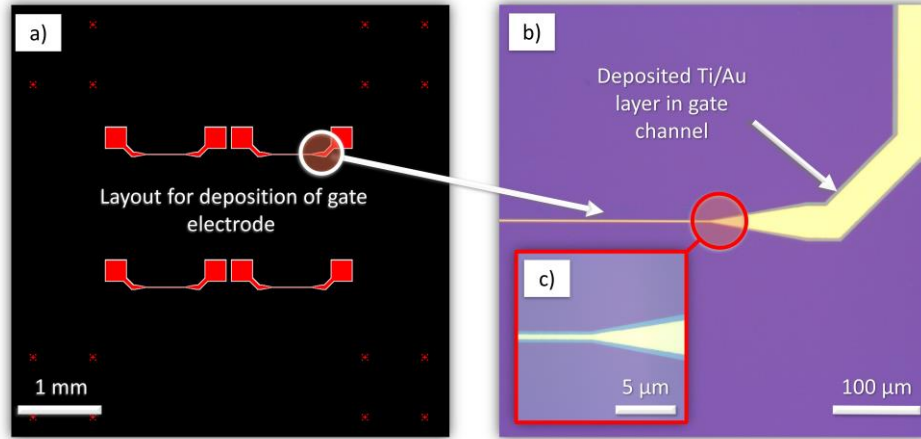
Figure 106. Illustration of Step 2 – deposition of Ti/Au conductive layer into the gate channel: a) one chip layout (red color – current lithography pattern), b) deposited gate electrode, c) detail of the precisely deposited gate electrode.

5. Deposition of the dielectric double-layer HfO₂/SiO₂ – stacked gate oxide and opening windows process (3rd photolithography, 2nd deposition, 2nd etching)

After intensive cleaning procedure, a dielectric double-layer of hafnium dioxide (10 nm) and silicon dioxide (90 nm) were deposited over the entire wafer (without resist) by using atomic layer deposition (ALD) Ultratech/Cambridge Nanotech Fiji 200 system. The deposition was performed at 200 °C in plasma mode, which allowed the creation of high-quality thin-layers at a lower temperature. This double-layer was chosen based on previously published works that recommend the use of double layers for the gate oxide in FET systems. [197] Nowadays, as was stated in [198], the usage of high-κ dielectrics on the gate contact is preferable (or the combination with SiO_2), especially, due to the elimination of the leakage current, which is the main undesirable effect. In this context, theoretically, it is possible to reach breakdown voltage more than 100 V, when the thickness of the double-layer is about 100 nm [199]. The parameters of the stacked gate oxide deposition are noted in Table 14.

Table 14. Parameters of HfO₂/SiO₂ dielectric layer deposition using atomic layer deposition system Ultratech/Cambridge – Fiji 200 (ALD).

CVD deposition – Ultratech/Cambridge Nanotech – Fiji 200 system (ALD)		
Parameter	**Material**	
	HfO₂	**SiO₂**
Temperature (°C)	200	200
Plasma power (W)	300	300
Deposition pressure (mbar)	$\sim 3 \cdot 10^{-1}$	$\sim 3 \cdot 10^{-1}$
Pulse (sec)	0.4	0.25
Deposition rate (Å/cycle)	0.9	0.63
Cycles (-)	111	1428
Layer thickness (nm)	10	90

Afterward, the dielectric layer was removed from the area of gate pads. This fabrication step is called opening windows, and the layout for the photolithography, which was performed with the positive tone resist (AR-P-3540), is depicted in Figure 107a. Buffered hydrofluoric acid (BHF or BOE) in 12:1 volume ratio solution was used for etching of SiO_2 layer, and a

10 % HF solution for HfO$_2$ etching. The etching rates of these solutions exceeded about 1.5 times. This rate was estimated based on previous literature [200,201] to assure full etching of the layer thickness. In addition, the etching effect was verified by measuring the gate resistance using (pad-to-pad) probe stations system Cascade Microtech MPS150 connected to parameter analyzer Keithley 4200-SCS. Figure 107b shows the Ti/Au layer pad scratched by the measuring probe tip after the electrical test.
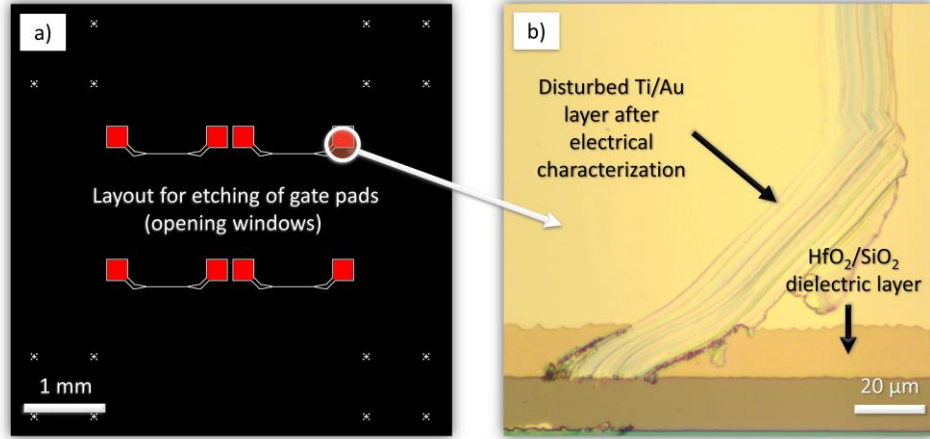
Figure 107. Illustration of Step 3 – deposited HfO$_2$/SiO$_2$ dielectric layer and the opening windows process: a) one chip layout (red color – current lithography pattern), b) depicted etched area at the edge of gate electrode pad after the electrical test.

6. Deposition of Ti/Au conductive layer – conductive layer for electrode system and cross-marks covering (4th photolithography, 3rd deposition)

In this fabrication step, the entire wafer was deposited with 100 nm (3/97 nm) thick conductive layer of Ti/Au using e-beam evaporator with parameters listed in Table 13 (deposited layer over the wafer, see in Figure 108b. The cross-marks located at the corners as a part of the cut-marks, which were masked in previous lithography step by double-stack resist are also seen in the layout pattern in Figure 108a. The cross-marks masking was performed with negative tone resist AR-N-4340 in combination with AR-BR (transparent bottom resist), similarly to the procedure listed in fabrication Step 2. After the deposition, the lift-off process was carried out to remove the resist from cross-marks, as it is depicted in Figure 108c.
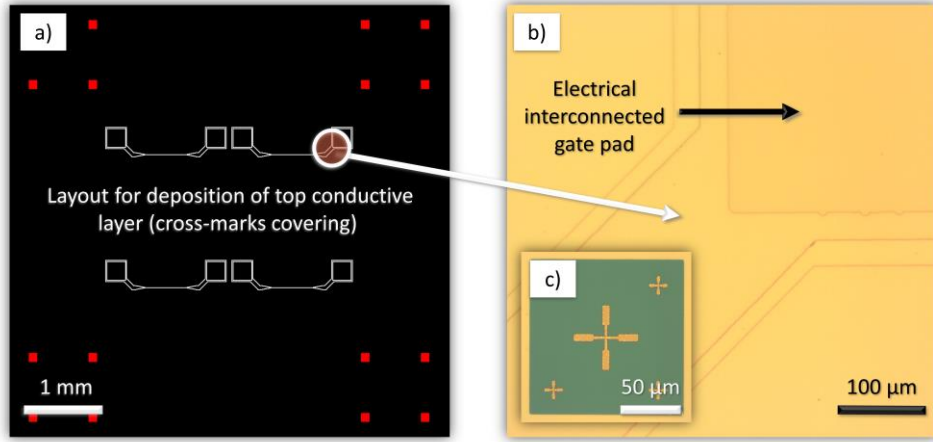
Figure 108. Illustration of Step 4 – deposition of Ti/Au conductive layer: a) one chip layout (red color – current lithography pattern), b) deposited Ti/Au layer over the entire wafer, c) detail of the masked cross-marks after lift-off process.

7. Etching of Au/Ti conductive layer – arrays of faced nanoelectrodes with proximity effect correction (1st e-beam lithography, 3rd etching)

For this fabrication step were used advanced design optimization tools Tracer and Beamer (described in 2.2.2), with which is possible to calibrate exposition parameters for a specific resist type or thickness by simulation. Except for various resists and its parameters, the optimization tools also calculate with all layers that lie under the resist and exposed area. The composition of materials has a major impact on lithography results, e.g., energy dissipation, resist undercut, shape (sharpness) and so forth. The example of the final output dataset for EBL system (Raith 150 II), containing calculated dose distribution levels over the faced nanoelectrodes pattern, is illustrated in Figure 109.
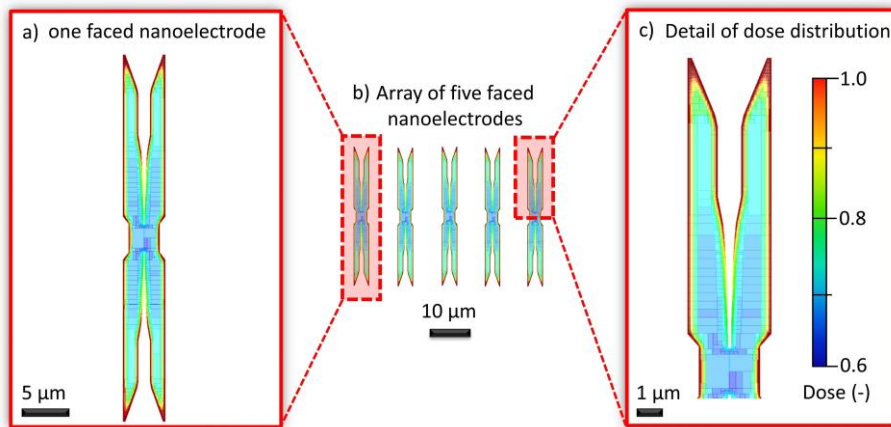
Figure 109. Illustration of proximity effect simulation: a) one faced nanoelectrode, b) array of five faced nanoelectrodes, c) detail of dose distribution with a dose scale bar.

The EBL process was carried out with the same parameters used for this process before, details were described in 4.1.1. Then, the etching of Au/Ti conductive layer was performed using IBE process parameters, which are listed in Table 6. To ensure the results of the etching process and the removal of the whole conductive layer down to the silicon dioxide, reactive-ion etching was used to etch the remaining Ti adhesion layer. This process is merely a precautionary procedure, in which the non-uniformity of ion-beam etching using accelerated

argon ions is compensated by additional chemical reaction of thin-film layer with reactive gas (i.e., SF_6) over the entire 4-inch substrate wafer. The SIMS endpoint detection was not appropriate to use due to the low area that was etched in this fabrication step. The parameters are listed in Table 15.

Table 15. Parameters of Ti adhesion layer etching using reactive-ion etching tool (NGP-80).

Reactive-ion etching – Oxford Plasma – NGP-80	
Parameter	Material
	Ti
DC Bias Voltage (V)	60
Forward/Reflected Power (W)	100/0
Strike pressure (mbar)	80
Etching pressure (mbar)	20
Ar flow (sccm)	20
SF_6 flow (sccm)	20
He backing flow (sccm)	10
Etching time (s)	15

Figure 110a depicts the design layout for e-beam lithography, in which four arrays of faced nanoelectrodes and the pattern for Van der Pauw measurement structure (temperature on-chip sensor Au220) are displayed in red color. After the IBE process, the resist removing procedure and cleaning process was carried out. Then, the structures were observed by optical and SEM microscopy, as shown in Figure 110b, c.
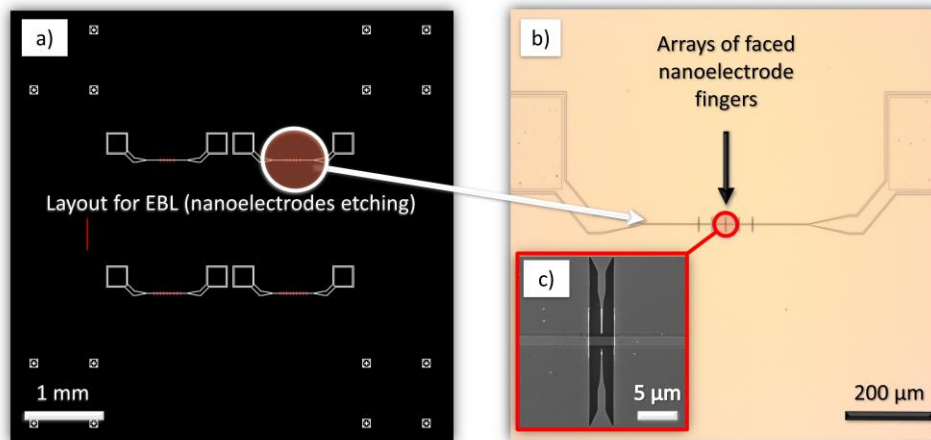
Figure 110. Illustration of Step 5 – etching of Ti/Au conductive layer (nanostructures): a) one chip layout (red color – current e-beam lithography pattern), b) gate electrode with arrays of faced nanoelectrode fingers after Ti/Au layer IBE process, c) detail of the nanoelectrode fingers (SEM inspection).

8. Etching of Au/Ti conductive layer (microstructures) – linking the remaining electrode system to the nanoelectrode arrays (5th photolithography, 4th etching)

The rest of the structures made of the Au/Ti conductive layer, for instance, pads, electrodes paths, and microelectrodes were performed in this fabrication step (see the design layout in Figure 111a). The negative tone resist (AR-N-4340) in combination with AR-BR (bottom resist) were used as the temporary mask for etching procedure, which is shown in Figure 111b. The critical operation of this fabrication step dealt mainly with the precise alignment of the pattern onto the previous EBL structures (arrays of faced nanoelectrodes

pattern), which were covered by the resist to protect them from etching, as depicted in Figure 111c.
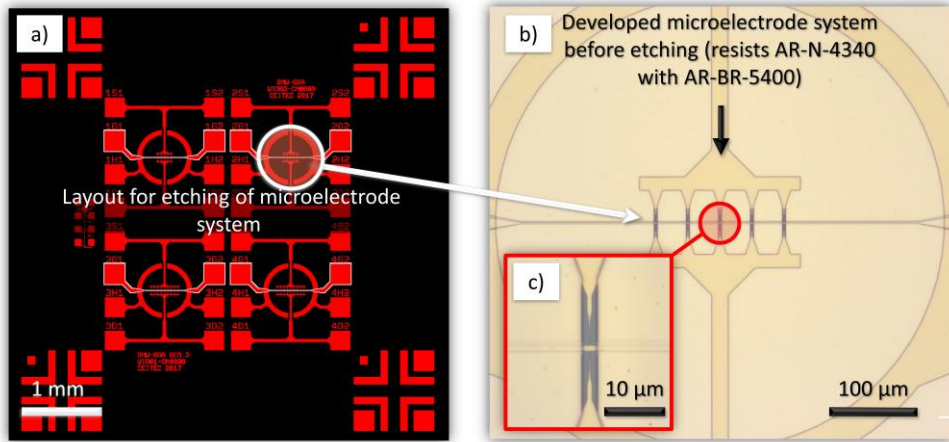
Figure 111. Illustration of Step 6 – etching of Ti/Au conductive layer (microstructures): a) one chip layout (red color – current lithography pattern), b) developed microelectrode system before IBE process, c) detail of the covered faced nanoelectrode by the double-stack resist.

The etching of Au/Ti conductive layer was performed using the same procedure as in the previous step. After the IBE, the wafer was deprived of the resist and thoroughly cleaned before the next step (wet cleaning and plasma cleaning process).

9. Deposition of SiO₂ dielectric layer – electric field shielding and opening windows process (4ᵗʰ deposition, 6ᵗʰ photolithography, 5ᵗʰ etching)

In the last fabrication step, the entire surface of the wafer was covered by 100 nm of silicon dioxide layer using ALD Fiji 200 system as in the fabrication Step 5. The deposition was realized using the same procedure (described in Table 14 for SiO_2) with the exception that a total of 1550 cycles were used instead of 1428 cycles. Thus, the wafer was coated with a positive tone resist (AR-P-3540), which served as a temporary mask with a design layout illustrated in Figure 112a. Subsequently, the uncovered areas (i.e., all pads, hydrophobic rings, and dielectric windows) were etched by RIE process ("opening windows" procedure, see in Figure 112b). For this process were used the same parameters as for the RIE process in fabrication Step 1.
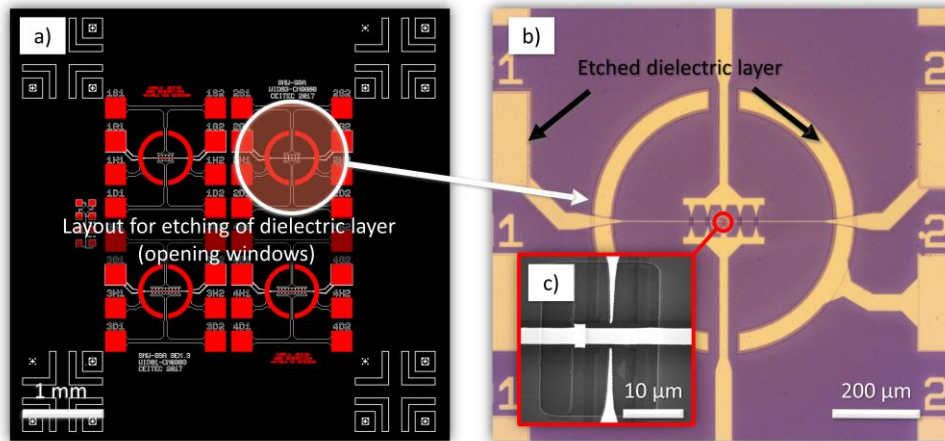
Figure 112. Illustration of Step 7 – deposition of SiO₂ dielectric layer and die (electric shielding and opening windows): a) one chip layout (red color – current lithography pattern), b) depicted areas with the etched dielectric layer, c) dielectric window (wide) uncovering the faced nanoelectrode (SEM inspection).

In contrast to Step 1, the resulting etched structures were electrically tested by the pad-to-pad resistance measurement using probe stations system Cascade Microtech MPS150 connected to parameter analyzer Keithley 4200 SCS. After the fabrication process, the wafer was covered with the positive tone resist (AR-P-3540) and cut into the chip pieces 5x5 mm using compact laser dicer (Oxford Lasers, A series).

5.1.3 Design and fabrication of a TO-8 gas chamber for low-current measurement

The gas chamber design was inspired by the UB chamber used for the gas testing of the second chip generation, during the internship at the University of Barcelona in Spain (shown in Figure 82). Despite there are many differences between both designs and their parts, the basic idea remains in using a chamber body similar to the materials used in vacuum technology (e.g., consisting of a flange, cap and clamp system) connected to the PCB (e.g., consisting of conductive paths, connectors or electronics) and forming one device.

The new design was focused to improve the chamber features, and this improves further the gas sensing tests. This, in order to eliminate as many undesirable effects as possible, for example, a low chamber degassing, or poor spreading of the gas flow in the chamber and many others. Due to the reduction of these effects, the characterization of the sensing element is more accurate and predictable, as the chips can be tested faster on the presence of one gas without the influence of other gasses remaining in the chamber (or other parts) from measurements before. In this context, a list of required features, which are mostly linked, is noted below:

- minimal chamber volume and dead volume,

- high gas exchange rate,

- chemically resistant materials,

- minimal adsorption surface,

- excellent electrical parameters and minimal signal noise.

Design and specification of the new TO-8 gas chamber

The body of the chamber solution is made of industry-standard connections and fittings from 316L grade stainless steel (SS). The inside organization consists two parts (top and bottom) that are solved based on Ketron® PEEK material providing required chemical and temperature resistance (up to 250 °C, continuously), and in combination with auxiliary sealings from polyfluorinated rubber (Viton®, o-rings) also the sealing capability. All parts of the chamber are shown in Figure 113.

The bottom part, which is illustrated in Figure 113b, is designed to carry 12 leads of TO-8 package equipped with two additional auxiliary contacts on each side for user custom application. The electrical and mechanical connection between the bottom part (TO-8 package) and PCB is carried out through standoff self-sealing press-fitted contacts (gold coated), which are soldered to the PCB. Also, the bottom part contains the exhaust situated directly underneath the TO-8 package to ensure the flow around the package surface. Further, the design counts with a humidity and temperatures sensor that are situated in the same exhaust cavity.

The top part was designed in three variations, where the basic version provides only the dead volume limitation, the second variant is equipped by UV LEDs for photoinduced reaction studies, as it is shown in Figure 113a. Thus, the most sophisticated variant is extended by the viewport, which is realized by axial channel and dual o-ring sealed window. Therefore, this modification might also be extended for the remote IR temperature sensor providing direct studied sensor element temperature readout.

At last, the outside world connection is provided by coaxial connectors (SMA type) mounted directly on PCB. The PCB is designed as a four-layer system with one signal, two ground planes and one shield plane; which works as the mechanical support for the chamber assembly and mound for chamber itself (see Figure 113c, d).
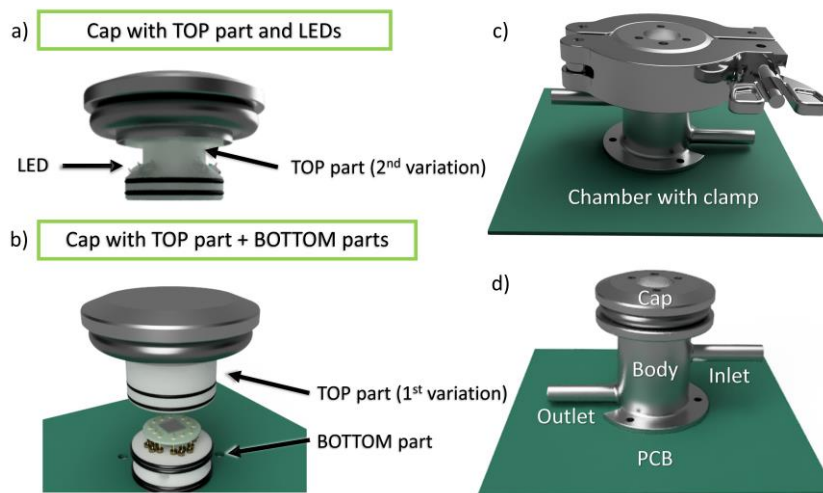
Figure 113. Illustration of the design of TO-8 gas chamber for low-current measurement: a) cap with TOP parts and LED system, b) cap with top and bottom parts, c) chamber with clamp, d) external organization without a clamp.

5.2 Results and discussion

In this section, the results of the fabrication process of the third chip generation with advanced nanoelectrode array provided of a third electrode are presented together with the method by which the single NW connection in the parallel array can be achieved. The effect of the gate potential on the gas sensing response was characterized by using the new TO-8 gas chamber system.

5.2.1 Advanced nanoelectrode arrays on 4-inch wafers and optimization of the structural parameters for single NW interconnection

In general, due to the chosen fabrication techniques, including through-mask lithography, or dry etching on 4-inch wafers, it was necessary to use several wafers for the optimization of the procedure parameters. For instance, the coating and development process (resists processing) optimization and its follow up operations, such as DESCUM, depositions, IBE, or RIE, were performed with more than ten wafers. However, the final fabrication process, after the fabrication testing procedures, were carried out on three wafers, particularly, because of the ALD process, which is limited by the size of the carrier (8-inches). Each of the three wafers comprised the same basics structures (described in 5.1.1) with only a few minor modifications, which are described further below.

On a wafer level, every 4-inch wafer consists of 212 chips in total (see Figure 114c), which are not placed in the center and close to the edge, as opposed to the previous second generation. It is mainly due to the homogeneity of resulting layers through the wafer surface and to ensure a space for precise marking of technological steps. Accordingly, instead of the chips, there were placed aligning marks (for the mask-aligner) and an individual fabrication step labels, which are shown in Figure 114a, b. For each fabrication step was developed a unique alignment mark including resolution bars, which were designed considering a follow-up process, such its resist type, layer material (e.g., Au, SiO_2), and so forth. Furthermore, the alignment mark contains two shape types; the first is for a coarse alignment processes (squares), where the resolution of the alignment might be above 2 μm, and second, in which the resolution is under 2 μm or lower (cross-lines), e.g., Step 6 – linking the remaining electrode system on the EBL electrodes. These cross-lines are visible in Figure 114b in the center of the alignment mark.
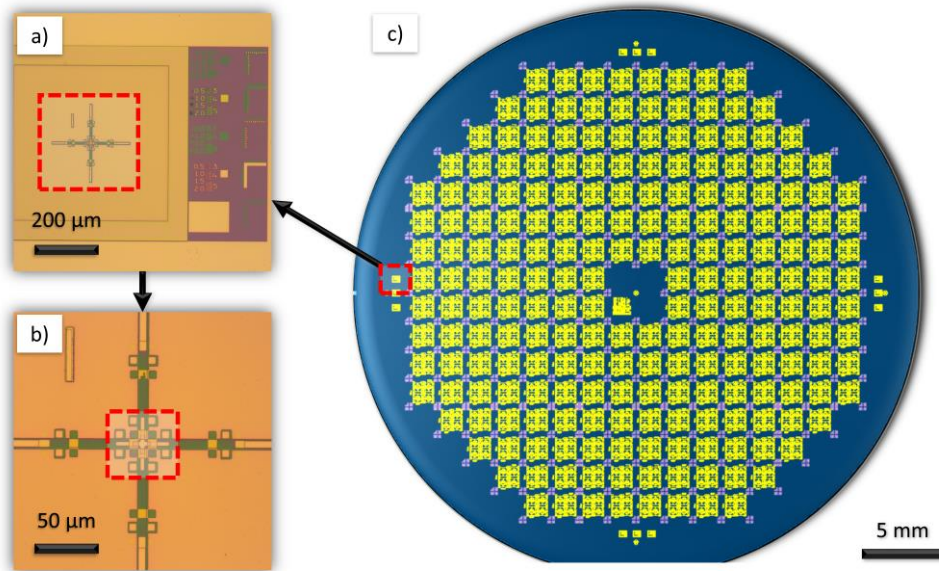
Figure 114. Illustration of the 4-inch wafer with structures of the third chip generation: a) alignment marks with resolution bars developed for the mask-aligner MA8, b) detailed view focused only on structures for the alignment procedure, c) 4-inch wafer after all procedures.

Thus, the final third chip generation consisting of four resistive nanoelectrode arrays with a buried gate electrode to enhance gas sensing is presented in Figure 115. Figure 115a illustrates the whole chip, whereas Figure 115b shows a closer view of the microelectrode array containing five electrodes and Figure 115c displays the detailed view of the nanoelectrode fingers with the buried gate electrode.
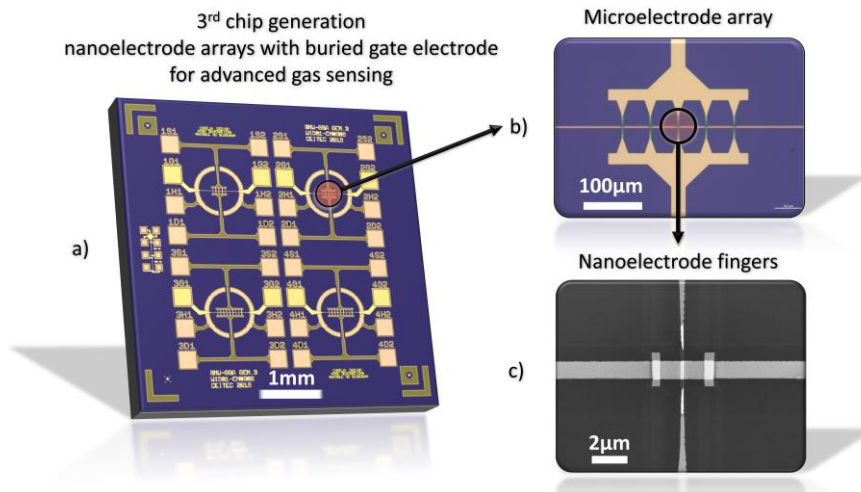
Figure 115. Illustration of the third chip generation: a) entire chip, b) microelectrode array with 5 electrodes – optical inspection, c) nanoelectrode fingers with gate electrode – SEM inspection.

As was stated above, the chip design was optimized during the fabrication process that was caused, mainly, due to the adjustment of the lithographic process parameters, such as the set bias tolerance of the follow-up lithography that comes from the design specification. To be concrete in such adjustment, an example of the optimization procedure is shown in Figure 116a. This figure shows the state of the faced nanoelectrode after the Step 6, in which the Ti/Au conductive layer was etched via double-stack resist (AR-BR) by using IBE, but obviously the pattern that covers the previous EBL pattern was a bit thicker. As a result, thin sidelines of

Ti/Au layer were not etched properly. This caused a shorted nanoelectrodes and the gate electrode was disturbed and broken in several places.
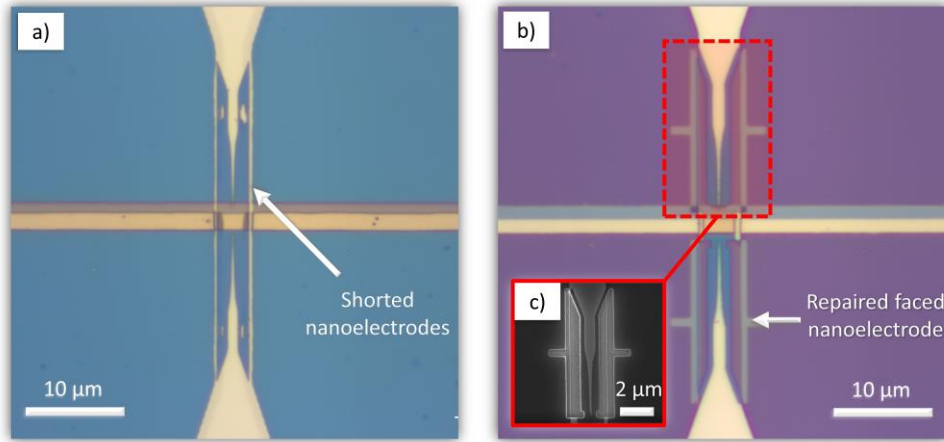
Figure 116. Optical inspection of the faced nanoelectrodes: a) shorted nanoelectrodes with sidelines and disturbed gate, b) faced nanoelectrodes after repairing procedure (IBE) on another wafer, c) SEM mapping of the repairing pattern in e-beam resist (CSAR) for one nanoelectrode before IBE.

Consequently, the shorted parts of the nanoelectrodes were repaired by using another EBL and IBE process, in which the EBL pattern (shown in Figure 116c) covers the nanoelectrodes and uncovers the thin sidelines to be etched during IBE process. The result of the repairing process is depicted in Figure 116b, where it is visible that all remaining Ti/Au sidelines were removed as compared to Figure 116a.

Generally, most attention was paid to the optimization of the single NW interconnection. As was stated before, the number of an aligned NWs on the faced nanoelectrodes in the array may be influenced by several factors, for instance, the geometry of the electrodes compared to the NWs geometry, DEP parameters, NW drop parameters (number of NWs and volume) and many others. [141,142] In the second chip generation, the effort was focused, basically, to the electrode width, which partly helped to get a single NW interconnection in one array. However, the process of the single NW alignment and its repeatability was still not optimized enough.

For this reason, two modifications of a dielectric (shielding) windows were made in order to find the differences between the NW alignment procedure with a wide dielectric window (about 10 μm thick and 20 μm long) and narrow dielectric window with dimensions comparable to a size of a NW (from 200 and 300 nm thick) and 10 μm long. In other words, if it is possible to achieve more accurate single NW alignment with a structure containing a combination of as-mentioned faced nanoelectrodes and narrow dielectric windows with dimensions of NW, which together can be used as a tool for precise DEP alignment.

These two modifications were evaluated by AFM tool (Bruker Dimension Icon), and the results of the fabrication are illustrated in Figure 117. Furthermore, the use of this technique was especially important in determining whether there is any remaining silicon dioxide on the nanoelectrodes. For this purpose, the AFM was used in a phase imaging mode that is capable of recognizing a different material composition based on its different phase shift. [202]
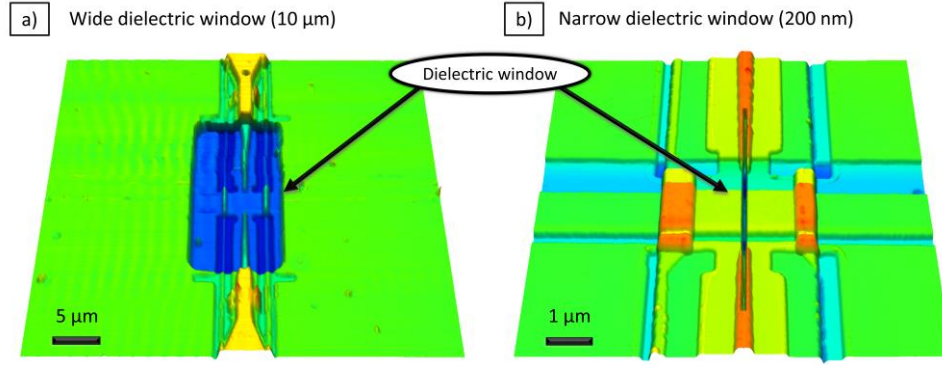
Figure 117. AFM inspection of dielectric windows with various width: a) wide dielectric window (10 μm), b) narrow dielectric window (200 nm).

As was stated in the fabrication part, wide windows were carried out by optical lithography during Step 7 of the fabrication process. In Figure 118 is depicted the fabrication process of the narrow windows, which, as opposed to the fabrication of the wide windows, were created by another e-beam lithography. Thus, the dielectric window in the SiO_2 layer after the RIE process is shown in Figure 118b. Unlike the wide window, the narrow window is situated only in the area of faced nanoelectrodes that goes in a thin channel over the gate electrode, as illustrated in a closer view in Figure 118c.
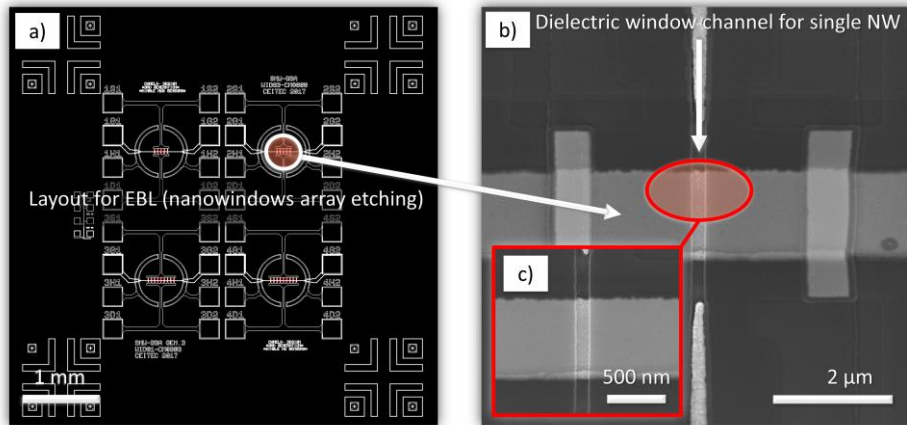
Figure 118. Illustration of additional fabrication step of SiO_2 dielectric window channel for single NW alignment enhancement: a) one chip layout (red color – current lithography pattern), b) distant view of the narrow dielectric window, c) closer view of the narrow dielectric window in the area of the gate electrode.

After the fabrication, the NW integration process, including standard developed procedures for NWs removal and coating, were performed for several chips for both modifications using probe station with the DEP parameters that were adjusted for the second chip generation previously. The result of the NW integration process by using DEP is presented in Figure 119, in which two modifications are compared by SEM figures with the same display parameters. The difference between these two modifications, in terms of alignment ability, is visible on a first look. Whereas the wide dielectric window (see Figure 119a) comprises bunches of multiple randomly interconnected NWs all over the window, the narrow dielectric window (see Figure 119b), on contrary, is loaded only with one NW that is exactly filling the space of the window starting from one electrode side, continuing over the gate electrode, and ending on the other side of the nanoelectrode pair, as it is shown in a close view in Figure 119c.
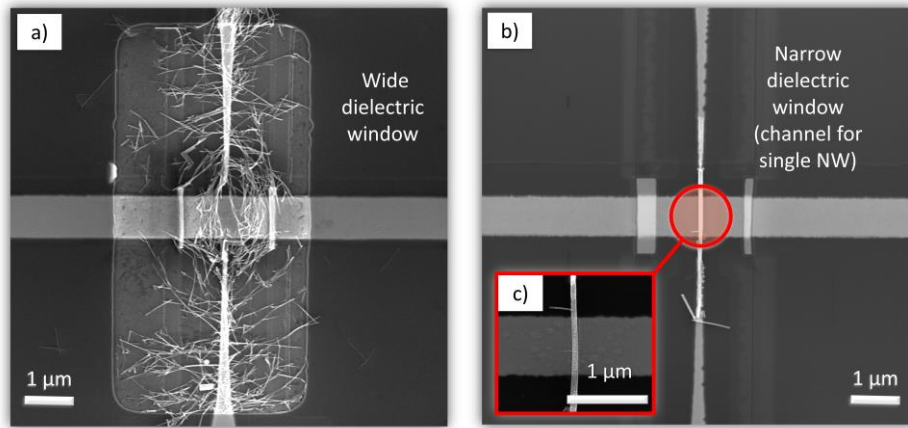
Figure 119. SEM inspection of two dielectric windows modification after DEP process: a) wide dielectric window with multiple interconnected NWs, b) narrow dielectric window with single NW interconnection, c) detail of single NW aligned within the window channel.

Overall, DEP tests on many chips proved that the probability of getting the single NW interconnections within one array increased significantly with using the narrow dielectric window structures, as opposed to the wide windows, in which it is a higher probability to obtain multi NW interconnections. These results show clearly the dependence of the obtained interconnection type (i.e., single-NW, or multiple-NW) on the dielectric window width, which was not clearly observed in previous chip generation as it was tested only one window width (four times narrower than present wide windows). In conclusion, the results showed the feasibility to interconnect a single NW based on a combination of DEP alignment procedure and limitation of the free space for aligning using dielectric layer frames.

In this context, Figure 120a depicts a 3D image that was taken to have a closer side view of an aligned NW in the dielectric window trench. The mapping of the surface morphology was performed on 15x15 μm area by AFM. In contrast with the top view that is done by SEM (see in Figure 120b), the 3D image shows that the NW is flexibly copying the surface of the etched dielectric window, as it is shown in Figure 120a and its detailed view.
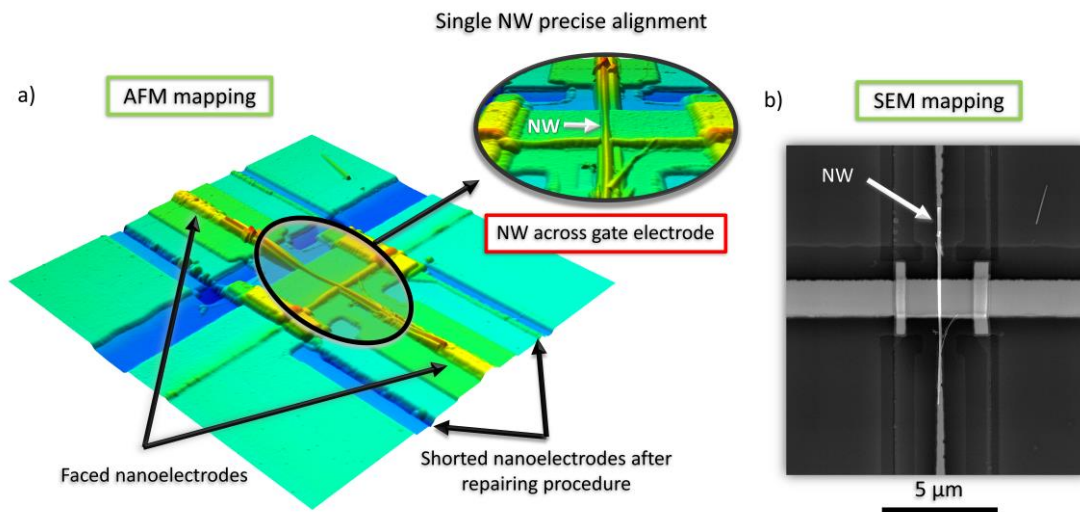
Figure 120. Detailed mapping of single NW aligned within the narrow dielectric window across gate electrode: a) 3D image showing a surface morphology of 15x15 μm area (AFM inspection), b) the same area depicted by SEM.

The results also show that the gate electrode is shifted more than 0.75 μm, causing a hill in the area of nanoelectrode end. This shift was due to an inaccurate mask alignment procedure during Step 2, which then affected another fabrication step, such as Ti/Au deposition or follow-up lithography and its alignment accuracy. Consequently, the alignment (local) marks for EBL were placed with a shift due to the wrong alignment in Step 2 that reflects on other structures such as mentioned shorted nanoelectrodes (see in Figure 120a on the right). On the contrary, the left side (see in Figure 120a, dark blue color) contain trench that was made in Step 6, in which the mask pattern was aligned to the wafer (global) marks of the first fabrication step (Step 1).

5.2.2 Gas sensing tests using three electrodes (FET) arrangement

The assembly of the sensing elements was performed using a modified procedure compared to previously assembled sensors in second chip generation. The modification consists in assembling whole sensor before the NW integration, so the alignment process (DEP) is implemented without the probe station, as described in 3.1.4. Instead, the TO-8 package, consisting of an electrically connected heater and chip, the structure is interconnected through pins via a PCB, which is subsequently connected to the waveform generator. Then, a precise alignment of a needle with a syringe containing NWs was performed by two cameras (*X, Y, Z*-axis), with which is possible to control the placement of a droplet on the chip, as shown in Figure 121a. This assembly process optimization was also reflected in the NWs integration process, including deposition via drop coating, and DEP process, which led to shorten the processing time and prevent the early drop evaporation. The result of the integration process is depicted in Figure 121b, in which two single NWs are shown aligned in a parallel array.
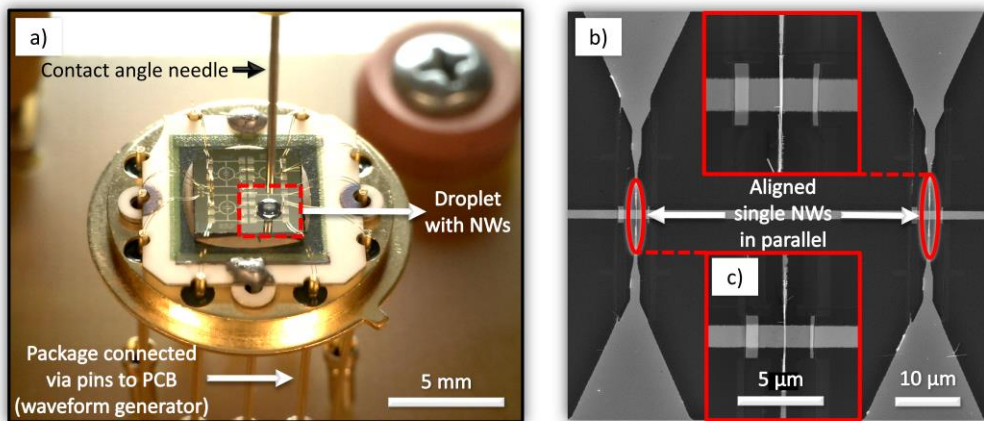
Figure 121. Illustration of the last step of the modified assembling procedure of a single NW gas sensor array using third chip generation: a) during the NWs integration process, b) aligned single NWs in parallel after the integration process (gas sensor ready for testing), c) detailed view.

The alignment procedure was carried out with various types of NWs, for instance, with cerium oxide-tungsten oxide core-shell NWs (Ce-WO_3) that are described in [203], but also with tungsten oxide NWs functionalized with Pt NPs that were used in the previous generation. However, pristine WO_3 were chosen for the tests to place apart the influence of catalytically active NPs and thus concentrate on the effects of applied voltage on the third electrode. In

general, the rate of success for the NW integration into the third chip generation was approximately 50 %, which is higher than in the previous chip generation. Therefore, several sensors were prepared for the gas tests, particularly, for tuning the parameters of the new tests.

The new fabricated gas chamber for TO-8 packages and low-current measurement and its parts are described in Figure 122. The TO-8 gas chamber is connected via pipeline to a gas station system, which was described in [104] in the details. Briefly, the gas station system is equipped by mass-flow controllers that are responsible for the precise gas flow adjustment. Thus, the parameters of the measurement, for instance, settings of the measurement procedure and its electrical and gas flow parameters, were controlled by PC software created in LabVIEW (National Instruments®). In this context, the program communicates with all external devices that are used for the measurement. Namely, it is SMU (Keithley 2450) for the measurement of the resistance (I_D), SMU (Keithley 2401) for gate voltage settings (V_{GS}), sensor heater control (Agilent 3633A) with a feedback from on-chip temperature sensor (Au220) measured by multimeter (Agilent 34410A), or power supply (Agilent U3606A) used for the chamber heating (DEGAS system). Additionally, the on-chip temperature sensing structure (Au220) was calibrated by the dependence of resistance on temperature, where the temperature on the chip was measured by two independent methods, i.e., using infrared thermometer and temperature sensor Pt100.

All these devices were interconnected via reduction PCB's, which were fabricated in order to make a connection with I/O of the chamber through SMA connectors.
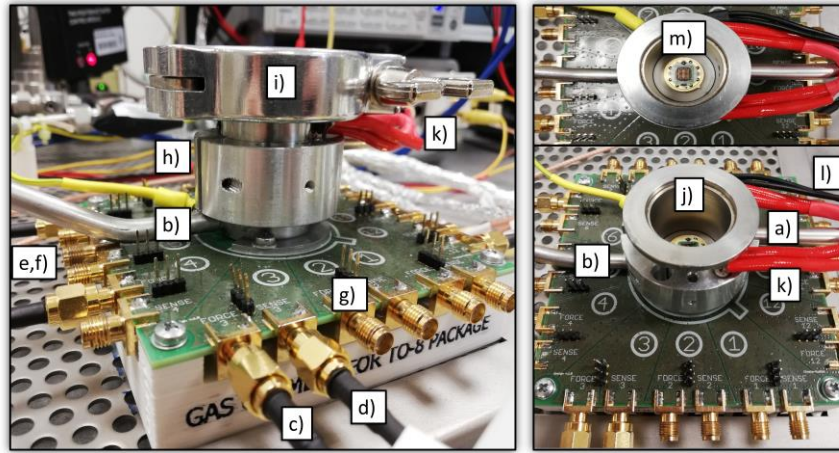
Figure 122. Description of the developed gas chamber and its parts (BUT chamber): a) gas inlet, b) gas outlet, c) sensor (Force+), d) sensor (Sense+), e) sensor (Force-), f) sensor (Sense-), g) heater +, h) heater -, i) chamber cap, j) chamber body, k) DEGAS heater, l) temperature sensor (PT 100), m) measured sensor.

The chamber underwent several production tests, particularly, the mechanical parts, including gas leakage test, degassing procedure, signal or gas flow interference test, resulting in a few design modifications mainly in the top part, adjusting the gas flow distribution respectively. After that, the chamber was prepared for a standard gas measurement procedure.

Effect of gate voltage potential on measured sensor resistance during gas exposure

The effect of applied voltage potential on the buried gate electrode, situated under the NWs channel, was tested to nitrogen dioxide (NO_2, oxidizing gas) and hydrogen (H_2, reducing gas). The response of the sensing elements was carried out by monitoring the electrical resistance changes of the NWs while applying different currents, the gate voltage (positive, negative), and various temperatures (from RT to 250 °C). The tests were performed using the same procedure employed for the second generation, i.e., findings the optimal current, temperature to reach satisfactory gas response and the concentrations measured.

Results proved a stable behavior (i.e., no resistance baseline changes due to the testing cycles). A general gas procedure was employed to show the effect of applied gate voltage on the sensor response in long term measurement (shown in Figure 123), in which one gas cycle at one gate voltage (started from 0 V) included stabilization, response, and recovery time that were equally long (30 minutes). This gas cycle was repeated alternately for two negative voltages (V_{GS} = -5 and -10 V), and two positive voltages (V_{GS} = 5 and 10 V) for one fixed temperature and current (I_D). To ensure visible resistance changes, the applied concentrations were intentionally high for both gases, i.e., 1000 ppm for hydrogen, 5 ppm for nitrogen dioxide, respectively. For instance, Figure 123a represents measured sensor resistance at 150 °C, as opposed to Figure 123b, in which the resistance is measured at 200 °C. The sensing parameters, such as response and recovery time of the sensor with applied current (I_D = 5 nA), occur at 200 °C rather than at 150 °C, which is consistent with our previous observations for tungsten oxide NWs. [204]
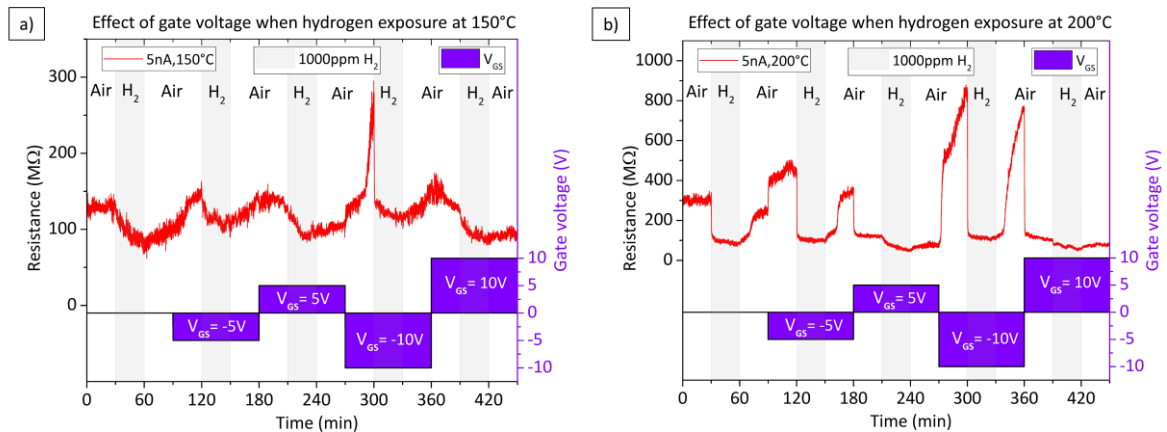
Figure 123. Effect of gate voltage sweeping on WO$_3$ gas sensor resistance (I_D = 5 nA, H_2 = 1000 ppm) during hydrogen exposure at various temperatures: a) T = 150 °C, b) T = 200 °C.

Results in Figure 123 show that the negative voltage potential (-V_{GS}) applied on the gate electrode increases the resistance of the sensor in air. On the contrary, the positive voltage (+V_{GS}) decreases the resistance when air is present. According to the interaction of gases at the solids (n-type MOX case), described in 1.2.3 and in [205], the adsorption of the oxygen molecules (in air) causes a reduction of the free charge carriers concentration and the formation of a potential barrier (depletion layer), in other words, the surface is highly depleted of electrons

(carriers) and the electrical resistance in the channel increases. After the exposure of the surface to a reducing gas (hydrogen), the electrical resistance and depletion layer thickness decrease, due to oxygen removal accompanied by reinjecting electrons into the conducting band. This process is opposite for oxidizing gases (adsorption of more oxygen) so that after the exposure of the surface to an oxidizing gas the depletion layer and the resistance increase.

Thus, the conductivity of the sensing element, and in turn the sensitivity, depends on the depletion layer thickness, which is in the order of tens nm (very thin). However, in gas sensing systems with an additional (third) electrode, the depletion layer and charge carrier density of the NWs channel is also modulated by the applied voltage potential on the gate (third electrode), so depletion and accumulation of electrons at the semiconductor can be modulated by the gate. For instance, in Figure 123b, the baseline resistance is increased as a result of the applied negative gate bias voltage (visible in both $V_{GS} = -5$ and -10 V), which indicates withdrawing of the electrons from conduction band along with a depletion layer extension compared to the the regime in which $V_{GS} = 0$ V. Consequently, during hydrogen exposure, adsorbed oxygen is removed by hydrogen molecules and numbers of free charge carriers are generated (i.e., the channel conductivity increased). Thus, the recorded resistance change was about one third higher for $V_{GS} = -5$ V, and three times higher for $V_{GS} = -10$ V, than for $V_{GS} = 0$ V. When the gas is removed, the surface is again depleted of carriers as the oxygen is again adsorbed on the surface. On the contrary, the positive voltage potential on the gate opens the NWs channel, due to the shrinking of the depletion layer and reinjection of electrons at the surface, which, in turn, leads to a low baseline resistance and low resistance changes when exposed to the reducing gas (see in Figure 124).

This phenomenon is also reproduced for oxidizing gas (nitrogen dioxide). Figure 124 shows a comparison of recorded sensor resistance under both reducing and oxidizing gases exposure at 200 °C with gate voltage sweeping, as described above. As seen in Figure 124b, the NWs channel is fully accumulated of electrons by the positive gate voltage, that almost no resistance change is visible, as opposed to the negative voltage, with which the change is noticeable. However, in contrast to the magnitude of the change in resistance upon applying the negative voltage under hydrogen exposure (see in Figure 124a), the resistance change, when using nitrogen dioxide and negative voltage ($V_{GS} = -5$ V), is lower than for $V_{GS} = 0$ V. On the other hand, the recovering is faster but the response does not reach the maximum value, as for $V_{GS} = 0$ V.
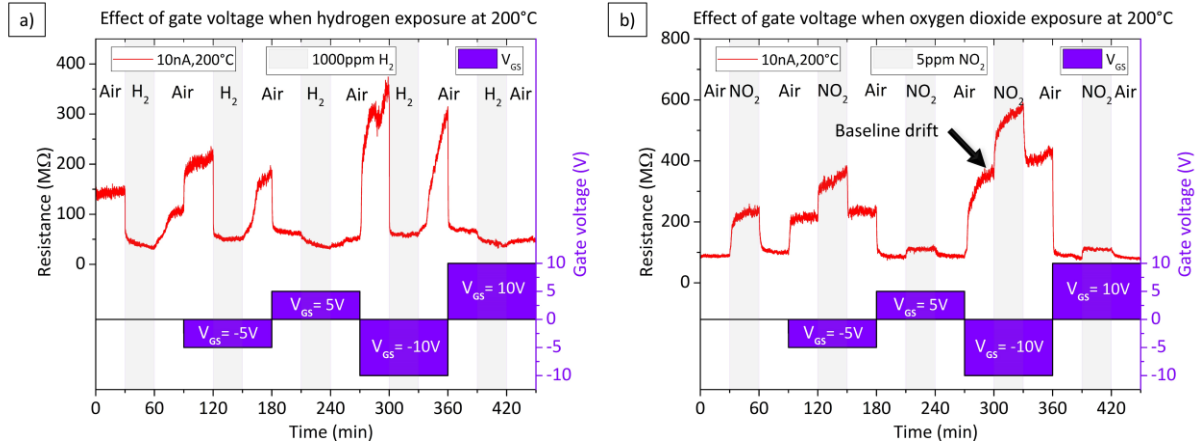
Figure 124. Effect of gate voltage sweeping on WO₃ gas sensor resistance (I_D = 10 nA, T = 200 °C) during exposure to various analytes: a) H₂ = 1000 ppm, b) NO₂ = 5 ppm.

Another phenomena, which appeared during the gas measurement, is baseline drift (marked in Figure 124b). This drift is more visible for negative voltage (e.g., V_{GS} = -10 V), although a slight drift can also be observed at a positive voltage (e.g., V_{GS} = 10 V). As stated in the fabrication section, the gate electrode is electrically insulated from the surface of NWs via dielectric double-layer (HfO_2/SiO_2), which creates a parallel capacitance (C_{OX}). Therefore, with increasing voltage (V_{GS}) applied to the gate electrode occur parasitic effects such as bias-stress induce contact (channel degradation), or charge trapping, resulting in resistance drift, as described in [205,206]. With time, the resistance reaches the steady-state; however, as higher is the gate voltage as longer is the relaxation time; in other words, the time to stabilize the sensor resistance. The charging effect can have origin in dielectric layer thickness, and/or the material composition of the layer.

Further measurements of these samples showed (see in Figure 125 and Figure 126) that the baseline drift can be reduced by increasing the sensing current (I_D), which is in line with the literature [205]. Figure 125a shows the gas measurement with applied sensing current I_D = 5 nA and compared to Figure 125b, in which the sensing current is four times higher (I_D = 20 nA), it is noticed that the drift is already visible at V_{GS} = -5 V. For instance, the resistance drift at negative gate voltage (V_{GS} = -5 V) and current (I_D = 20 nA) is not noticeable, as appose to the that using lower current (I_D = 5 nA), and the recovery time of the sensor is almost comparable with response time. Also, the slope of the recovering part of the curve is lower for negative gate voltage (V_{GS} = -10 V), as the relaxation time to get to the steady-state is faster.
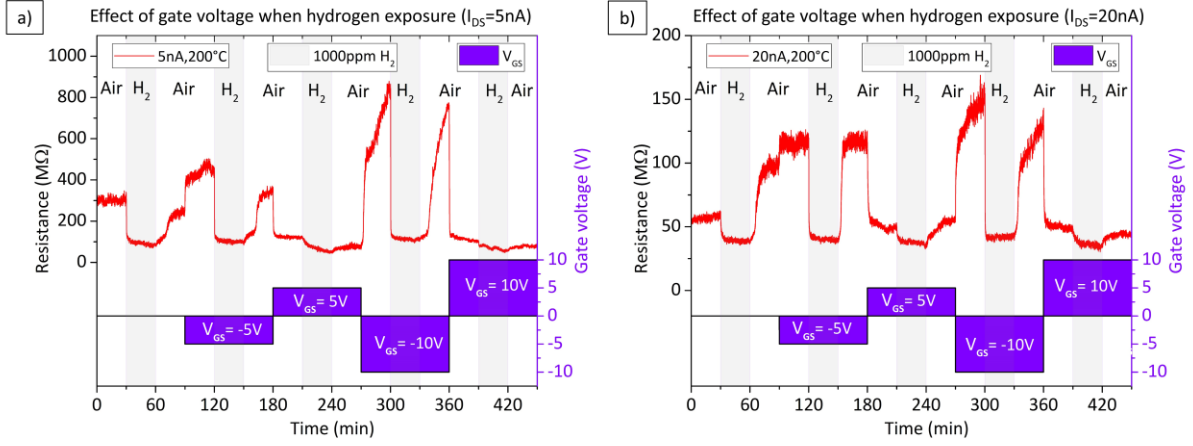
Figure 125. Effect of gate voltage sweeping on WO₃ gas sensor resistance (H$_2$ = 1000 ppm, Temp. = 200 °C) during hydrogen exposure with different applied currents: a) I$_D$ = 5 nA, b) I$_D$ = 20 nA.

Therefore the increase of the applied sensing current could play a role in the following aspects. First, the drift effect can be reduced, but the higher current is applied, the more negligible is the gate voltage effect, in relation to the desired increase of the sensor reactivity in the presence of the analyte. Second, the increase of sensing current in combination with negative gate voltage can be used to recover the sensor at lower temperatures. Figure 126 shows the sensor recovering effect at 150 °C when two different currents (I$_D$) are applied. The measurements proved that the sensor recovering is more effective by using higher current (I$_D$ = 40 nA) as shown in Figure 126b, in which the recovering effect appeared already at V$_{GS}$ = -5 V. Also, both response and recovery time were faster than in case of lower current (I$_D$ = 5 nA), see in Figure 126a.
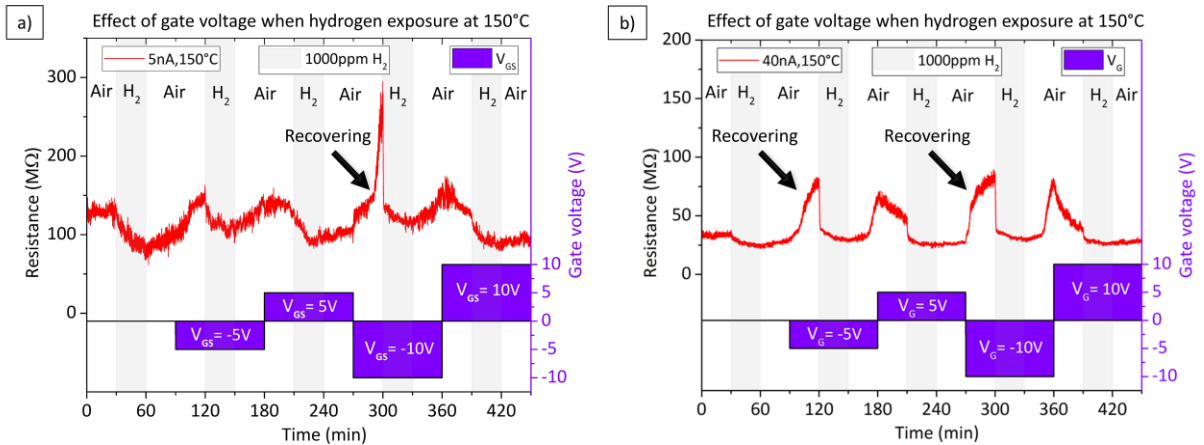
Figure 126. Combined recovering effect of different applied currents and negative gate voltages at a lower temperature (150 °C): a) I$_D$ = 5 nA, b) I$_D$ = 40 nA.

Summary of gas sensor response – the influence of gate voltage biasing

Similarly to the second chip generation, the sensor response based on third chip generation was defined as (R$_{air}$-R$_{gas}$/R$_{gas}$) for hydrogen (reducing gas) and (R$_{gas}$-R$_{air}$/R$_{air}$) for nitrogen dioxide (oxidizing gas), where R$_{air}$ is the sensor resistance in air at the stationary state and R$_{gas}$ the sensor resistance after a defined time of analyte exposure. Figure 127 shows the effect of gate voltage sweeping on the sensor response with various applied sensing currents (5,

10, 20, and 40 nA) toward 1000 ppm of hydrogen (Figure 127a), and 5 ppm of nitrogen dioxide (Figure 127b) both mixed with synthetic air, using three single aligned pristine WO$_3$ NWs in array as sensing elements.
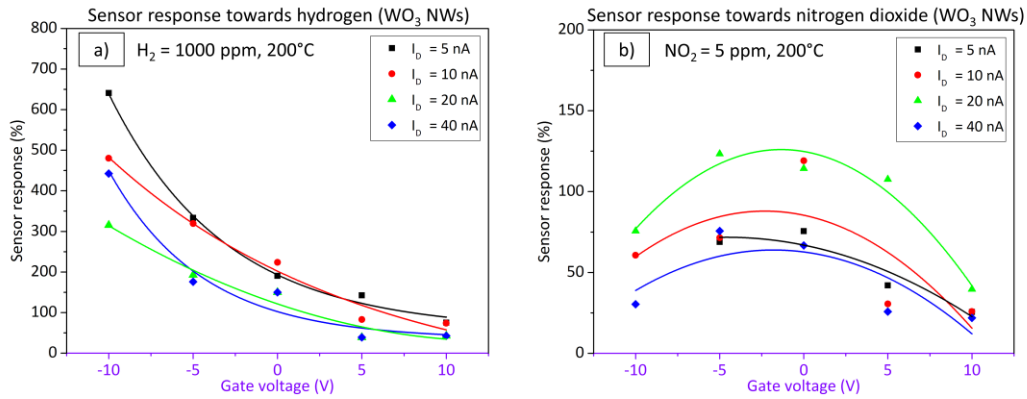
Figure 127. Sensor response vs. gate bias voltage of the gas sensor based on single WO$_3$ NWs toward various analytes at 200 °C: a) H$_2$ = 1000 ppm (reducing gas), b) NO$_2$ = 5 ppm (oxidizing gas).

As discussed above, the results show a generally better response to hydrogen than nitrogen dioxide. Thus, the discussion is focused particularly on hydrogen results. For instance, the sensor response registered the highest value of approximately 650 % for applied current I_D = 5nA and gate voltage V_{GS} = -10 V, as opposed to the four times higher current I_D = 20nA which showed a response of approximately 325 % for the same negative gate bias voltage (see in Figure 127a). On the contrary, the sensor response values using positive gate voltage (V_{GS} = 10V) varies between 50 and 100 % for all currents. Results also show that the sensor responses for zero gate voltage (V_{GS} = 0 V) register lower values for higher currents I_D = 20 and 40 nA (150 % approx.), and higher values for lower currents I_D = 5 and 10 nA (around 200 % approx.). These results are in line with the results observed above, in which the sensor response was enhanced to hydrogen molecules when applying lower sensing current and higher negative gate voltage (I_D ≤ 10 nA and V_{GS} ≤ -5 V) than without the gate bias.

In contrast to hydrogen, the results for nitrogen dioxide molecules (oxidizing gas) are different (see in Figure 127b). For nitrogen dioxide, the influence of the gate biasing on the sensor response was minimal and only in certain circumstances. For example, the enhancing effect on the response occurred at V_{GS} = -5 V, but only for higher currents I_D = 20 and 40 nA. Moreover, the difference between sensor response at V_{GS} = -5 V and that at V_{GS} = 0 V was approximately 10 %. Also, the highest registered response was 125 % (I_D = 20 nA, V_{GS} = -5 V), and the lowest registered sensor response was approximately 20 % with applied positive gate voltage and the highest current (I_D = 40 nA, V_{GS} = 10 V).

To sum up, these results show the enhancement of the sensor response to hydrogen molecules using negative gate voltage (V_{GS} ≤ -5 V) while the response to nitrogen dioxide is suppressed for the same conditions. Therefore, the results prove that the gate voltage biasing of the NWs channel parameters works better for hydrogen (reducing gas) than for nitrogen (oxidizing gas). The positive gate voltage (V_{GS} = 10 V) lower the response more than two times, compared to that with the negative voltage (V_{GS} = -10 V), which enlarge the response more

than three times. Except for the nitrogen dioxide, as stated, in which the gas response decreased, but not as significant as the increasing effect in case of hydrogen.

5.3 Summary

This chapter presented the fabrication steps and implantation of the third chip generation, which includes new concepts and the improvements determined in the two previous generations. All the experience that was gradually acquired during the thesis is reflected in the development of such an optimized platform, which showed enhanced gas sensing in FET arrangement. The third chip generation was designed to be used together with developed heating system on the TO-8 package as a highly sensitive and possible selective gas sensing elements. The characterization of these chips was performed in the newly developed gas chamber for low current measurement.

In sum, the third chip generation was designed with the same chip size as second (5x5 mm), consisting of two pairs of nanoelectrode arrays with 5 and 9 faced nanoelectrodes, which divide the chip area into the four parts. Each pair has two modifications with different end width of the nanoelectrode fingers (200 nm and 300 nm). Each array consists of four doubled pads belonging to four electrodes (D, S, G, and H) with the size 300x300 μm. These pads were situated on the sides of the nanoelectrode array in the center, which is surrounded by hydrophobic structures with round shape. Additionally, the aligning electrodes D and S can also be used as measuring electrodes for applying the sensing current (I_d). The gate electrode (G) under the hydrophobic ring, and through the gap between the faced electrodes, has a size of 3.5 μm. Another important structure included in this chip is, for example, the Van der Pauw measuring structure, which was originally intended for sheet resistance measurement of the gold layer during the fabrication process, but eventually, it was also used as an on-chip temperature sensor (Au220). Other significant structures included in this chip generation are the narrow windows for single NWs alignment, which was performed by etching of the top dielectric SiO_2 layer.

Thus, the third chip generation was carried out using throughout fabrication techniques, which required advanced fabrication process with higher reliability to implement multi-step nanofabrication using 4-inch wafer technology. In this context, a total of seventeen general fabrication processes were performed, including two e-beam lithography, six optical lithographies, four depositions, and five etchings. This number does not involve additional fabrication procedures, such as cleaning, mask design development, or repair processes. Several structures, mainly used for multi-step lithography process, were developed, for example, alignment marks for through-mask lithography, which consists of resolution bars that consider the follow-up processes. Also, unique chip ID, including chip numbers and wafer number (WID) were part of the wafer. In addition, one 4-inch silicon wafer consisting of 212 chips with four resistive nanoelectrode arrays with the buried gate electrode, narrow dielectric windows with dimensions comparable to a size of the NW. To be specific, these windows, which were

made in SiO_2 dielectric top layer, are 200 and 300 nm thick and 10 μm long. Consequently, the nanoelectrode array platform enabled the selective assembling of various types of NWs with a success rate of approximately 50 %.

This chapter also included the gas test chamber developed for the characterization of the gas sensing elements in FET arrangement. Briefly, the top part of the chamber was designed in three variations, including basic version provides only the dead volume limitation, variant equipped with UV LEDs for future photoinduced sensing tests or the variation with an extended viewport for remote temperature sensing. The gas chamber passed standard initial laboratory gas tests to prevent leaks and optimize the electrical parameters. The gas sensing characterization (for chips with three single pristine non-functionalized WO_3 NWs aligned in a parallel array) consists of exposing these structures to NO_2 (oxidizing gas), and H_2 (reducing gas). The response of these samples was determined by monitoring the electrical resistance changes of the NWs while applying different currents, gate voltages (positive, negative), and various temperatures (from RT to 250 °C controlled directly on-chip using Au220).

At last, the results from the third chip generation proved that the gate voltage biasing of the NWs channel parameters increases significantly the response to reducing gas (H_2) compared to oxidizing gas (NO_2). Also, results to hydrogen showed that the positive gate voltage ($V_{GS} = 10$ V) decrease the response about two times, as opposed to the negative voltage ($V_{GS} = -10$ V) which increments the response more than three times (results for nitrogen dioxide registerd gas response decreased for both voltage polarization). Further, it was proved that higher negative voltage applied on the gate electrode is able to recover the sensor at lower temperatures in case of both oxidizing and reducing gases. Additionally, the negative voltage potential on gate electrode decreased the reaction time (response time) and the recovery time of the sensing element, as opposed to the positive potential, which demonstrated slow change mainly in the recovery time.

6 General conclusions and future perspectives

6.1 General conclusions

This thesis described and discussed the work performed to develop platforms for selective integration of 1D materials (nanowires) using state-of-the-art fabrication techniques, as well as the application of these structures as highly sensitive and selective gas sensing elements. The results showed that using currently available technology is possible to improve the integration of arrays of single-nanowires and the sensing capabilities of these systems by gradually modifying and optimizing the electrode arrays-based platform and the sensitive material. In particular, the characteristics of the electrode array-based platforms were found to play a key role in (1) the alignment of single NWs and (2) the overall gas sensing response and dynamics, especially in the arrangement including the third electrode under the sensitive nanowire. Below are described the most relevant findings of this thesis.

6.1.1 On the fabrication process

The results associated with the specific objectives linked to the fabrication process of single nanowire-based arrays for gas sensing applications are summarized below:

1. **Determination and optimization of nanowires processing techniques** – several steps to meet a general use of the NWs for their integration on the electrode platforms were explored. The core procedures included: (1) the separation of as-deposited NWs from the basic substrate using sonication in the water solution, (2) the transfer of dispersed NWs using drop coating deposition technique, and (3) the positioning and integration of NWs using dielectric forces to align and assemble the NWs across the faced electrodes. To ensure the optimal conditions these procedures were optimized at each step. It was found that (1) NWs removal process needs to carry with low power sonication to keep the NWs length up to 10 μm without significant length reduction. Also, that (2) the basic substrate with as-deposited NWs needs to be cut into small (1x1 mm) pieces to provide a good dispersion and to reduce the numbers of the NW in the solution together with small drop amount (5 μl). This aspect showed relevant to control the numbers of NWs assembled across the electrodes. The first chip generation of microelectrode platforms with various array and electrode modification (presented in **section 3.1.2**) was developed to optimize (3) the positioning and integration process using various settings of alternating electric field. The experiments using the first chip generation showed that multiple (WO$_3$) NWs interconnection was achieved by applying 5 V (peak-to-peak) with a frequency of 9 MHz. Results (presented in **section 3.2.2**) indicates that to achieve only single NW interconnection across the contact field with parallel faced microelectrode (with size several times more than a NW), is not feasible. The experiments showed that only the faced microelectrodes with spike end and gap around 3 μm could be successful in aligning single NWs. Therefore, the second chip generation included arrays with the finger electrode width

closely related to the diameter of nanowires (i.e., 75 nm approximately). Finally, the test of these structures confirmed the benefit of reducing the width of the finger electrodes to the nanoscale in allowing the alignment only single nanowires across the nanoelectrodes in the array (presented in **section 4.2**).

2. **Setting of the protocol for the fabrication of electrode arrays to provide mechanical support and electrical connectivity to single nanowires** – the first version of arrays with nanoscale features was introduced in the second generation chip (**section 4.1**). This first version was achieved by lift-off fabrication approach and presented in **section 4.2**. The results associated with this technology, especially the nanoelectrodes, revealed defects, such as fence-like features (redeposition), or poor electrical contact at nanoelectrode-microelectrode junction, which prevented their general usage. Thus, an optimized design is presented in **section 4.3.1**. This new design was fabricated by etch-back approach demonstrating better features such as well-shaped structures without major defects and no redeposited sidewalls. These results contributed to establishing an initial optimized fabrication protocol (introduced in **section 4.4.1**) to improve the fabrication of the nanoelectrode arrays. Although the second chip generation proved the concept of possible single NW alignment with nanoelectrodes (electrode width ≈ NW diameter), multiple NWs interconnection still prevailed after the dielectrophoresis step. Therefore, the modified design of third chip generation included (**section 5.1.1**), besides the nanoelectrodes, a narrow dielectric windows situated along the ends of the faced electrode. These two functional nanostructures altogether secured the success of the NWs alignment procedure. These results were included in **section 5.2.1**. The third chip was fabricated using multi-step throughout and nanofabrication process, including simulation of dose distribution in e-beam lithography using 4-inch wafer technology, described in **section 5.1.2**. All the experience gained during the tuning of the fabrication steps was summarized into the realization of this chip, which contains four independent arrays with nanoelectrodes for selective single NWs integration of various NWs types (selective sensing), and buried gate (third) electrode for enhancing of gas sensing properties (sensitivity enhancement).

3. **Assembling of the gas sensing system** – the first gas sensing tests based on WO_3 NWs were achieved using the second chip generation and backside ceramic heater assembled on TO-8 package with 12 pins (**section 4.3.3**). This heating element was made using thick-film technology with maximal operating temperature up to 280 °C, as presented in **section 4.4.3**. The heater was isolated by an interlevel alumina layer which (1) reduces thermal losses through the TO-8 package body, and also (2) provides the mechanical stabilization during the soldering, in which the heater contacts were electrically mounted to pins of TO-8 package by using high-temperature lead solder. The chip was mounted using a glue to the heater and electrically interconnected to the TO-8 package pins by gold wires. The same procedure of assembling was also used for the enhanced gas tests performed on the third chip generation.

The progress achieved during the fabrication and development of the nanoelectrode platforms with arrays consisting of single (gas sensitive) nanowires for gas sensing applications is summarized in **Table 16**.

Table 16. Most relevant characteristics of the three generations of chips fabricated to integrate arrays of single gas sensitive nanowires.

Progress made in the development of single NW-based arrays – electrodes platform			
	Design	**Fabrication**	**Alignment**
1ˢᵗ chip generation	12 microelectrodes arrays with different modifications (shape, spacing)	1 deposition, 1 lithography, 1 etching process	multiple NWs interconnections predominantly
2ⁿᵈ chip generation	4 nanoelectrodes arrays separated by hydrophobic stripes (15, 30, 45, 60 pairs of electrodes, 100-300 nm width)	2 deposition, 3 lithographies (1 e-beam), 2 etching process, fully assembled for gas tests	multiple and single NWs interconnections
3ʳᵈ chip generation	4 nanoelectrodes arrays separated by hydrophobic ring + buried gate electrode (5 and 9 pairs of electrodes, (200-300 nm width)	4 deposition, 6 lithographies (2 e-beam), 5 etching process, fully assembled for gas tests in the newly developed gas chamber	single NWs interconnections predominantly

6.1.2   On the sensing performance and characterization

The sensing platforms with nanoelectrode arrays assembled with WO_3 NWs were tested in the presence of various gaseous analytes. The results from gas measurements were summarized in the following conclusions:

4. **Development and implementation of the gas characterization system** – a new gas chamber for low current measurement, presented in **section 5.1.3**, was used for enhanced gas measurements with third generation nanoelectrode array platform containing (third) buried gate electrode. The chamber was developed with minimal dead volume strategy, which reduces empty space in the chamber at a minimum volume to 20 cm^3, resulting in ten times gas exchange rate per minute. Also, other optimizations of the chamber were employed, including (1) a special gas spreading shower which was designed for optimal spreading of the gas flow inside the chamber, (2) a degassing heating system enables to heat the chamber up to 120 °C, and (3) a PID regulation system control of the on-chip feedback temperature sensor AU220 which allows the sensing of temperature during the gas tests. In the production test of the chamber, the minimal applied current with a satisfactory S/N ratio was determined approximately 1 nA. The chamber was realized in the basic design (for electrical measurements), but a second variant is in progress for photoinduced reaction studies (i.e., using UV LED system).

5. **Gas sensing characterization in resistive mode** – two types of the NWs, namely, non-functionalized pristine WO_3 and Pt-functionalized WO_3, were integrated into the gas sensing platform using second chip generation, as presented in **section 4.4.3**, and validated on the presence of reducing gases (C_2H_5OH, NH_3, and CO) and oxidizing gas (NO_2). Gas

tests were performed in resistive regime using a various concentration of the gases mixed with synthetic air, finding the maximum response with good S/N ratio using constant current of 50 nA and temperature about 250 °C. Results validated the functionality of such a system, which provided a stable sensing performance at 250 °C for long-term measurements. Gas sensing elements represented by Pt-functionalized NWs demonstrated better response to C_2H_5OH, compared to the non-functionalized NWs systems, which responded better to NO_2 (see **Table 17**). These results were attributed to the additional chemical and electronic interactions at the interface of the Pt NPs and tungsten oxide NWs, which increase the pre-adsorption of oxygen species at the functionalized NW surface, as opposed to the non-functionalized surface of NW. Also, the responses to C_2H_5OH and NO_2 of gas sensing system based on single NWs aligned in the array was compared with similar systems based on single NWs in the literature. The comparison proved better sensing ability for the NW systems fabricated in this work. Further tests showed possible low cross-responses (selectivity) toward other analytes.

6. **Gas sensing characterization in enhanced mode** – enhanced gas sensing tests were performed based on non-functionalized WO_3 NWs. Results, shown in **section 5.2.2**, demonstrated thirteen-fold higher sensitivity to reducing gas (H_2) by modulating the NW channel via the application of a negative voltage on the third electrode. This effect was opposite with the positive voltage, with which the sensitivity registered a two-fold decrease compared to the zero (non-) applied voltage. On the contrary, results registered a decrease in the sensitivity to oxidizing gas (NO_2) while both positive and negative voltage was applied to the third electrode (see **Table 17**). These results were attributed to the depletion or accumulation of charge carrier density in the NW channel, which changes by the application of positive or negative voltage on the third electrode. This effect influences the depth of the depletion layer, which, in turn, is responsible for subsequent gas-solid interaction and the sensor response.

Table 17. Most relevant characteristics of the gas sensing tests using single NW-based arrays with nanoelectrodes.

Progress made in gas sensing using single NW-based arrays – nanoelectrodes platform							
		Gas response, SR (%)		NH_3 cross-response (***), ΔSR (%)		Gases	NWs
Resistive arrangement (*)		NO_2 (2.5 ppm)	C_2H_5OH (100 ppm)	NO_2 (1 ppm)	C_2H_5OH (10 ppm)		
2nd chip generation	WO_3	168	132	79	110	NO_2, C_2H_5OH, NH_3, CO	WO_3, Pt@WO_3
	Pt@WO_3	130	186	85	85		
		Gas response, SR (%)					
Enhanced arrangement (**)		I_{DS} = 5 nA		I_{DS} = 40 nA			
		NO_2 (5 ppm)	H_2 (1000 ppm)	NO_2 (5 ppm)	H_2 (1000 ppm)		
3rd chip generation	(V_{GS} = -10V)	~ 60	640	75	315	NO_2, H_2	WO_3
	(V_{GS} = 0V)	75	190	115	150		
	(V_{GS} = 10V)	25	75	40	45		
Operating temperature: (*) 250 °C, 50 nA, (**) 200 °C; (***) selectivity: NH_3 = 10 ppm							

6.2   Future work

In this section, it is summarized the possible further steps, considered by the author as promising or innovative ideas, that could push forward a generalized application and implementation of single semiconducting nanowires not only for gas sensors but also for other chemical sensors.

NWs processing and integration techniques further optimization

Some of the NWs processing techniques, including NWs separation from the basic substrate, transfer, and deposition of the NWs drop, can be optimized by tuning of their parameters necessary for the following processes. The NWs integration process using DEP forces to provide the assembling the NWs over the electrodes can be enhanced by additional electric field, which helps to concentrate the movement forces in the center, i.e., between the faced nanoelectrodes, as was described in [151]. For this purpose, it can be used the gate electrode that is already implemented in the third chip generation.

Design and fabrication process upgrade

The chip design, as was presented in this work, is capable to integrate only four types of sensitive material, because the design consists of only four nanoelectrode arrays. Increasing the number of electrode arrays extends the possibility to integrate more types of NWs, which, in turn, would increase the selectivity of the sensor toward more gaseous analytes.

Another future modification the integration of similar nanoelectrode arrays on a micromachined hotplate to replace the current heater made by thick-film technology. The advantage of micromachined hotplates on the thermally isolated membrane is connected with

the reduction of power consumption of such a sensing device. In the same line, a decrease of the power consumption of the sensor based on single NWs aligned in parallel could also be achieved by modulating the self-heating effect of the NWs when sourced to a current or voltage. Notice that devices based on self-heated NWs do not need any external heating system to set the optimum sensing temperature but use four-wire measurement method to heat the NWs and receive their gas responses at the same time.

The future works could also be focused to modify and optimize the sensor assembling process in order to reach higher throughput and efficient fabrication in large scale.

Gas sensing and characterization

The integration of NW with other surface modifications could allow the detection of more gaseous analytes, including volatile organic compounds, such as acetone, ethanol, or toluene, which are typically involved in various diseases in human breath and are attractive for early disease diagnosis. Research on this topic is currently undergoing in our research group using semiconducting nanowires with nanoscale heterojunctions. These new materials could be integrated into the platforms developed in this thesis.

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List of abbreviations

Short-cut	Definition
FEEC	Faculty of Electrical Engineering and Communications
BUT	Brno University of Technology
PVD	Physical Vapor Deposition
CVD	Chemical Vapor Deposition
AACVD	Aerosol-Assisted Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
NW	NanoWire
NP	NanoParticle
M-NW	Multiple Nanowire
S-NW	Single Nanowire
DEP	Dielectrophoresis
DESCUM	Descumming process, plasma ashing
TO-8	Package (round shape) with 12 pins
IDE	Inter-Digital Electrodes
MOX	Metal-Oxide Semiconductor
FET	Field-Effect transistor
VLS	Vapor-Liquid-Solid CVD material growth method
VS	Vapor-Solid CVD material growth method
DEMI	Demineralized water
IPA	Isopropylalcohol
DWL	Direct-Write Laser
EBL	Electron-Beam Lithography
SEM	Scanning-Electron Microscopy
AFM	Atomic-Force Microscopy
UHV	Ultra-High Vacuum
HV	High Vacuum
UV	Ultra-Violet spectrum
RIE	Reactive-Ion Etching
IBE	Ion-Beam Etching
IBAD	Ion-Beam Assisted Deposition
RFICP	Radio Frequency Inductive-Coupled Plasma
SIMS	Secondary Ion-Mass Spectroscopy
PSF	Point-Spread Function
PEC	Proximity Effect Correction
CCD	Charge-Coupled Device
DT	Dose Test
AC	Alternate
Au	Gold
Ti	Titanium
NiCr	Nickel-chromium
SiO_2	Silicon dioxide
Al_2O_3	Alumina ceramic
TCR	Temperature Coefficient of Resistance

List of symbols and physical constants

Symbol	Definition	Unit
SR	Sensor response	%
R_{air} (R_0)	Resistance in air	Ω
R_{gas} (R_{max})	Resistance under gas exposure	Ω
(φ_i)	Flux of molecules impinging a surface	-
m	Mass of molecule	-
P	Pressure	Pa/mBar
k_B	Boltzmann constant ($1.380648 \cdot 10^{-23}$)	$J \cdot K^{-1}$
T	Temperature	K
E_A	Adsorption energy	$kJ \cdot mol^{-1}$
E_D	Desorption energy	$kJ \cdot mol^{-1}$
T_{max}	Optimal temperature for chemisorption	K
k_L	Adsorption coefficient	-
k_{ads}	Rate constant for adsorption	-
k_{des}	Rate constant for desorption	-
H_{Chem}	Reaction heat for chemisorption	$kJ \cdot mol^{-1}$
ε_r	Relative permittivity	-
ε_0	Permittivity of vacuum ($8.854187 \cdot 10^{-12}$ $F \cdot m^{-1}$)	$F \cdot m^{-1}$
D^+	Density of singly charged donors	m^{-3}
A^-	Density of singly charged acceptors	m^{-3}
L_D	Depth of depletion layer	m
e	Elementary charge ($1.602176 \cdot 10^{-19}$)	C
n	Number of electrons	-
p	Number of holes	-
μ_n	Electron mobility	$m^2 \cdot V^{-1} \cdot s^{-1}$
μ_p	Hole mobility	$m^2 \cdot V^{-1} \cdot s^{-1}$
λ_D	Debye length	m
D	Grain diameter	m
eV_s	Barrier height	eV
E_C	Conduction band	eV
E_F	Fermi level	eV
E_V	Valence band	eV
I_{DS}	Drain-source current	A
V_{DS}	Drain-Source voltage	V
V_{GS}	Gate-Source voltage	V
RT	Room temperature	°C
V_{pp}	Peak-to-peak voltage	V
f	Frequency	Hz

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Curriculum Vitae

PERSONAL INFORMATION

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Place of birth:	Zlín, Czech Republic
Nationality:	Czech
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EDUCATION

2013 – Present   Brno University of Technology / Department of Microelectronics
Postgraduate doctoral study, Microelectronics,
Doctoral thesis: Progress toward the development of single nanowire-based arrays for gas sensing applications.

2011 – 2013   Brno University of Technology / Department of Microelectronics
Master study, Microelectronics,
Master thesis: Polyethylenterephthalate copper plating for conductive structures realization.

2008 – 2011   Brno University of Technology / Department of Microelectronics
Bachelor study, Microelectronics,
Bachelor thesis: Laboratory and low series double layer PCB's production in PROTOCAD laboratory.

WORK EXPERIENCE

2013 – Present   Smart Nanodevices – Micro/Nano Fabrication Specialist (PhD student)
Brno University of Technology – Central European Institute of Technology (CEITEC), Purkyňova 123, 61200 Brno (Czech Republic).

Fabrication of nanoelectrode arrays for gas sensing applications:

- Material depositions: PVD (evaporation, sputtering), CVD (PECVD, ALD),
- Micro/Nanolithography: optical (DWL, through-mask), and e-beam lithography,
- Material etchings: dry etching techniques (RIE, DRIE, IBE),
- Characterization techniques: fabrication (SEM, EDX, AFM, profilometry, SIMS, electrical tests), gas sensing (multiple/single nanowires sensors testing).

ADDITIONAL INFORMATION

Participation in funded projects

- Surface modified nanowires for selective detection of volatile organic compounds (NoWSens) (GAČR 17-16531S), Grant Agency of Czech Republic - Standard Grants, 2017 – 2019, early-stage researcher,
- CEITEC - Central European Institute of Technology (CZ.1.05/1.1.00/02.0068), Ministry of Education, Youth and Sports ČR, 2011 – 2015, Research group fund, early-stage researcher,
- Nano-Electro-Bio-Tools for Biochemical and Molecularly-Biological Studies of Eukaryotic Cells (NanoBioTECell) (GAP102/11/1068), Czech Science Foundation - Standard Grants, 2011 – 2015, early-stage researcher,
- Study of contribution of different DNA-damaging mechanisms to toxicity of cytostatics to human chemosensitive and chemoresistant neuroblastomas (GAP301/10/0356), Czech Science Foundation - Standard Grants, 2010 – 2014,

- International Cooperation in the Field of Nanotechnologies with In Vivo Imaging Techniques (CZ.1.07/2.3.00/20.0148), MEYS - OP Education for Competitiveness, 2012 – 2014, early-stage researcher,
- Partner Network for Bionanotechnological and Metallomic Research (CZ.1.07/2.4.00/31.0023), MEYS - OP Education for Competitiveness, 2012 – 2014, early-stage researcher,
- Support of the development of high-quality teams in R&D in the field of material science (CZ.1.07/2.3.00/20.0029), MEYS - OP Education for Competitiveness, 2011 – 2014, early-stage researcher.

PERSONAL SKILLS

- English (C1), Spanish (A1),
- Designer and technologist in micro/nano technology (kLayout, Cadence Virtuoso Design),
- Designer of electronic circuits and systems (Cadence OrCAD PSpice, Eagle),
- Graphical software (3ds Max, Fusion 360, Adobe Photoshop & Illustrator, Autodesk Inventor, SolidWorks),
- Analysis software (Gwyddion, OriginLab).

INTERNSHIPS

04-08/2016	Internship at University of Barcelona, Barcelona, Spain (program ERASMUS+) Characterization and measurement of gas sensor based on various single nanowires aligned in array.
09-11/2017	Internship at Institute of Microelectronics of Barcelona IMB-CNM, Barcelona, Spain (program ERASMUS+) Synthesis of nanowires and analysis of materials; completion of a training program to get access to infrastructure and complementary facilities at IMB-CNM.
07/2018	Internship at Institute of Microelectronics of Barcelona IMB-CNM, Barcelona, Spain (FREEMOVERS fund) Evaluation of the initial dataset of gas tests realized for the new generation of single nanowire-based sensors with third electrode.

OTHER RESULTS

2014	Test chamber for organic material in inert atmosphere (prototype),
2017	Heating platform for TO-8 package with 12 pin outlets (functional sample),
2017	Electrode array of parallel nano-contacts for selective nanowires alignment designed for sensors applications – 1st generation (functional sample).
2018	Electrode array of parallel nano-contacts for selective nanowires alignment designed for sensors applications – 2nd generation (functional sample).
2019	Gast chamber for low current measurement for TO-8 packages (prototype).