BRNO UNIVERSITY OF TECHNOLOGY

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ANALOG IMPLEMENTATION OF FRACTIONAL-ORDER ELEMENTS AND THEIR APPLICATIONS

ANALOGOVÁ IMPLEMENTACE PRVKŮ NECELOČÍSELNÉHO ŘÁDU A JEJICH APLIKACE

SHORTENED VERSION OF PH.D. THESIS

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KEYWORDS

Analog integrated circuit, circuit connections, fabrication, fractional calculus, fractional-order capacitor, fractional-order derivative, fractional-order device, fractional-order element, fractional-order inductor, fractional-order integrator, fractional-order system, fractional-order oscillator, solid-state fractional-order capacitor.

KLÍČOVÁ SLOVA

Analogový integrovaný obvod, obvodové zapojení, výroba, počet neceločíselného řádu, kapacitor neceločíselného řádu, derivace neceločíselného řádu, zařízení neceločíselného řádu, prvek neceločíselného řádu, induktor neceločíselného řádu, integrátor neceločíselného řádu, systém neceločíselného řádu, oscilátor neceločíselného řádu, kapacitor s pevným dielektrikem neceločíselného řádu.

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Dissertation is available at the Scientific and Foreign Department of Dean's Office FEEC, Brno University of Technology, Technická 10, Brno, 616 00

MÍSTO ULOŽENÍ PRÁCE

Disertační práce je k dispozici na Vědeckém a zahraničním oddělení děkanátu FEKT VUT v Brně, Technická 10, Brno, 616 00

CONTENTS

1   INTRODUCTION

Fractional calculus, the branch of mathematics regarding differentiations and integrations to non-integer orders, is a field that has been introduced 300 years ago [1]. Inspiring from the fractal models in the environment, from integer to non-integer models was explored. It origins from 30th of September in 1695 between Leibniz and L'Hopital correspondance, with L'Hôpital inquiring about Leibniz's notation, $d^n y/dx^n$ where n is a positive integer. L'Hôpital addressed in this letter the question [2]: what happens if this concept is extended to a situation, when the order of differentiation is arbitrary (non-integer), for example, $n = 1/2$? Since then the concept of fractional calculus has drawn the attention of many famous mathematicians, including Euler, Laplace, Fourier, Liouville, Riemann, Abel, and Laurent.

Considering the non-integer order n, such as 1.3, $\sqrt{2}$, $3j$-4 or any other real or imaginary order, the differentiation $d^n f(t)/dt^n$ is solved by fractional calculus. Understanding the solutions of fractional-order differential equations is the key to building better models for fractional order dynamic systems. The most significant definitions are Riemann-Liouville, Grünwald-Letnikov approaches and Caputo definition [1] which is described as:

$$
{}_a D_t^\alpha f(t) = \frac{1}{\Gamma(n-\alpha)} \int_a^t \frac{f^{(n)}(\tau)}{(t-\tau)^{\alpha+1-n}} d\tau , \tag{1.1}
$$

where n-$1 < \alpha < n$. The main advantage of Caputo's approach is that the initial conditions for fractional differential equations take on the same form as integer-order differential equations. Mathematical expressions such as difference or differential equations may be considered as advanced mathematical or analytical models and they are preferred to the simpler models once the application becomes complicated. Mathematical models are categorized into groups such as time continuous or time discrete, lumped or distributed, deterministic or stochastic, linear or nonlinear. Each of these adjectives marks a property of the used model for the dynamic system and thus determines the type of the equation.

1.1   Fractional Calculus in Electrical Engineering

Time has proven Leibniz as the applications of fractional calculus e.g., differentiation or integration of non-integer order, has seen explosive growth in many fields of science and engineering. These mathematical phenomena allow us to better characterize many real dynamic systems. The first applications were in the tautochrone problem, electromagnetic theory [3], semi-infinite lossy transmission line [3]. Other systems that are known to display fractional-order dynamics are electrode-electrolyte polarization [4], [5], dielectric polarization [6], electromagnetic waves, an ideal capacitor model [7], [8] etc. As many of these systems depend upon specific material and chemical properties, it is expected that a wide range realization of fractional-order behaviors are also possible using different materials.

There are two methods for realization of fractional-order integral and derivative operators. First one is digital realization based on microprocessor devices and appropriate control algorithm and the second one is analogue realization based on analog circuits. An analog circuit emulating fractional-order behavior is often modeled by fractional-order differential equations based on the current-voltage relationship of the electrical circuits. They are called as fractional-order elements

(FOE), and fractional-order capacitor (FOC) or fractional-order inductors (FOI) defining the integrator and differentiator operators, respectively. Since their mathematical representations in the frequency domain are irrational, direct analysis methods and corresponding time domain behavior seem difficult to handle. Therefore, design of FOEs is done easily using any of the rational approximations [9]−[14]. However, no specific method for recovering a fractional process model was provided. These methods also have computational difficulties in higher orders thus their practical realization becomes more complex.

Fractional-order systems, or systems containing fractional derivatives and integrals, have been studied in many engineering areas [15]−[19]. These systems constructed using n number of FOEs are described with an nth-order fractional systems of fractional differential equations. For instance, fractional-order oscillators are designed considering the FOEs with an order of less than one, thus the total system order decreased from two or three as known from the integer-order systems. However, the oscillation criterion is still sustained.

Identification on real systems has shown that fractional-order models can be more intrinsic and adequate than integer-order models in describing the dynamics of many real systems [20], [21]. Indeed, the fractional derivatives provide an excellent tool for the description of memory and hereditary properties of various materials and processes. This is the main advantage of fractional-order models (fractional derivatives) in comparison with classical integer-order models, in which such effects are in fact neglected. Moreover, defining a system as fractional is that the fractional-order gives an extra degree of freedom (coming from its arbitrary order) in controlling the system's performance. It leads researchers to believe that the future of discrete element circuit design and fabrication of single solid-state components will undergo a paradigm shift in favor of FOEs.

1.2 Research Objectives

Particular importance is the use of fractional-order models and their applications in analog circuit design. Studies show that a huge portion of FOEs realizations — about 90% — are of multicomponent FOEs; moreover, it was found that about 80% of these existing FOEs are realized on FOC part with poorly control of constant phase angle [22]. Some of the challenges generally in fractional-order systems are shortly described in Fig. 1.1. Since the application of FOCs in analog domain offer tunability, independent control of parameters between each other, it is expected that their integrated circuit design will result in considerable benefit. Therefore, the main contribution of the author of the thesis is the development of optimum design for passive FOEs for systems described by fractional dynamic models and increasing their availability in analog electronic circuit design. This contribution comprises three consecutive parts:

- Optimization: Instead of approximating the rational functions of irrational transfer functions using the approximations at a certain frequency (or bandwidth), the phase and/or impedance responses of RC/RL networks in the whole desired frequency range is optimized. This is achieved with a new approach based on the mixed integer-order genetic algorithm (GA) to obtain accurate phase and magnitude response with minimal branch number and optimum passive values [23]. Standardized, IEC 60063 compliant commercially available passive component values are used; hence, no correction on passive elements is required which leads us to a decrease of phase angle deviation and overall enhancement of the performance of the FOE.
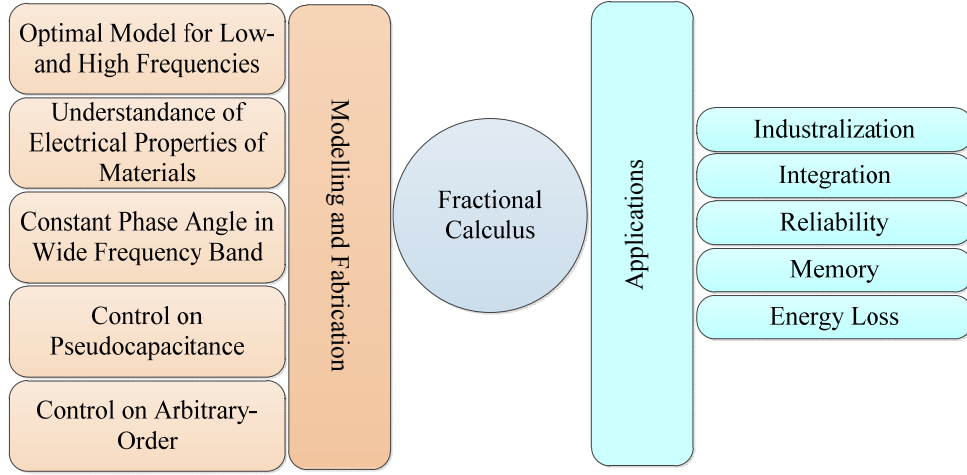
Fig. 1.1: Challenges in fractional-order dynamic systems

This approach is also used in modelling of filler in double layer capacitor [24] to find the best fit of fabrication of FOC with hexagonal-boron nitride (*h*BN) over a frequency range of five decades.

- Integration: The main objective of this part is to introduce a new analogue implementation of FOEs and their applications in oscillator design using compact CMOS active building blocks (ABBs) with reduced transistor count. The first implementation is the design of fractional-order integrator, which is a synonym of FOC in analog design, using cascade of first-order BTSs. The performance of this circuit is used in fractional-order proportional-integral (FOPI$^\lambda$) control [25] for a speed control system of an armature controlled DC motor, which is often used in mechatronic and other fields of control theory. The second implementation is the fractional-order oscillators. The increased circuit complexity, the power dissipation of the active cells becomes quite high. In order to overcome this obstacle, novel very simple voltage–mode (VM) fractional-order oscillator topologies are introduced [26]−[28].

- Experimental verification: The accuracy and stability of proposed FOEs and their primary versions are experimentally verified on real-life analog electronic circuits. The solid-state, PCB compatible polymer composite based FOCs [24], [29] are tested in circuit network connections considering the identical- and arbitrary-orders of the elements. The theory of fractional-order circuit network connections is formulated and experimentally verified [30], [31]. This study helps to show the stability of the solid-state FOCs. Moreover, the PCB-compatible FOCs fabricated using molybdenum disulfide (MoS$_2$)-ferroelectric polymer composites [32] are used in Wien oscillator [33].

2   A SURVEY ON FRACTIONAL-ORDER ELEMENTS AND DEVICES

In electrical engineering in particular, the constant-phase behavior of capacitors is explained as the frequency dispersion of the capacitance by dielectric relaxation, where the electric current density follows changes in the electric field with a delay. In 1994, to express this phenomenon of "off the shelf" real capacitors mathematically, the capacitance current in the time domain was given as [8]
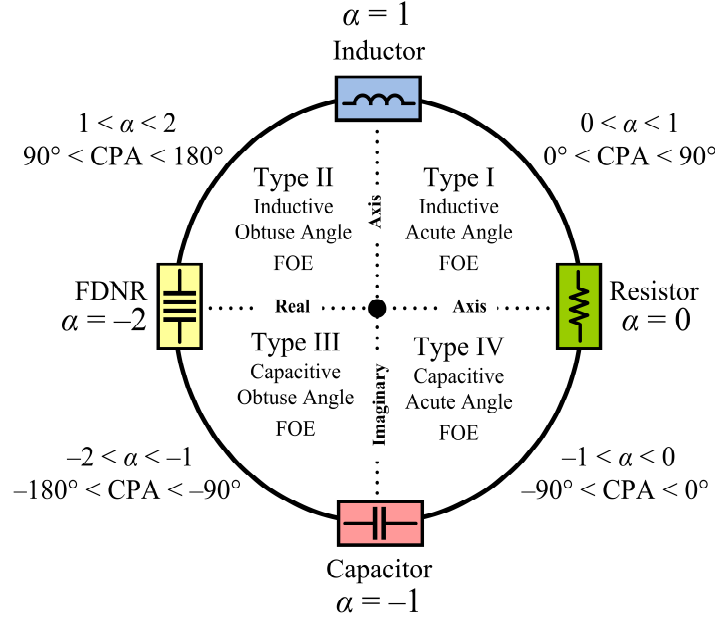
$$i(t) = C\frac{d^\alpha u(t)}{dt^\alpha},$$
(2.1)

Fig. 2.1: Description of fractional-order elements in four quadrants [34]

where $d^{\alpha}u(t)\big/dt^{\alpha}$ denotes the "fractional-order time derivative". In same way, the given relationship for FOI is expressed as:

$$i(t) = \frac{1}{L} \int_{-\infty}^{t} u(t)dt^{\alpha} ,$$

(2.2)

where $\int_{-\infty}^{t} u(t)dt^{\alpha}$ denotes the "fractional-order time integral" with having the order $0 < \alpha < 1$.

Fig. 2.1 shows these fundamental components in frequency domain and possible FOEs in four quadrants [34]. Their impedance is described as $Z(s) = Ks^{\alpha}$, where ω is the angular frequency in $s = j\omega$, and the phase is given in radians ($\varphi = -\alpha\pi/2$) or in degrees (°) ($\varphi = -90\alpha$). Obviously the impedance of the FOE has a real part dependent on the non-zero frequency and its magnitude value varies by 20α dB per decade of frequency. In particular, the impedance of Type IV FOEs, i.e. FOCs in quadrant IV, is provided with an order of $-1 < \alpha < 0$ and pseudocapacitance of $C_{\alpha} = 1/K$, whereas FOIs in quadrant I (Type I) have an order of $0 < \alpha < 1$ and pseudoinductance of $L_{\alpha} = K$. Their units are expressed in units of farad·sec$^{\alpha-1}$ (F·s$^{\alpha-1}$) and henry·sec$^{\alpha-1}$ (H·s$^{\alpha-1}$). The higher order FOCs and FOIs with the described impedances then matched in quadrant II and III (Type II and III), respectively. Their characteristics such as pseudocapacitance, pseudoinductance, constant phase zone (CPZ), constant phase angle (CPA – defined phase angle in CPZ), and phase angle deviation (PAD – maximum difference between a designed/measured phase and a target phase) profoundly impact the transfer function of the fractional systems [35]−[37]. Therefore, in order to practically realize fractional operators, a finite, infinite, semi-infinite dimensional integer-order system resulting from the approximation of an irrational function can be used. This equivalent integer-order transfer functions then can be used also in design of analog integrator and differentiator circuit by selecting proper time constant or correct distribution of zeros and poles of the function.

2.1 Discrete Element Realizations of Fractional-Order Elements

Numerous methods for synthesis of FOEs have been proposed. They differ by the approximation of their functions. They are expanded using analytical methods to calculate the parameters of their equivalent circuits. They consist of capacitors and resistors, which are described by conventional (integer) models; however, the circuit itself may have non-integer order properties, becoming a so-called constant phase element, or fractional-order capacitor. The realization of fractional order inductors using resistive/inductive networks are limited due to their size, cost and limited operating frequency range. Therefore, the research on this area remained limited. A number of mathematicians and scientists have proposed various models [1], [22] e.g. Vaschy and Heaviside (1890), M. I. Pupin (1899), George A. Campbell (1903), Karl Willy Wagner (1915), Wilhelm Cauer (1930-1940), Sidney Darlington (1939), Ralph Morrison (1959), Donald C. Douglas (1961), Robert M. Lerner (1963), G. E. Carlson and C. A. Halijak (1964), , Suhash C. Dutta Roy (1966), K. Steiglitz (1967), C. A. Hesselberth (1967), Keith B. Oldham (1973), J. C. Wang (1987), A. Charef (1992), M. Nakagawa and K. Sorimachi (1992), K. Matsuda (1993), A. Oustaloup (1995), M. Sugi (2002), D. Xue (2006), P. Yifei (2005), A. A. Arbuzov (2008), J. Valsa (2011), D. Sierociuk (2011), R. El-Khazali (2014). However, there are several drawbacks on these proposed methods/models:

- Approximated rational functions require complex mathematical analysis.
- Constrained optimization to identify the network.
- The value of the components are not well-scaled and negative values may be obtained, in which case one would need to use negative impedance converters.
- Obtained values have to be approximated to closest a standardized value which leads to overall degradation of the performance of the FOE.
- High numbers of elements are used for low phase error, in which clearly requires increased branch number thus high-order transfer functions.
- High numbers of elements also requires large circuit layout which results in extra parasitic due to the transmission line effects especially at high frequencies.

2.2 Development of Fractional-Order Devices

An ideal dielectric in a capacitor would violate causality. Thus, it is typical to look for dielectrics for instance "low-loss" dielectrics for the order "α" of s as close to unity as possible, as the exponent is directly related to the constant phase angle. This can be explained in electrical engineering as the frequency dispersion of capacitance by dielectric relaxation, where the electric current density follows the change of an electric field with a delay [38]. This statement clearly shows that an ideal capacitor cannot exist in nature. Considering also the definition of Warburg impedance, the impedance varying as the square-root of frequency, several FOCs are designed and fabricated. Many of the studies are done after 1990s [31], [36], [39]−[46] since the connection between math's and physical properties of materials established after this year [8]. However, to make such components as widely used as the conventional passive components, it is necessary to satisfy the design and the technology with the following requirements:

- Compatibility with manufacturing technology of semiconductors or thin-film integrated circuits.
- Constant phase response for a wide frequency spectrum.

- Fractional impedance dependence on the maximum range of allowed order "$0 < \alpha < 1$".
- Precise adjustment of the fractional impedance parameters and characters, especially the control on pseudocapacitance "C_α".
- Capability of parameter dynamical adjustment.
- Suitable packaging for circuit applications.
- Size in terms of electrodes.
- Longevity of the lifetime.

3 SYNTHESIS AND OPTIMIZATION OF FRACTIONAL-ORDER ELEMENTS USING A GENETIC ALGORITHM

Up until now, evolutionary computing algorithms have been used to reduce the drawbacks in traditional optimization methods and to solve complex problems where conventional techniques fail in many areas of the fractional-order domain. In this chapter, a mixed integer-order GA in MATLAB® is employed [47]. Instead of approximating s^α at a certain frequency (or bandwidth), the phase and/or impedance responses of RC/RL networks are optimized in the whole desired frequency range. Furthermore, the required values are obtained with GA, even if the passive component values are restricted to commercially available kit values defined by standard IEC 60063. Hence, this chapter aims to introduce an FOE optimization method that achieves a broad operating frequency range with CPA deviation of approximately ±1° using commercially available passive component values in RC and RL structures with five branches. Most crucially, the presented approach avoids the use of negative component values, GICs, or random passive element values. Thus, the best optimal emulation of an FOE is introduced currently available in the literature. In particular, Foster-II and Valsa networks [23] are selected as our main objective, because the former offers a minimum total capacitance value and the latter provides a minimum CPA deviation. Here it is also worth noting that, to the best knowledge of the author, an FOI design using the listed five RL networks is studied for the first time in the open literature.

3.1 Optimization and Verification of FOC

The measurement results of $\alpha = -0.5$ order FOCs, that designed with six branches of the Valsa network, using an ENA Series Network Analyzer E5071C (300 kHz–20 GHz) in three different frequency ranges [case study (a) in 1 MHz–100 MHz, (b) 5 MHz–500 MHz, and (c) 50 MHz–1 GHz] are shown in Fig. 3.1. Two variants of the FOE device with dimensions of 20 mm × 20 mm were designed (for 0402 and 0603 size passive components) employing a subminiature version A (SMA) coaxial RF connector. The fabricated printed circuit board for 0402 size kit values is shown in Fig. 3.1(c) as an inset. Considering an input impedance 50 Ω of the connector, the phase is measured by defining the equation of impedance as $Z = 50 \cdot [(1 + S_{11})/(1 - S_{11})]$. As passive elements, RF-type resistors from Vishay [48] and capacitors from Kemet [49] are used. Because of the producers fabrication boundaries, used passive components having CPA in limited frequency range, operate up to a maximum of 5 GHz. In addition, this frequency range is inversely proportional to the resistance values. For instance, a 100 Ω resistor works until 8 GHz, whereas a 1 kΩ resistor has a constant zero-degree phase response up to 800 MHz and so forth. At high frequencies, the transmission line effect becomes dominant; therefore, we maintain the
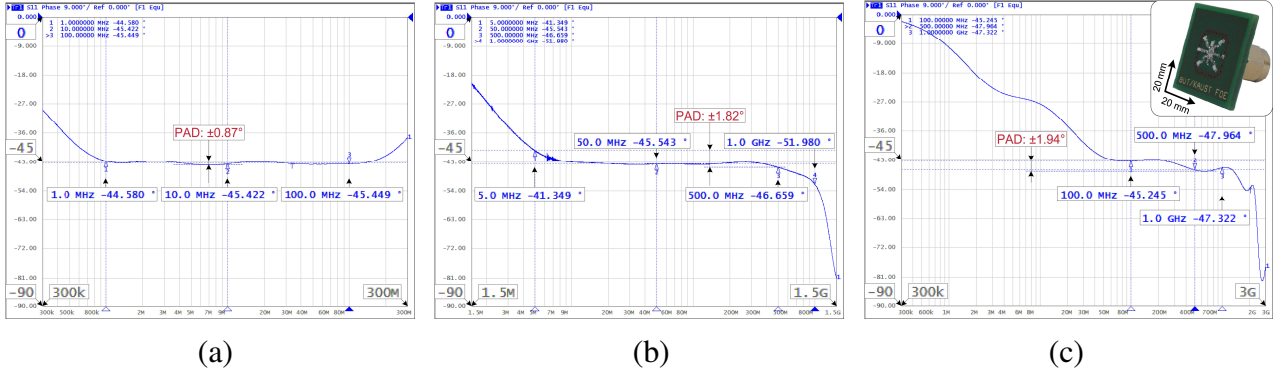
| (a) | (b) | (c) |

Fig. 3.1: Measurement results of an α = −0.5 order FOC implemented using the Valsa network optimized using GA for two decades in different frequency ranges: (a) 1 MHz – 100 MHz, (b) 5 MHz – 500 MHz, and (c) 50 MHz – 1 GHz
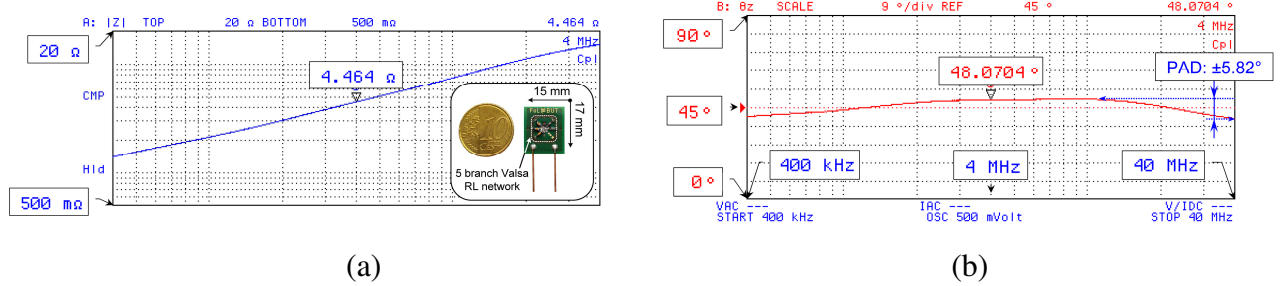

| (a) | (b) |

Fig. 3.2: Measurement results of an α = 0.5 order FOI from Fig. 3.8 and the fabricated device with dimensions of 15 mm × 17 mm as in inset (blue line − impedance response; red line − phase response)

distance between passive elements the least. Despite the above mentioned limitations, we obtained the results until 1 GHz with low phase angle deviations as shown in Figs. 3.1(a)−(c).

3.2 Optimization and Verification of FOI

The most popular technique to mimic an inductor is using a GIC employing Op-Amps, resistors, and capacitors [50], [51]. However, the performances of these GIC-based active inductance simulators often suffer from the non-idealities of Op-Amps. Therefore, this section deals with the optimal emulation of an FOI for the first time in the literature. The FOI design using the GA is studied numerically and experimentally verified.

The Valsa RC network is modified to RL-type structure by replacing all capacitors with inductors. The behavior of an α = 0.5 order FOI was verified using the Agilent 4294A precision Impedance Analyzer. Standard calibration tests (open and short circuits) of the 16047E Test Fixture were performed to calibrate the instrument. During the experimental validation in the frequency range 400 kHz – 40 MHz (801 logarithmically spaced points in two decades), a sinusoidal input signal with a default AC voltage of 500 mV and a frequency of 1 MHz was applied, while one of terminals was grounded. The measurement results and a photograph of the fabricated device with dimensions of 15 mm × 17 mm are depicted in Fig. 3.2. The measured PAD in two decades of the frequency range of our interest is ±5.82°.

3.3 Discussions

The GA generally provides the minimum total capacitance value and can be limited in any range of the designer's choice. As the order increases, the total capacitance increases and the resistance decrease, as shown in Fig. 3.3(a). Maintaining the order constant and increasing the capacitance value provides the same results as in the previous case. The frequency effect on the values is shown in Fig. 3.3(b). At high frequencies, small R and C values are used, whereas larger passive values are used at low frequencies. This fact can be explained by the dissipation factor (DF) expressed as $DF = ESR / X_C$, where ESR and X_C denote the equivalent series resistance and capacitors reactance, respectively, or as a tangent of the loss angle [52].

Fig. 3.4 shows the distribution of R and L values depending on an order and the frequency range for FOI design. Different to the FOC evaluation, resistance and inductance vary linearly with an order. It is also clear that an increasing FOI order has the effect of increasing passive values. This result can be explained by the quality factor (Q) definition $Q = X_L/R$, where X_L is the inductive reactance and R is the DC resistance [53]. Maintaining the Q constant, increasing an order (effecting X_L) has the effect of increasing the R. At low frequencies and within limits, both passive values become much greater than their equivalents at high frequencies.

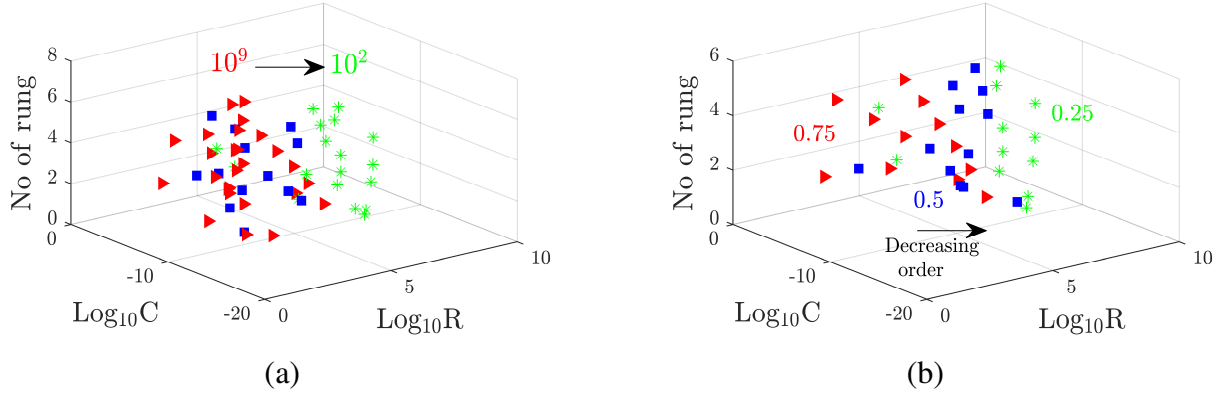(a)   (b)

Fig. 3.3: (a) Order and (b) frequency effect on R and C values on each rung of the Foster-II and Valsa structures for FOC design
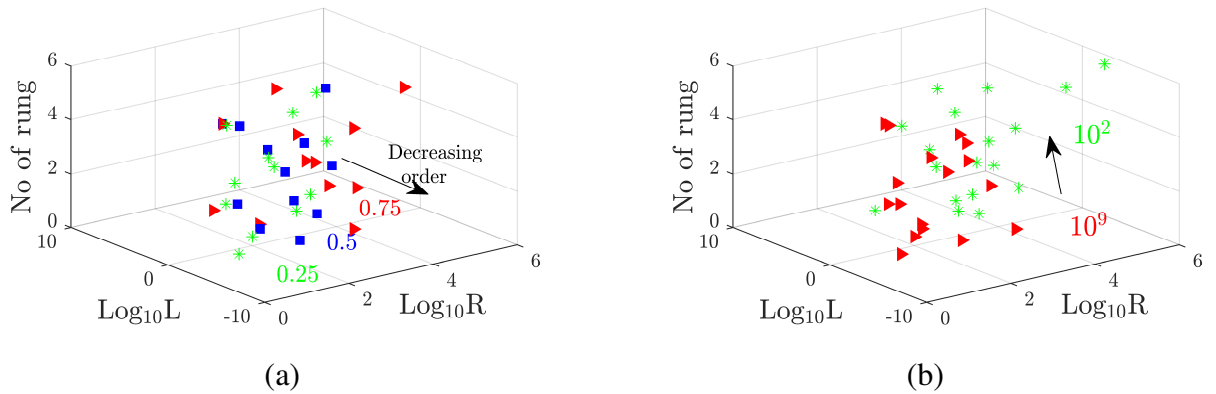

(a)   (b)

Fig. 3.4: (a) Order and (b) frequency effect on R and L values on each rung of the Valsa structures for FOI design

4 ANALOG IMPLEMENTATION OF FRACTIONAL-ORDER PI$^{\lambda}$ CONTROLLERS

In this chapter, particularly, fractional-order integral operator $s^{-\lambda}$ (integrator I$^{\lambda}$, where $0 < \lambda < 1$) is implemented employing two-stage Op-Amps. Cascade of first-order bilinear transfer segments (BTSs) is used, which is a two-port network with a single pole and a single zero. The behavior of both proposed analogue circuits employing two-stage Op-Amps is confirmed by SPICE simulations using TSMC 0.18 µm level-7 LO EPI SCN018 CMOS process parameters with ±0.9 V supply voltages. The cascade of BTSs creates so-called constant phase block, which generates desired magnitude and phase response by proper setting of both polynomial roots (zero and pole frequencies) of each BTS [54]. This approach ensures direct emulation of the behavior of an I$^{\lambda}$, which is very beneficial for fractional-order PI$^{\lambda}$ (FOPI$^{\lambda}$) design. FOPI$^{\lambda}$ controller, which is used as an application of I$^{\lambda}$ in this chapter, are widely used in industrial applications because of their simplicity and applicability to wide range of industrial control problems. In recent years, the survey [55] indicates fractional-order controllers become an emerging research topic. While design, these controllers have an additional degree of freedom and thus offer potential reduction of the control effort, which also results in reduction of wasted energy. Furthermore, their analog implementation allows us to integrate full design in chip and tune the control parameters easily.

4.1 Fractional- Order PI$^{\lambda}$ Controller Design

Block diagram of a proposed integrator I$^{\lambda}$ by cascade connection of first-order BTSs and first-order low-pass filter (LPF) is depicted in Fig. 4.1 and can be expressed as:

$$K_{\mathrm{I}^{\lambda}}(s) = \frac{V_{\mathrm{I}}(s)}{V_{\mathrm{S}}(s)} = \frac{\prod_{i=1}^{m}(s - z_i)}{\prod_{j=1}^{n}(s - p_j)} = \left. \frac{\sum_{i=1}^{m} a_i s^i}{\sum_{j=1}^{n} b_j s^j} \right|_{z_i, p_j \in \Re}, \tag{4.1}$$

where m denotes total number of BTS needed for the design of constant phase block and $n = m + 1$ will be mathematical order of the final circuit due to use of an additional LPF. The usefulness of LPF is described below.

Proposed realization of BTS using two ideal Op-Amps (assuming open loop gain $A \to \infty$) and a set of passive components is shown in Fig. 4.2(a), while the non-inverting LPF is depicted in Fig. 4.2(b). Hence, transfer function (TF) of cascade of m BTS and LPF in our particular case as depicted in Fig. 4.1 can be expressed as:
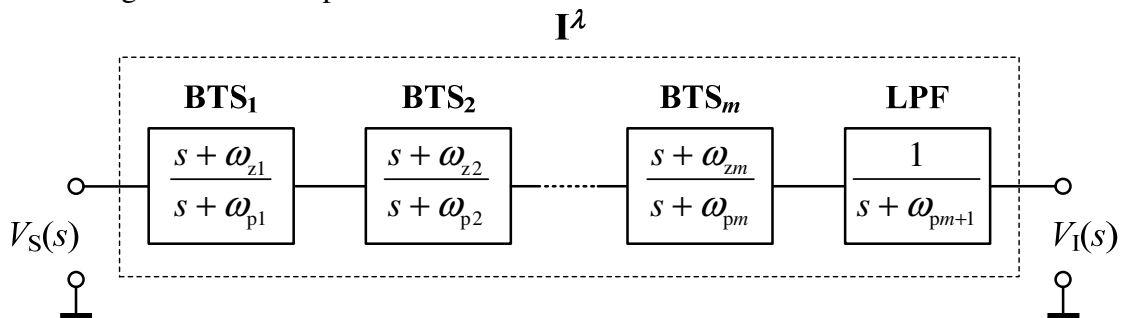

Fig. 4.1: Block diagram of a fractional-order integrator using BTSs and LPF
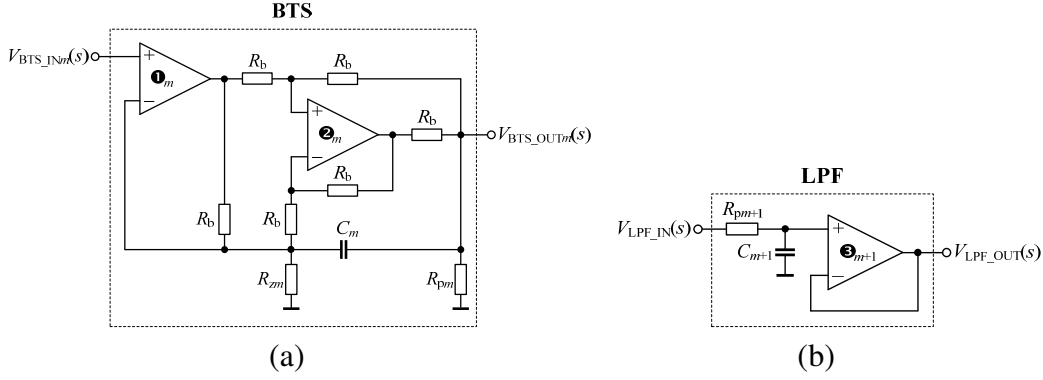
Fig. 4.2: (a) Realization of a bilinear transfer segment and (b) low-pass filter using Op-Amps

$$K_{I^\lambda}(s) = \frac{V_I(s)}{V_S(s)} = K_{BTS\_1}(s)K_{BTS\_2}(s)\ldots K_{BTS\_m}(s)K_{LPF}(s) =$$

$$= \prod_{i=1}^{m}\left[\frac{2sC_m + \left(R_b \parallel R_{zm}\right)}{2sC_m + \left(R_b \parallel R_{pm}\right)}\right]\left(\frac{1}{sC_{pm+1}R_{pm+1}+1}\right) = (\tau_\lambda s)^{-\lambda}. \tag{4.2}$$

Generalized TF (4.2) of a fractional-order I^λ has feature to set m pairs of zeros and poles independently and an additional pole as our design requires. The main advantage of this approach is an easy and low-cost realization of I^λ using discrete passive components and on the shelf available Op-Amps.

Ones the I^λ is designed, its integration constant K_I must be also realized. For this purpose the inverting Op-Amp configuration was selected, which closed loop voltage gain using an ideal Op-Amp can be calculated by ratio of two resistors in the path as $K_I = -R_{I2}/R_{I1}$. The minus sign (−) comes from the inverting Op-Amp configuration and indicates a 180° phase shift.

4.2 Simulation Results

Firstly, the I^λ of order 0.89 (i.e. the time constant $\tau_\lambda^{-\lambda}$) was designed. The five-branch Valsa structure [56] was used, which provides a minimum PAD. Required R and C values were calculated via approach implemented in Matlab with the following inputs: pseudo-capacitance $C_\lambda = 20\ \mu F \cdot sec^{-0.11}$, bandwidth (CPZ) from 30 mHz up to 100 Hz (> 3 decades), CPA −80.1° (i.e. $\lambda = 0.89$), and PAD = ±1°. Preliminary calculations showed that five BTSs ($m = 5$) and a LPF are required in the constant phase block shown in Fig. 4.2 in order to achieve the design specification. Note that the LPF is used for correction purposes of additional pole in Valsa structure. As the next step, zero and pole frequencies were recalculated and corresponding passive component values of R_{zm}, R_{pm}, R_{pm+1}, C_m, and C_{pm+1} obtained via Matlab algorithm and optimized using modified least squares quadratic method.

Ideal and simulated gain and phase responses of the I^λ in frequency domain are given in Fig. 4.3. Selected zooms and equivalent equations for fitting the gain and phase in CPZ 45 mHz – 115 Hz via natural logarithm and linear regressions, respectively, are provided inside Figures. Following [57], design parameters of the FOPI$^\lambda$ controller: $K_P = 1.37$, $K_I = 2.28$, and $\lambda = 0.89$. As the I^λ is designed, the remaining design parameters can be recalculated, which are the
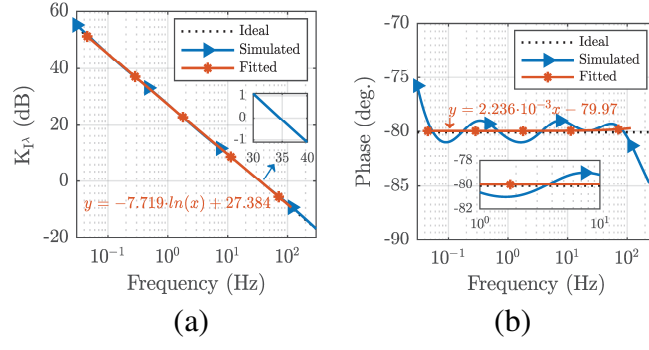
Fig. 4.3: Ideal, simulated, and fitted (a) gain and (b) phase responses of 0.89-order integrator
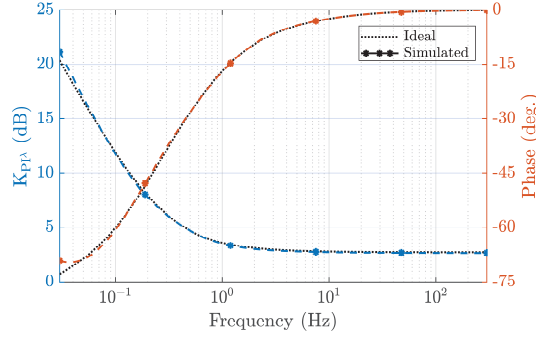

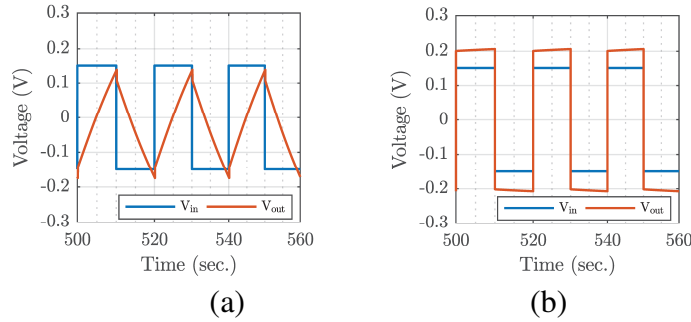Fig. 4.4: Ideal and simulated gain and phase responses for the proposed FOPI$^\lambda$ controller

Fig. 4.5: Time-domain responses of proposed (a) I$^\lambda$ and (b) FOPI$^\lambda$ controller with applied square wave input voltage signal with frequency 100 mHz

following: $R = R_{P1} = R_{P3} = 10\ \text{k}\Omega$, $R_{P2} = 13.7\ \text{k}\Omega$, $R_{PI1} = 27.4\ \text{k}\Omega$, $R_{PI2} = 1.3\ \text{k}\Omega$, and $R_{PI3} = 24.9\ \text{k}\Omega$. An ideal and simulated gain and phase responses of the FOPI$^\lambda$ are given in Fig. 4.4 confirming the accurate operation of the controller.

Moreover, in order to illustrate the time-domain performance of I$^\lambda$ and FOPI$^\lambda$ controller, transient analyses were performed and results are depicted in Fig. 4.5. A square wave input signal with amplitude 150 mV and frequency 100 mHz ($T_D = 0$, $T_R = 1$ ms, $T_F = 1$ ms, $T_{PW} = 10$ s, $T_{PER} = 20$ s, i.e. $12\tau_\lambda^{-\lambda}$) was applied to both circuits. Hence, following the theory, in Fig. 4.5(a) the simulated output signal of the I$^\lambda$ has triangular waveform, while Fig. 4.5(b) indicates increasing gain in the proposed FOPI$^\lambda$ controller as the effect of the K_P.

5   FABRICATION OF A FRACTIONAL-ORDER CAPACITOR

In this chapter, fabrication of a FOC using the hexagonal boron nitride (*h*BN) -ferroelectric polymer blends is investigated. The tunability of the constant phase is obtained using only two tuning knobs e.g., different volume ratio of *h*BN and multi-walled carbon nanotube (CNT). This

fabrication process is therefore quite simple rather than previously fabricated ones [24], [32]. Fig. 5.1 schematically shows an exemplary FOC that has fractional order impedance. The proposed FOC integrates layers of two conductive films, and between them polymer composite with significantly improved CPA, CPZ, and phase angle variation performance. The device is mounted PCB with having one common and nine pins while each showing a FOC characteristic.

It can be categorized between solid-state and passive FOCs. The presented FOCs show better performance in terms of fabrication cost and dynamic range of constant phase angle compared to FOCs from already existing devices. It is important make clear here that this schematic is previously proposed by our collaborators [24], [29] however the study based on hBN-ferroelectric polymer was not investigated.

5.1 Method

An FOC requires an insulator with high dielectric constant, dissipation factor, and dielectric loss. One potential candidate with such electrical properties is P(VDF-TrFE-CFE) terpolymer. Thus, it is a good reason to explore the possibility of using terpolymer in FOC fabrication. They are easily available in the market and good candidates after a closer look at the behavior of the phase angle.
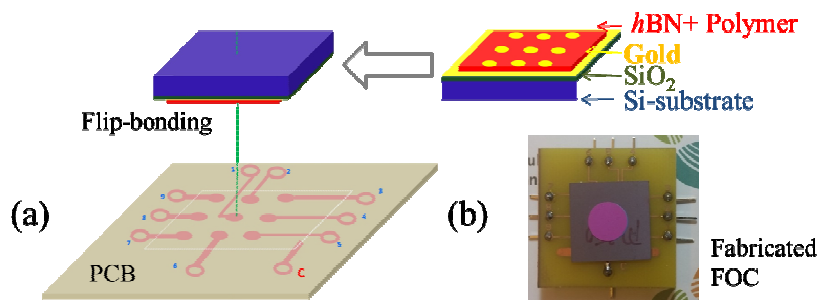

Fig. 5.1: Illustration showing FOC fabrication from bilayer polymer. Photograph showing the final device [29]

This behavior can be tracked by studying the relaxation phenomenon due to polarization, e.g. dipolar (orientation), ionic and interfacial polarization, in polymer dielectrics. Using the phenomenon above and the formulas of permittivity from [38], the hBN is selected as a good candidate to fabricate hBN-ferroelectric polymer based FOC. The fabrication procedure is given as the following:

- 200 mg P(VDF-TrFE-CFE) is dissolved in a 2 ml solvent, N, N-Dimethylformamide (DMF), under constant stirring at room temperature for two days to obtain 0.1 g/ml polymer solution.
- The hBN powders are dispersed in DMF at a concentration of {50, 100, 150, 200, 250} mg/ml and stirred one hour using ultrasonication.
- {5, 10, 15} mg of CNTs are suspended in 1 ml DMF, and dispersed via ultrasonication for 1 hour.
- The dispersed CNT solutions are poured onto the dissolved hBN:P(VDF-TrFE-CFE) polymer solution and mixed under continuous stirring for another 24 hours. This step is valid only for hBN:P(VDF-TrFE-CFE):CNT composites.
- 10 nm Ti followed by 190 nm Au is deposited on Si/SiO$_2$ wafers via DC sputter to define the bottoms of the electrodes.

- Then, the composite solutions are drop-casted onto the Au-deposited 2 cm x 2 cm wafers and dried for 12 hours 90°C under a vacuum.
- The circular Au electrode with 3 mm diameter and 200 nm thickness is deposited by similar method using a shadow mask to permit the fabrication of nine individual FOCs on a 2 cm x 2 cm sample area. The FOC fabrication process is depicted in Fig. 5.1.

Two types of FOCs are fabricated using two different knobs. First is the hBN:P(VDF-TrFE-CFE) polymer blend while second is its composition with CNT. Their material and electrical characterization with different volume ratios of hBN and CNT are given in following chapters.

5.2 Characterization of the Device

The transmission electron microscopy (TEM) image in Fig. 5.2 shows the P(VDF-TrFE-CFE) composite with fillers of hBN and CNT with a 0.5 μm and 200 nm lateral size The CNTs are clearly distinguished from the polymer in the TEM image of the composite provided in Fig. 5.2.
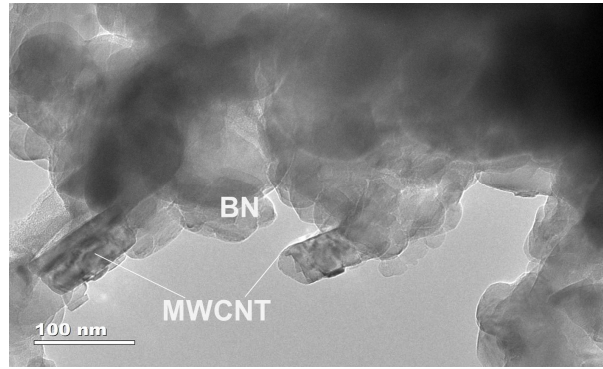

Fig. 5.2: TEM image of the hBN polymer composites with CNT

5.3 Results and Discussions

A solid-state FOC design based on hBN: P(VDF-TrFE-CFE) polymer composite is presented. Results are optimized within a frequency range of 100 Hz – 10 MHz. The best, optimum devices are found and shown in Fig. 5.3 using {200, 250} mg hBN, 100 mg hBN mix with 8 mg CNT, and 150 mg hBN mix with 6 mg CNT –polymer composites with ±2.9°, ±2.2°, ±4°, ±3.2° phase error, respectively. To the best of the author' knowledge, these are best results in given bandwidth until now in open literature. Moreover, the advantages of this new method can be summarized as:
- Fabrication cost of this new FOC is expected to be lower than that of the previously developed FOCs [43]
- Fabrication process employs simple solution-mixing and drop-casting approach
- Relatively small error in larger dynamic range
- Variability of the phase reached with controlling two tuning parameter: concentration of hBN or CNT

This work demonstrates that FOCs fabricated using CNT-ferroelectric polymers composites have the potential to become essential components for reliable/robust electrical and electronic systems.
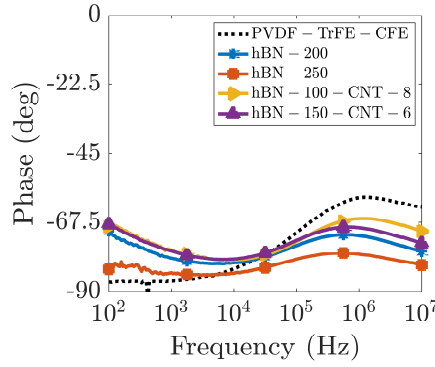
Fig. 5.3: Constant phase angle responses of best *h*BN polymer composite

6 ANALYSIS AND VERIFICATION OF IDENTICAL- AND ARBITRARY-ORDER SOLID-STATE FRACTIONAL-ORDER CAPACITOR NETWORKS

The lossy nature of the dielectric material in capacitors and their electrical conductivity does not allow us to treat them as ideal capacitors since their impedances show a complex frequency-dependent behavior. Due to this fact a FOC, also called as constant phase element, possess both a real and imaginary impedance part $Z(j\omega) = 1 \Big/ \left(\omega^{\alpha} C_{\alpha} \left[\cos\left(\frac{\alpha\pi}{2}\right) + j\sin\left(\frac{\alpha\pi}{2}\right) \right] \right)$ while its phase is frequency independent. However, an ideal capacitor has only an imaginary part [8]. This is particularly important, if the proposed application requires a configuration using capacitors, where errors accumulate the metrics of the individual components. Therefore, firstly, the general formulas for impedance, magnitude, and phase responses of series- and parallel-connected *n* FOCs are derived. Secondly, fabrication process and experimental characterization of three types (orders 0.69 (TP2), 0.92 (P2), 0.62 (G2)) [24], [29] of solid-state compact and stable-in-phase (in the measured frequency range 0.2 MHz – 20 MHz) electric passive FOCs are explained. The experimental results for two and three series- and parallel-, FOCs are presented in following sub-section.

6.1 Mathematical Description of *n* FOCs Connection

6.1.1 Series Connection

In particular, having multiple FOCs in a circuit, the main aim is to replace them with a single equivalent capacitor and/or reach a desired phase angle with a combination of arbitrary-order capacitors. Therefore, the general formulas for equivalent impedance, magnitude and phase responses of *n* FOCs connected in series are expressed as (6.1), (6.2) and (6.3), respectively, where the indexes from *i* to *k* are the numbers of FOCs, each counted from 1 to *n*. The function of the sum is valid under the condition that $i < j < \ldots < l$ and $k \neq i, j, \ldots, l$.

$$Z_{\text{eq,s}}(s) = Z_{\alpha_1} + Z_{\alpha_2} + Z_{\alpha_3} + \ldots + Z_{\alpha_n} = \sum_{i=1}^{n} \frac{1}{s^{\alpha_i} C_{\alpha_i}} . \ (\Omega) \qquad (6.1)$$

$$\left|Z_{\mathrm{eq,s}}\left(s\right)\right|=\frac{\sqrt{\displaystyle\sum_{\substack{i,j,\dots,l,k=1\\i<j<\dots<l\\k\neq i,j,\dots,l}}^{n}\omega^{2\left(\alpha_i+\alpha_j+\dots+\alpha_l\right)}\frac{1}{C_{\alpha_k}^{2}}+2\left\{\displaystyle\sum_{\substack{i,j,\dots,l,k=1\\i<j<\dots<l\\k\neq i,j,\dots,l}}^{n}\omega^{\alpha_i+\alpha_j+\dots+\alpha_l+2\alpha_k}\cos\left[\left(\alpha_i-\alpha_j\right)\frac{\pi}{2}\right]\right\}}}{\displaystyle\prod_{i=1}^{n}\omega^{\alpha_i}},$$

<div align="right">(Ω)   (6.2)</div>

$$\mathrm{Arg}\left[Z_{\mathrm{eq,s}}\left(s\right)\right]=\tan^{-1}\left\{\frac{\displaystyle\sum_{\substack{i,j,\dots,l,k=1\\i<j<\dots<l\\k\neq i,j,\dots,l}}^{n}\omega^{\alpha_i+\alpha_j+\dots+\alpha_l}\frac{1}{C_{\alpha_k}}\sin\left[\left(\alpha_i+\alpha_j+\dots+\alpha_l\right)\frac{\pi}{2}\right]}{\displaystyle\sum_{\substack{i,j,\dots,l,k=1\\i<j<\dots<l\\k\neq i,j,\dots,l}}^{n}\omega^{\alpha_i+\alpha_j+\dots+\alpha_l}\frac{1}{C_{\alpha_k}}\cos\left[\left(\alpha_i+\alpha_j+\dots+\alpha_l\right)\frac{\pi}{2}\right]}\right\}-\sum_{i=1}^{n}\left(\alpha_i\right)\frac{\pi}{2},$$

<div align="right">(Degree)   (6.3)</div>

6.1.2 Parallel Connection

When n FOCs with arbitrary order are connected in parallel, the equivalent total impedance, magnitude, and phase can be expressed as:

$$Z_{\mathrm{eq,p}}\left(s\right)=\frac{1}{s^{\alpha_1}C_{\alpha_1}+s^{\alpha_2}C_{\alpha_2}+s^{\alpha_3}C_{\alpha_3}+\dots+s^{\alpha_n}C_{\alpha_n}}=\frac{1}{\displaystyle\sum_{i=1}^{n}s^{\alpha_i}C_{\alpha_i}}.\qquad\text{(Ω)}\qquad(6.4)$$

$$\left|Z_{\mathrm{eq,p}}\left(s\right)\right|=\frac{1}{\sqrt{\displaystyle\sum_{i=1}^{n}\omega^{2\alpha_i}C_{\alpha_i}^{2}+2\left[\displaystyle\sum_{\substack{i,j=1\\i<j}}^{n}\omega^{\alpha_i+\alpha_j}C_{\alpha_i}C_{\alpha_j}\cos\left(\alpha_i-\alpha_j\right)\frac{\pi}{2}\right]}},\qquad\text{(Ω)}\qquad(6.5)$$

$$\mathrm{Arg}\left[Z_{\mathrm{eq,p}}\left(s\right)\right]=-\tan^{-1}\left[\frac{\displaystyle\sum_{i=1}^{n}\omega^{\alpha_i}C_{\alpha_i}\sin\left(\alpha_i\frac{\pi}{2}\right)}{\displaystyle\sum_{i=1}^{n}\omega^{\alpha_i}C_{\alpha_i}\cos\left(\alpha_i\frac{\pi}{2}\right)}\right].\qquad\text{(Degree)}\qquad(6.6)$$

The frequency and number of capacitors influence only the magnitude, while the order affects both the magnitude and phase responses. Units of impedance, magnitude, and phase responses of FOCs remain in both the series and parallel cases the same as in the integer-order case, i.e. the impedance and magnitude are in units of ohms and the phase in units of degrees, respectively.

6.2 Experimental Verification

6.2.1 Series Connection of Arbitrary-Order FOCs

The results obtained, including each individual FOC, are shown in Figs. 6.1(a) (magnitude) and (b) (phase). To estimate the equivalent order α (or phase), the magnitude data measured are fitted to the function $\log|Z| = \alpha \log f + \log(2\pi)^{\alpha} C_{\alpha}$ using the LLS method. From the results the orders are evident of FOCs as single devices TP2, P2, G2, i.e. 0.69, 0.92, and 0.62, with corresponding phases $-61.91°$, $-82.59°$, and $-55.68°$, while their equivalent orders from series connections are found to be 0.85, 0.65, 0.85, 0.81. The equivalent magnitudes vary in ranges of $(67.2 \rightarrow 1.26, 17.87 \rightarrow 0.829, 61.69 \rightarrow 1.16,$ and $72.38 \rightarrow 1.69)$ kΩ, respectively.
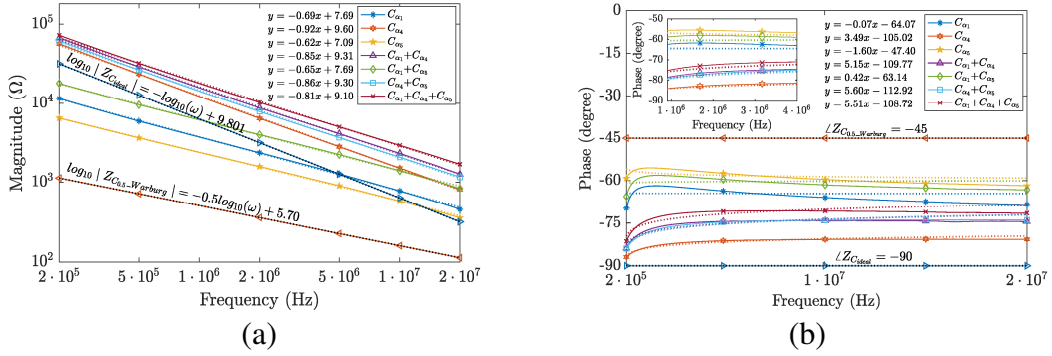

Fig. 6.1: Two and three arbitrary-order FOCs connected in series: (a) magnitude, (b) phase responses

6.2.2 Parallel Connection of Arbitrary-Order FOCs

The magnitude and phase responses of the equivalent impedances are shown in Figs. 6.2(a) and (b). The equivalent new orders, which are achieved using the LLS fitting and given in Fig. 6.2(a) next to the legend, are found to be 0.74, 0.64, 0.68, and 0.66. As can be observed, the orders match well to those obtained from the measured phase responses, which are depicted in Fig. 6.2(b). Overall, the equivalent impedances have capacitive behavior and vary in ranges of $(9.24 \rightarrow 0.27)$ kΩ, $(4.11 \rightarrow 0.19)$ kΩ, $(5.84 \rightarrow 0.24)$ kΩ, and $(3.78 \rightarrow 0.16)$ kΩ, respectively. It is also worth noting that the relative phase errors at f_c are again small and vary in the range of -2.65% to 0.10%.
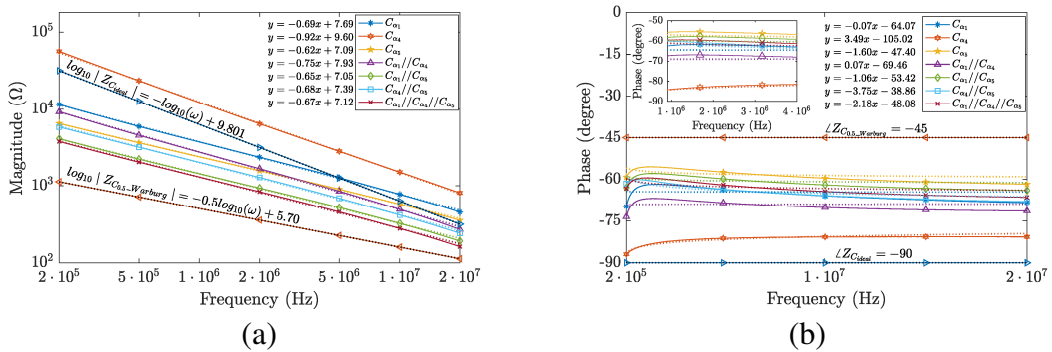

Fig. 6.2: Two and three arbitrary-order FOCs connected in parallel: (a) magnitude, (b) phase responses

6.3 Brief Discussion of Results

Figures 6.3(a) and (b) give a comparison of the calculated, measured, and fitted line values of the magnitude and phase responses of three arbitrary-order series- and parallel-connected FOCs. Furthermore, the equivalent pseudo-capacitance versus frequency is plotted for both circuits in Fig. 6.3(c). The pseudo-capacitance of both FOCs is constant in the same region as the phase is. The normalized histograms show low absolute error between the measured and the calculated equivalent integer-order capacitance values, which is less than 1 pF and 4 pF, respectively, for the series- and parallel-connected FOCs. It can be concluded that the equivalent impedances of fabricated arbitrary-order FOCs connected in series and parallel exhibit the same capacitive behavior as integer-order capacitors.
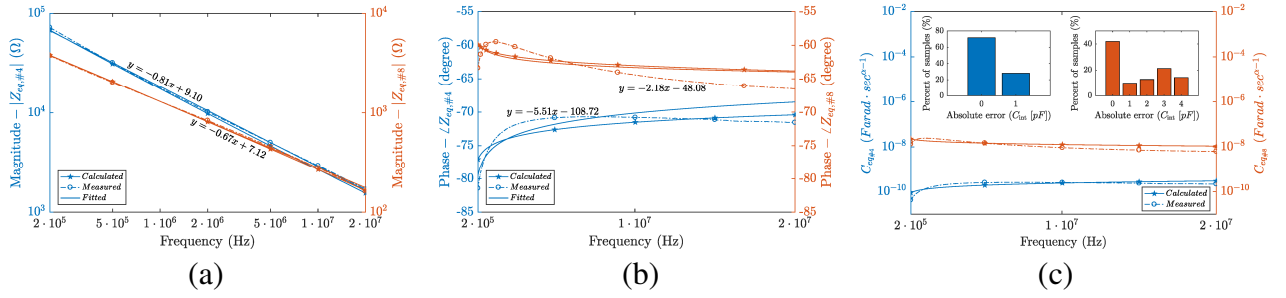

Fig. 6.3: Comparison of (a) magnitude, (b) phase, and (c) pseudo-capacitance versus frequency of three arbitrary-order FOCs connected in series (#4 - blue color) and parallel (#8 - orange color)

7 DESIGN AND IMPLEMENTATION OF FRACTIONAL-ORDER OSCILLATORS

In this chapter, design of voltage-mode fractional-order oscillators, fractional-order Colpitts and Wien oscillators are studied. Main focus of this chapter is to study the effect of FOEs in system equations which results in several design features such as possibility of changing the frequency of oscillation (FO) and condition of oscillation (CO), amplitude and phase etc.

Their design in integrated circuit design is another study point. Many classical fractional-order oscillators were presented using conventional op-amps or its equivalent macromodels. Although the aforementioned solutions could be implemented using commercially available discrete-component ICs, from the integration point of view they suffer from the increased transistor count that they are required for implementing the active. Moreover, part of attention will be on validity check of Barkhausen conditions. Because, an accurate oscillator models are designed with differential equations to be certainly nonlinear due to the lack of unstable periodic oscillations in the pure integer-order or fractional-order linear systems, and also insufficient oscillation condition according to the Barkhausen criteria.

7.1 Compact MOS-RC Voltage-Mode Oscillators

Replacing the ideal capacitors C_i for $i = \{1, 2\}$ with a FOC ($C_1 \Rightarrow C_\alpha$, $C_2 \Rightarrow C_\beta$) in Fig. 7.1 with impedance of $Z_\alpha(s) = 1/(s^\alpha C_\alpha)$, $Z_\beta(s) = 1/(s^\beta C_\beta)$, the linear fractional-order system can be described as:

$$\begin{pmatrix} \dfrac{d^{\alpha}V_{C_{\alpha}}}{dt^{\alpha}} \\[2ex] \dfrac{d^{\beta}V_{C_{\beta}}}{dt^{\beta}} \end{pmatrix} = \begin{pmatrix} \dfrac{g_{m1}}{C_{\alpha}} & -\left(\dfrac{g_{m1}}{C_{\alpha}}+\dfrac{1}{RC_{\alpha}}\right) \\[2ex] \dfrac{g_{m2}}{C_{\beta}} & -\dfrac{g_{m2}}{C_{\beta}} \end{pmatrix} \begin{pmatrix} V_{C_{\alpha}} \\[2ex] V_{C_{\beta}} \end{pmatrix}, \tag{7.1}$$

Hence, the CE from (7.1) becomes in general form as:

$$\text{CE}: \quad s^{\alpha+\beta} - s^{\beta}\frac{g_{m1}}{C_{\alpha}} + s^{\alpha}\frac{g_{m2}}{C_{\beta}} + \frac{g_{m2}}{C_{\alpha}C_{\beta}R} = 0. \tag{7.2}$$

By solving (7.2) the CO and FO of fractional-order oscillator can be obtained as:

$$\text{CO}: \quad \omega^{\alpha+\beta}\cos\frac{(\alpha+\beta)\pi}{2} - \frac{g_{m1}}{C_{\alpha}}\omega^{\beta}\cos\frac{\beta\pi}{2} + \frac{g_{m2}}{C_{\beta}}\omega^{\alpha}\cos\frac{\alpha\pi}{2} + \frac{g_{m2}}{RC_{\alpha}C_{\beta}} = 0,$$

$$\text{FO}: \quad \omega^{\alpha+\beta}\sin\frac{(\alpha+\beta)\pi}{2} - \frac{g_{m1}}{C_{\alpha}}\omega^{\beta}\sin\frac{\beta\pi}{2} + \frac{g_{m2}}{C_{\beta}}\omega^{\alpha}\sin\frac{\alpha\pi}{2} = 0. \tag{7.3}$$

In fractional-order case the relation between the outputs of the oscillator is:

$$\frac{V_{o1}}{V_{o2}} = -\frac{g_{m1}R+1}{s^{\alpha}RC_{1\alpha}+1}, \tag{7.4}$$

while the phase difference "φ" between two outputs V_{o1} and V_{o2} can be calculated as:

$$\varphi = \tan^{-1}\frac{\omega^{\alpha}\sin(0.5\alpha\pi)}{\omega^{\alpha}\cos(0.5\alpha\pi)-\dfrac{g_{m1}}{C_{1\alpha}}} - \pi = -\tan^{-1}\frac{\omega^{\beta}\sin(0.5\beta\pi)}{\omega^{\beta}\cos(0.5\beta\pi)+\dfrac{g_{m2}}{C_{2\beta}}}. \tag{7.5}$$

The fractional-order cases are studied for selected orders $\alpha = \{0.2;\ 0.2\}$ and $\beta = \{1;\ 0.8\}$, respectively. The fractional-order capacitors were realized using the Foster I network. The values of passive elements have been calculated by employing the second-order CFE method. The calculated oscillation start-up conditions are $C_{2\beta} = \{6.31\ \text{n};\ 89.9\ \text{n}\}\text{Fs}^{(\beta-1)}$ and the FOs are $f_{0\_\text{theor\_fract}} = \{15.9\ \text{k};\ 9.64\ \text{k}\}\text{Hz}$, while the simulated FOs are 15 kHz, and 10 kHz, respectively. Transient responses of the outputs for fractional-order cases are shown in Figs. 7.2(a)–(b). The following peak-to-peak values of oscillation amplitudes were simulated for outputs $\{V_{o1};\ V_{o2}\}$: Case 1 $\{608.9;\ 602.8\}$mV, and Case 2 $\{575.1;\ 542.1\}$mV, respectively. Here the theoretical ratios of amplitudes according to (7.4) are 1; 1.05.
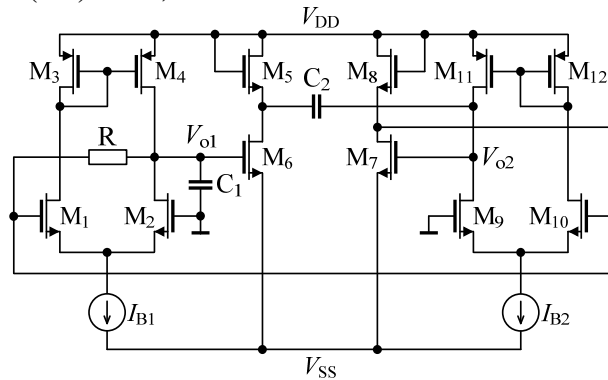

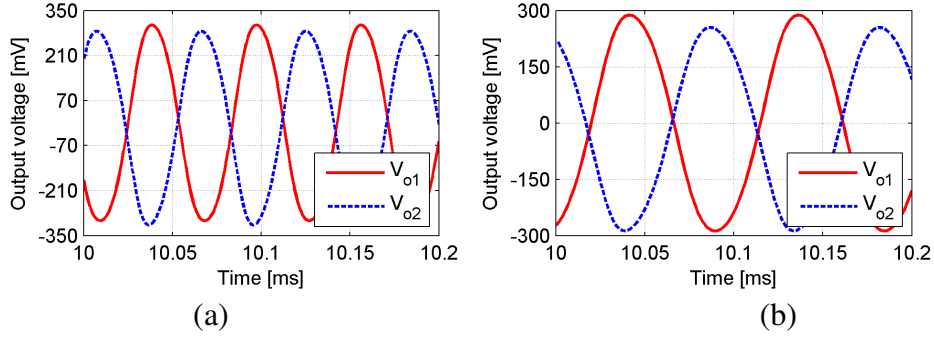Fig. 7.1: The proposed compact voltage-mode oscillator using OTAs and IVBs

Fig. 7.2: Transient responses of the output voltages: (a) $\alpha = 0.2$ and $\beta = 1$, (b) $\alpha = 0.2$ and $\beta = 0.8$

7.2 CMOS-RC Colpitts Oscillator Design Using Floating Fractional-Order Inductance Simulator

Here, Colpitts oscillator implemented using two CMOS-based transconductors is shown in Fig. 7.3. The CE has the following general form:

$$\text{CE}: s^{\alpha+\beta+\gamma} RC_\alpha C_\beta L_\gamma + s^{\alpha+\gamma} C_\alpha L_\gamma + s^\alpha RC_\alpha + s^\beta RC_\beta + Rg_\text{m} + 1 = 0. \qquad (7.15)$$

In analog electronics, due to the large silicon area, cost, and lack of electronically tunability, CMOS-based inductance simulators are used. The CMOS implementation of the proposed FOI simulator is shown in Fig. 7.4. It consists from two inverting voltage buffers (IVBs), two unity-gain current followers (CFs), and one simple transconductor. Considering described ABBs, one capacitor, and assuming matching condition $g_\text{m} = 1/R_{\text{CF\_in1}}$, while $R_{\text{CF\_in}k} \approx R_k{}'$, routine circuit analysis yields the following short circuit admittance matrix $[Y_{L_\gamma}] = \dfrac{1}{s^\gamma L_\gamma}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$, from which

$L_\gamma = R_1{}' R_2{}' C_\gamma$. As it can be seen the equivalent inductance value is adjustable by order of the FOC (or phase). The simulated phase (pseudo)-inductance responses of 0.75 and integer-order inductance simulator are shown in Fig. 7.5. In this case the circuit was simulated with C and C_γ given above, which in fractional-order case theoretically resulted in $L_{\gamma\_\text{theor}} = 17.3$ mH·s$^{-0.25}$ and the simulated one has a value $L_{\gamma\_\text{sim}} = 18.4$ mH·s$^{-0.25}$. Considering ±5 degree deviation in phase, the useful frequency range for $L_{0.75}$ is about 138 kHz up to 2.45 MHz.
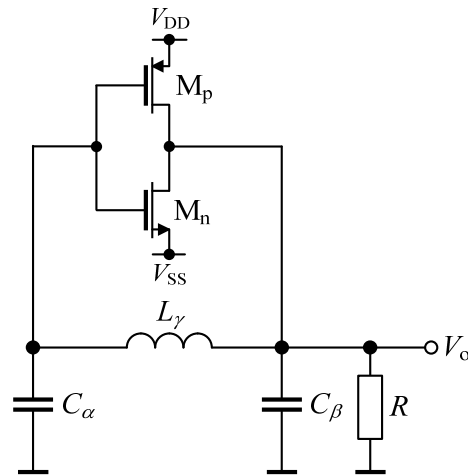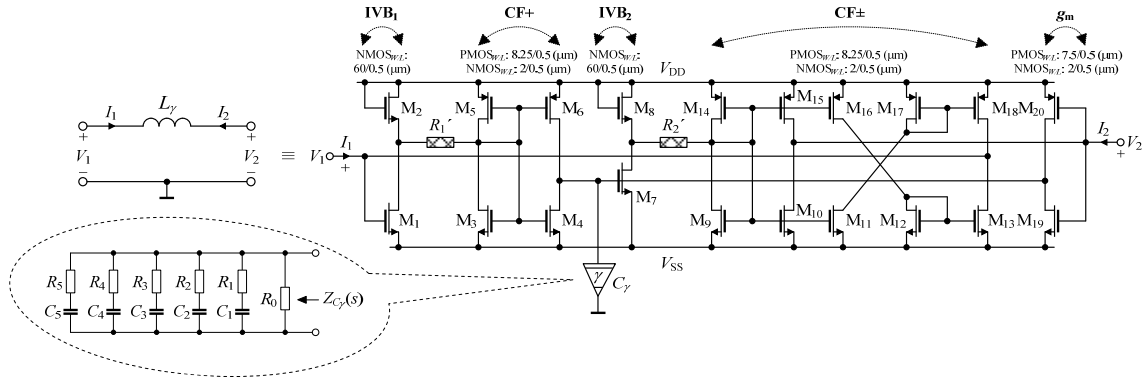

Fig. 7.3: Voltage-mode Colpitts oscillator

Fig. 7.4: Proposed CMOS fractional-order inductance simulator including RC network emulating fractional-order capacitor

Both 2.75^{th} and 3rd order Colpitts oscillator were designed with CMOS transconductance and capacitor values were selected as $C_1 = C_2 = 61$ pF. The calculated oscillation start-up condition is $R = 28.13$ kΩ and the FO is $f_{0\_theor\_fract} = 1.3$ MHz, while the simulated CO is $R = 30$ kΩ and FO is 1.58 MHz. On the other hand, the CO is 1.8 kΩ and FO is 1.26 MHz in integer-order case. The steady-state output voltage waveforms of both cases are depicted in Fig. 7.6. For the output the generated peak-to-peak value is 1.34 V and 1.06 V for 2.75^{th} and 3rd-order, respectively, while the total harmonic distortion (THD) at the outputs are about 4.1% and 5.3% for the fractional and integer cases, respectively.
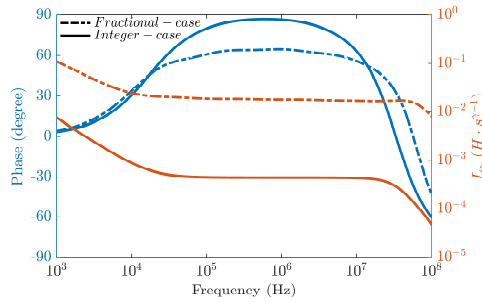

Fig. 7.5: Phase (left) and (pseudo)-inductance (right) responses of proposed 0.75 and integer-order CMOS inductance simulator

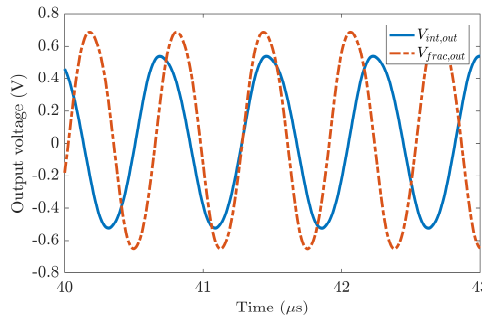
Fig. 7.6: Simulated output voltage waveforms of the proposed 2.75^{th} and 3rd-order Colpitts oscillator

7.3 Fractional-Order Wien Oscillator

A PCB-compatible FOCs using molybdenum disulfide (MoS_2)-ferroelectric polymer composites

are first presented in [32]. In this chapter, their application in fractional-order Wien oscillator is shown. The values of two fabricated FOCs at 25 kHz are $C_{\alpha 1} = 37.2$ nF·s$^{-0.35}$ and $C_{\alpha 2} = 55.2$ nF·s$^{-0.34}$. In the circuit of Fig. 7.7, the passive element values are $R_1 = R_2 = 10$ kΩ, $R_2 = 47$ kΩ.. The measured frequency of oscillation (FO) is 24.87 kHz as seen in Fig. 7.8(a) while the one calculated using the above values is 23.52 kHz [15]. The measurement is repeated after the FOCs are replaced with two conventional capacitors with a capacitance value of 30 nF and 50 nF. For this case the FO is measured to be 0.414 kHz as seen in Fig. 7.8(b). This demonstrates that the fractional-order Wien oscillator has a significantly higher FO that its conventional counterpart. It should also be noted here that the peak-to-peak amplitudes of the output voltage of both oscillators are same and equal to 1.88 V.
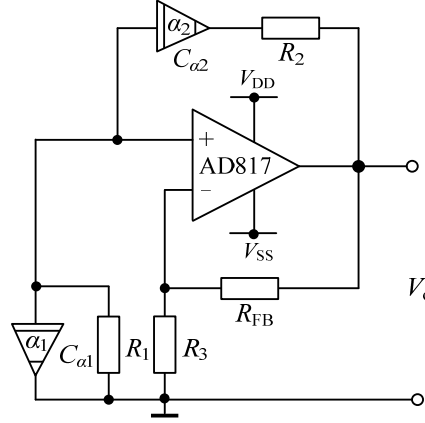
Fig. 7.7: Schematic of fractional-order Wien oscillator

	(a)		(b)
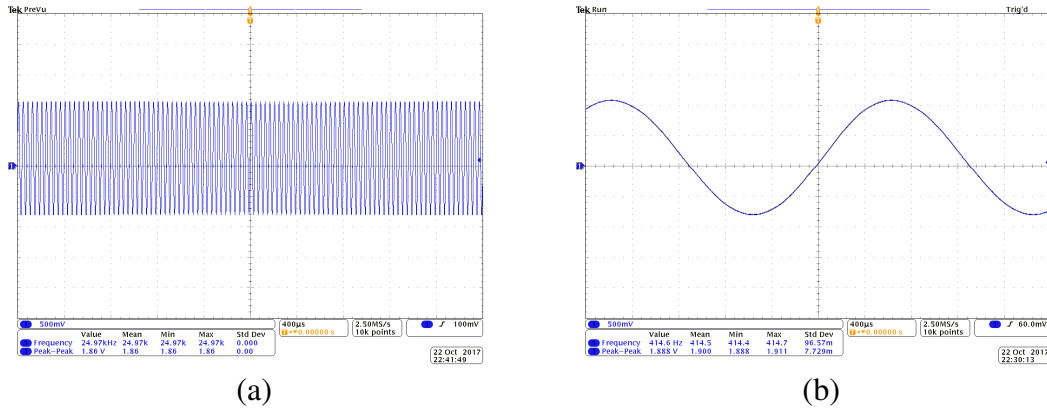
Fig. 7.8: Measured steady-state output voltage waveform of (a) the fractional-order Wien oscillator and (b) the conventional one as an inset

8 CONCLUSIONS

Throughout this thesis, a wide range of problems associated with analog circuit design of fractional-order dynamic systems are covered: passive component optimization of resistive-capacitive and resistive-inductive type FOEs, active realization of FOCs, analog integrated circuit design of fractional-order integrator, robust fractional-order proportional-integral control design, investigation of different materials for ultra-wide band, low phase error FOC, possible low- and high-frequency realization of fractional-order oscillators in analog circuit design, stability study of solid-state FOCs in series-, parallel- and interconnected networks. The major target of this thesis is

to develop novel stable and accurate solutions in the form of FOE realization, analog circuit design of fractional-order dynamic systems and their performance evaluation frameworks to significantly improve requirements of analog circuit designs.

When discussing distributed element realization of FOEs and fabrication of FODs in Chapter 2, the need for joint study of precise modelling and characterizing electrical properties of dielectric materials is realized. Several structures have been proposed for FOEs design and studied within fractional-order systems. Highlighting important practical trade-off in Chapter 2, the results from Chapter 3, 4 and 5 indicated significant promise for future research in the area of analog circuit design of fractional-order systems. In particular, in Chapter 2, an optimization of passive component values in RC/RL networks improves the constant phase angle and makes them easily use in experimental verification of fractional-order systems. Extending this idea on precise modelling and then the fabrication of FODs, a new solid-state FOC based on hBN-P(VDF-TrFE-CFE) polymer composites is presented in Chapter 5 and analyzed within a frequency range of $100\,\text{Hz} - 10\,\text{MHz}$ and minimum $\pm 2.2°$, maximum $\pm 4°$ phase error.

Whereas there is a natural connection between Chapters 3 and 5, the fractional-order integral design using cascade of BTSs is presented in Chapter 4. The structure benefits from the rational approximation of irrational impedance functions and their zero-pole distributions. An example for the analog integrated circuit design using ABBs of BTSs is shown and studied FOPI$^\lambda$ controller. There is still need to investigate proper approximation and structure to build a low cost hardware for industrialization. However, the preliminary results prove the possibility of the idea and are currently sufficient to move on this direction.

While improving the performance and increasing the variability of FOEs and FODs, their stability and accuracy becomes important. This can be simply tested in circuit network connections. Therefore, the series-, parallel- and interconnected identical- and arbitrary-order FOCs are studied mathematically in Chapter 6.

Derived formulas are experimentally verified. I believe that this study might be one of the fundamental topics of electronic circuit lectures in fractional domain in the future.

In Chapter 7, the effect of FOEs on system design equations of fractional-order oscillators is investigated. For that, new design structures for compact voltage-mode fractional-order oscillators are presented. Beside it, the classic oscillators e.g. Colpitts and Wien are studied. Some of early fabricated FOCs are used in application of Wien oscillator. Our analysis confirms that it is possible to reach extremely low- and high- frequency FO by only changing the order without necessity to use high value capacitors or inductors.

The complex research summarized in this thesis results in both theoretical innovations and practical applications. It is expected that the proposed solutions [16], [23], [25]−[28], [30], [31], [33], [54], [58]−[62] and their future extensions will become of significant importance toward further development of analog implementation of fractional-order systems. These solutions are primarily intended for, but not limited to, fractional-order integrators, fractional-order differentiators, analog integrated circuit design, nanofabrication, and electronic component producers.

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Curriculum Vitae

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PROFILE

- Researcher on analog integrated circuit design of fractional-order circuits
- Experienced in modelling and fabrication of fractional-order elements
- Author and co-author of 13 journal, 32 conference papers
- Multidisciplinary international experience as R&D engineer, lecturer, and researcher

QUALIFICATION

Position

2016 – present:	*Research Assistant* – Dept. of Telecommunications, Brno University of Technology
2017 – 2018:	*Teaching Assistant* – Dept. of Radio Electronics, Brno University of Technology

Education

2016 – till now	*Ph.D.* – Brno University of Technology (specialization: Electronics and Communication)
2013 – 2015	*M.Sc.* – Yildiz Technical University, Turkey (specialization: Electronics and Communication)

PROFESSIONAL ACTIVITIES

Research Topics of Interest	Fractional-order components & systems; analog integrated circuits with modern active elements, and their applications as filters and oscillators, general element simulator, numerical methods for analysis of electronic networks, computer-aided methods for simulation of electronic circuits.

Selected Internships & Trainings

16/01/ – 18/05/2018:	Freemover Internship at the Sensors Laboratory, King Abdullah University of Science and Technology (KAUST), Thuwal, Saudi Arabia - Supervisor: Prof. Khaled Nabil Salama
24/02/ – 03/03/2018:	COST Action CA15225 "Short Term Scientific Missions (STSM)", University of Sharjah, Emirates - Visited Professor: Prof. Ahmed Elwakil
05 – 08/09/2017:	COST Action CA15225 "Training School on Fractional Order Controllers: From Theory to Application", University of Catania, Italy
05 – 17/03/2017:	COST Action CA15225 "Short Term Scientific Missions (STSM)", University of Patras, Greece - Visited Professor: Prof. Costas Psychalinos
24 – 26/11/2016:	COST Action CA15225 "COST/IEEE-CASS Seasonal Training School in Fractional-Order Systems", Brno, Czech Republic
10/01/ – 10/06/2015:	ERASMUS Exchange Student, Brno University of Technology, Czech Republic

Memberships / Volunteering

Since 2019	IEEE Czechoslovakia Section Student Activities Chair
Since 2017:	IEEE Czechoslovakia Section SP/CAS/COM Joint Chapter Student Chair

2016 – 2018:	IEEE Czechoslovakia Section Brno University of Technology Student Branch Vice-President
Since 2015:	IEEE Circuits and Systems Society (CASS) Member
Since 2015:	Student Member of Institute of Electrical and Electronic Engineers (IEEE)

Selected Editorships / Technical Program Committee (TPC) Memberships

2017:	*Technical Program Committee Member* of 2017 24th IEEE Int. Conference on Electronics, Circuits and Systems (ICECS), Batumi, Georgia, Organized by IEEE CASS - http://icecs2017.org/
2016:	*Organizer* of COST/IEEE-CASS Seasonal Training School in Fractional-Order Systems, Brno, Czech Republic, Organized by IEEE CASS, COST Association, and IEEE Czechoslovakia Section - http://fractal.utko.feec.vutbr.cz/
Since 2016:	*Congress Publicity Chair* of Int. Congress on Ultra-Modern Telecommunications and Control Systems (ICUMT) - https://www.icumt.info
Since 2016:	*Publicity and Social Media Chair* of Int. Conference on Telecommunications and Signal Processing (TSP), Technically co-sponsored by IEEE R8 & IEEE Czechoslovakia Section - http://tsp.vutbr.cz/
Since 2015:	Number of *Peer-Reviewed SCI-E Journal & Conference Proceedings Paper Reviews*: 50

SELECTED RESEARCH RESULTS AND GRANT PROJECTS

Developed Integrated Circuit

2018:	N. Herencsar, R. Sotner, V. Kledrowetz, A. Kartci, J. Jerabek, and J. Koton, *UDE - Universal Differencing Element* (in EUROPRACTICE IC Service).

Participation In Grant Projects

Projects supported by the MŠMT INTER-EXCELLENCE - INTER-COST:

2018 – 2020:	LTC18022: Analogue Fractional Systems, Their Synthesis and Analysis. Holder: doc. Ing. Jan Jeřábek, Ph.D.

Projects supported by the Czech Science Foundation (GA CR):

2019 – 2021:	GA1924585S: Synthesis of Reliable Electrical Phantoms Describing Fractional Impedance Behavior of Real-World Systems. Holder: doc. Ing. Jaroslav Koton, Ph.D.
2016 – 2018:	GJ16-11460Y: Active Devices with Differencing Terminals for Novel Single-Ended and Pseudo-Differential Function Block Design. Holder: doc. Ing. Norbert Herencsár, Ph.D.
2015 – 2017:	GA15-18288S: Research of Signal Integrity at High-Speed Interconnects. Holder: prof. Ing. Lubomír Brančík, CSc.

OVERALL RESEARCH RESULTS (According to Web of Science)

h-index:	8
No. of papers published in SCI-E journals / conferences:	10 / 28
Sum of times cited / without self-citations:	211 / 167
Average citations per item:	5.55
Citing articles / without self-citations:	133 / 102

ABSTRACT

With advancements in the theory of fractional calculus and also with widespread engineering application of fractional-order systems, analog implementation of fractional-order integrators and differentiators have received considerable attention. This is due to the fact that this powerful mathematical tool allows us to describe and model a real-world phenomenon more accurately than via classical "integer" methods. Moreover, their additional degree of freedom allows researchers to design accurate and more robust systems that would be impractical or impossible to implement with conventional capacitors. Throughout this thesis, a wide range of problems associated with analog circuit design of fractional-order systems are covered: passive component optimization of resistive-capacitive and resistive-inductive type fractional-order elements, realization of active fractional-order capacitors (FOCs), analog implementation of fractional-order integrators, robust fractional-order proportional-integral control design, investigation of different materials for FOC fabrication having ultra-wide frequency band, low phase error, possible low- and high-frequency realization of fractional-order oscillators in analog domain, mathematical and experimental study of solid-state FOCs in series-, parallel- and interconnected circuit networks. Consequently, the proposed approaches in this thesis are important considerations in beyond the future studies of fractional dynamic systems.

ABSTRAKT

S pokroky v teorii počtu neceločíselného řádu a také s rozšířením inženýrských aplikací systémů neceločíselného řádu byla značná pozornost věnována analogové implementaci integrátorů a derivátorů neceločíselného řádu. Je to dáno tím, že tento mocný matematický nástroj nám umožňuje přesněji popsat a modelovat fenomén reálného světa ve srovnání s klasickými „celočíselnými" metodami. Navíc nám jejich dodatečný stupeň volnosti umožňuje navrhovat přesnější a robustnější systémy, které by s konvenčními kondenzátory bylo nepraktické nebo nemožné realizovat. V předložené disertační práci je věnována pozornost širokému spektru problémů spojených s návrhem analogových obvodů systémů neceločíselného řádu: optimalizace rezistivně-kapacitních a rezistivně-induktivních typů prvků neceločíselného řádu, realizace aktivních kapacitorů neceločíselného řádu, analogová implementace integrátoru neceločíselného řádů, robustní návrh proporcionálně-integračního regulátoru neceločíselného řádu, výzkum různých materiálů pro výrobu kapacitorů neceločíselného řádu s ultraširokým kmitočtovým pásmem a malou fázovou chybou, možná realizace nízkofrekvenčních a vysokofrekvenčních oscilátorů neceločíselného řádu v analogové oblasti, matematická a experimentální studie kapacitorů s pevným dielektrikem neceločíselného řádu v sériových, paralelních a složených obvodech. Navrhované přístupy v této práci jsou důležitými faktory v rámci budoucích studií dynamických systémů neceločíselného řádu.